

# 1.75-V to 5.5-V Input, 0.6-/1-A Synchronous Step-Down Converter with I<sup>2</sup>C/VSEL Interface

## 1 Features

- 2.3- $\mu$ A operating quiescent current
- Up to 4-MHz switching frequency
- 1% output voltage accuracy
- DVS output from 0.4 V to 1.9875 V (12.5-mV steps)
- I<sup>2</sup>C user interface to adjust
  - Output voltage presets
  - Ramp speed
- VSEL-pin to toggle V<sub>OUT</sub> during operation
- Power good indication
- Supports <6-mm<sup>2</sup> solution size
- Supports <0.6-mm solution height
- Tiny 8-pin, 0.35-mm pitch WCSP package
- Optimized pinout to support 0201 components

## 2 Applications

- [Wearable electronics](#)
- [Portable electronics](#)
- [Mobile phones](#)
- [Medical sensor patches and patient monitors](#)

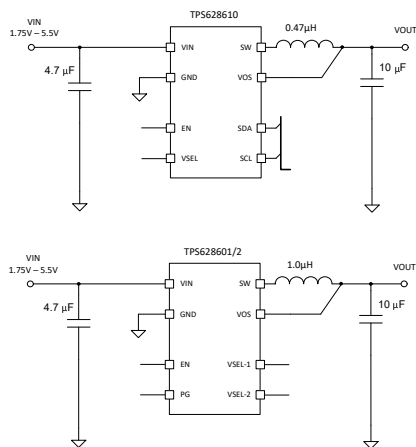
## 3 Description

The TPS6286x devices are high-frequency synchronous step-down converters with I<sup>2</sup>C- and VSEL-Interface. They provide an efficient, flexible, and high-power density point-of-load DC/DC solution. At medium to heavy loads, the converter operates in PWM mode and automatically enters Power Save Mode operation at light load to maintain high efficiency over the entire load current range. The device can also be forced in PWM mode operation for the smallest output voltage ripple. Together, with its DCS-control architecture, excellent load transient performance and tight output voltage accuracy are achieved. With the I<sup>2</sup>C interface and a dedicated VSEL pin, the output voltage is quickly adjusted to adapt the power consumption of the load to the ever-changing performance needs of the application. The TPS6286x family is available with two VSEL pins and four factory preset voltages to allow usage without I<sup>2</sup>C interface.

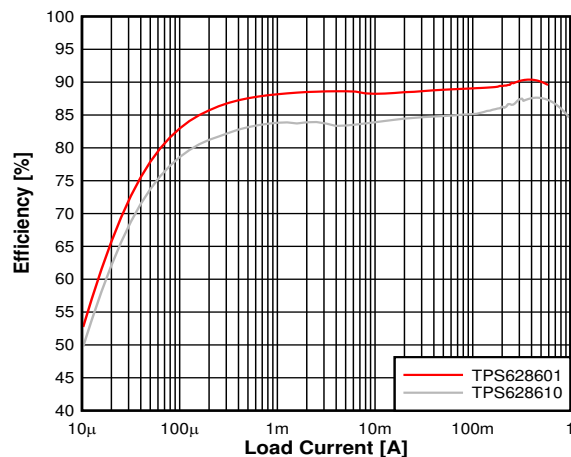
### Device Information

PART NUMBER	CURRENT	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
TPS628610	1 A	DSBGA (8)	0.7 × 1.4 × 0.4 mm
TPS628601	0.6 A	DSBGA (8)	0.7 × 1.4 × 0.4 mm
TPS628600	0.6 A	DSBGA (8)	0.7 × 1.4 × 0.4 mm
TPS628602	0.6 A	DSBGA (8)	0.7 × 1.4 × 0.4 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application



Efficiency Versus I<sub>OUT</sub> at 1.1 V<sub>OUT</sub>, 3.8 V<sub>IN</sub>



## Table of Contents

<b>1 Features</b> .....	1	8.4 Programming.....	13
<b>2 Applications</b> .....	1	8.5 Register Map.....	16
<b>3 Description</b> .....	1	<b>9 Application and Implementation</b> .....	19
<b>4 Revision History</b> .....	2	9.1 Application Information.....	19
<b>5 Device Comparison Table</b> .....	3	9.2 Typical Application, TPS628610.....	19
<b>6 Pin Configuration and Functions</b> .....	3	<b>10 Power Supply Recommendations</b> .....	27
<b>7 Specifications</b> .....	4	<b>11 Layout</b> .....	28
7.1 Absolute Maximum Ratings.....	4	11.1 Layout Guidelines.....	28
7.2 ESD Ratings.....	4	11.2 Layout Example.....	28
7.3 Recommended Operating Conditions.....	4	<b>12 Device and Documentation Support</b> .....	29
7.4 Thermal Information.....	4	12.1 Device Support.....	29
7.5 Electrical Characteristics.....	5	12.2 Receiving Notification of Documentation Updates.....	29
7.6 I <sup>2</sup> C Interface Timing Characteristics.....	6	12.3 Support Resources.....	29
7.7 Typical Characteristics.....	8	12.4 Trademarks.....	29
<b>8 Detailed Description</b> .....	9	12.5 Electrostatic Discharge Caution.....	29
8.1 Overview.....	9	12.6 Glossary.....	29
8.2 Functional Block Diagram.....	9	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	30
8.3 Feature Description.....	10		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

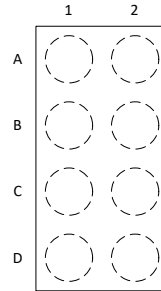
<b>Changes from Revision C (March 2022) to Revision D (May 2022)</b>	<b>Page</b>
• Corrected the internal fixed soft-start time test condition.....	5

<b>Changes from Revision B (September 2020) to Revision C (March 2022)</b>	<b>Page</b>
• Added the TPS628602 to the data sheet.....	1

## 5 Device Comparison Table

ORDERABLE PART NUMBER	OUTPUT CURRENT	DEFAULT $V_O$ SETTING	$f_{sw}$	USER INTERFACE
TPS628600YCH	0.6 A	0.6 V, 1.1 V	1.5 MHz	EN, I2C, VSEL
TPS628601YCH	0.6 A	0.6 V, 0.7 V, 0.8 V, 1.0 V	1.5 MHz	2x VSEL, EN, PG
TPS628610YCH	1 A	0.6 V, 1.1 V	4 MHz	EN, I2C, VSEL
TPS628602YCH	0.6 A	1.05 V, 0.9 V, 0.875 V, 0.625 V	1.5 MHz	2x VSEL, EN, PG

## 6 Pin Configuration and Functions



**Figure 6-1. 8-Pin DSBGA YCH Package (Top View)**

**Table 6-1. Pin Functions, TPS628610 and TPS628600**

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	D2	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VOS	D1	IN	Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges $V_{OUT}$ by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace.
VIN	C2	PWR	$V_{IN}$ power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required.
SW	C1	PWR	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
VSEL	B2	IN	Voltage Selection Pin. Can be toggled during operation. LOW = 0.6 V, HIGH = 1.1 V
EN	B1	IN	A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up.
SDA	A2	IN	I <sup>2</sup> C serial data pin. Do not leave floating.
SCL	A1	IN	I <sup>2</sup> C serial clock pin. Do not leave floating.

**Table 6-2. Pin Functions, TPS628601, TPS628602**

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	D2	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VOS	D1	IN	Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges $V_{OUT}$ by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace.
VIN	C2	PWR	$V_{IN}$ power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required.
SW	C1	PWR	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
PG	B2	OUT	Open-drain power-good output
EN	B1	IN	A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up.
VSEL-1	A2	IN	Voltage Selection Pin. Can be toggled during operation.
VSEL-2	A1	IN	Voltage Selection Pin. Can be toggled during operation.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Pin voltage	V <sub>IN</sub>	-0.3	6	V
Pin voltage	SW, DC	-0.3	V <sub>IN</sub> + 0.3 V	V
Pin voltage	SW, transient < 10 ns, while switching	-2.5	9	V
Pin voltage	EN, VSEL, SDA, SCL, PG	-0.3	6	V
Pin voltage	VOS	-0.3	5	V
T <sub>J</sub>	Operating junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input supply voltage range	1.75		5.5	V
V <sub>OUT</sub>	Output voltage range	0.4		1.9875	V
	Pin voltage		SW	5.5	V
	Pin voltage		EN, SDA, SCL, VSEL, PG	5.5	V
I <sub>OUT</sub>	Output current range		TPS628610, V <sub>IN</sub> > 2.3 V	1	A
I <sub>OUT</sub>	Output current range		TPS628610, V <sub>IN</sub> ≤ 2.3 V	0.7	A
I <sub>OUT</sub>	Output current range		TPS628601	0.6	A
I <sub>PG</sub>	Power-good input current capability			1	mA
T <sub>J</sub>	Operating junction temperature	-40		125	°C
C <sub>IN</sub>	Effective input capacitance	2	4.7		μF
L	Effective inductance	0.33	0.47	0.82	μH
CO <sub>UT</sub>	Effective output capacitance	2		26	μF
L	Effective inductance	0.7	1.0	1.2	μH
CO <sub>UT</sub>	Effective output capacitance	3		26	μF

### 7.4 Thermal Information

THERMAL METRIC		YCH (DSBGA)	UNIT
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	121.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	1.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	33.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.7	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	33.5	°C/W

## 7.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{IN} = 3.6\text{ V}$ . Typical values are at  $T_J = 25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$I_{Q(VIN)}$	VIN quiescent current	EN = VIN, $I_{OUT} = 0\ \mu\text{A}$ , $V_{OUT} = 1.2\text{ V}$ device not switching, $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		2.3	4	$\mu\text{A}$
		EN = VIN, $I_{OUT} = 0\ \mu\text{A}$ , $V_{OUT} = 1.2\text{ V}$ , device switching		2.5		$\mu\text{A}$
$I_{SD(VIN)}$	VIN shutdown supply current	EN = GND, shutdown current into VIN VSEL, MODE = GND, $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		120	250	nA
<b>UVLO</b>						
$V_{UVLO(R)}$	VIN UVLO rising threshold	$V_{IN}$ rising		1.65	1.75	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	$V_{IN}$ falling		1.56	1.7	V
$V_{UVLO(H)}$	VIN UVLO hysteresis			100		mV
<b>LOGIC PINS</b>						
$V_{IH}$	High-level input voltage threshold		0.8			V
$V_{IL}$	Low-level input voltage threshold				0.4	V
$I_{LKG}$	Input leakage current into SDA, SCL, VSEL	Pin connected to VIN, $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$		10	25	nA
	EN internal pulldown resistance	EN pin to GND		0.5		M $\Omega$
$I_{LKG}$	Input leakage into EN	Pin connected to VIN, $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$		10	25	nA
<b>VOUT VOLTAGE</b>						
$V_{OUT}$	Output voltage accuracy	PWM mode, no load, $T_J = 25^{\circ}\text{C}$ to $85^{\circ}\text{C}$	-1%		+1%	
$V_{OUT}$	Output voltage accuracy	PWM mode, no load, $T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	-2%		+1.7%	
$I_{VOS(LKG)}$	VOS input leakage current	EN = VIN, $V_{OUT} = 1.2\text{ V}$ (internal 12-M $\Omega$ resistor divider), $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		100	400	nA
<b>SWITCHING FREQUENCY</b>						
$f_{SW(FCCM)}$	Switching frequency, TPS62861x	$V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.2\text{ V}$ , PWM operation		4		MHz
$f_{SW(FCCM)}$	Switching frequency, TPS62860x	$V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.2\text{ V}$ , PWM operation		1.5		MHz
<b>START-UP</b>						
	Internal fixed soft-start time	from $V_{OUT} = 0\text{ V}$ to 95% of $V_{OUT}$ nominal		0.125	0.2	ms
	EN HIGH to start of switching delay			500	1000	$\mu\text{s}$
<b>POWER STAGE</b>						
$R_{DS(ON)(HS)}$	High-side MOSFET on-resistance	$I_{OUT} = 500\text{ mA}$		120	170	m $\Omega$
$R_{DS(ON)(LS)}$	Low-side MOSFET on-resistance	$I_{OUT} = 500\text{ mA}$		80	115	m $\Omega$
<b>OVERCURRENT PROTECTION</b>						
$I_{HS(OC)}$	High-side peak current limit	TPS628610	1.3	1.45	1.55	A
$I_{LS(OC)}$	Low-side valley current limit	TPS628610	1.2	1.35	1.45	A
$I_{HS(OC)}$	High-side peak current limit	TPS628601	0.95	1.1	1.2	A
$I_{LS(OC)}$	Low-side valley current limit	TPS628601	0.85	1.0	1.1	A
$I_{LS(NOC)}$	Low-side negative current limit	Sinking current limit on LS FET				A
<b>POWER GOOD</b>						
$V_{PGTH}$	Power-good threshold	PGOOD low, VOS falling		93%		
$V_{PGTH}$	Power-good threshold	PGOOD high, VOS rising		96%		
$t_{PG:DLY}$	Power-good deglitch delay	PG rising edge		16		$\mu\text{s}$
$I_{PG:LKG}$	Input leakage current into the PG pin	$V_{PG} = 5.0\text{ V}$		10	100	nA
	PG pin output low-level voltage	$I_{PG} = 1\text{ mA}$			400	mV
<b>OUTPUT DISCHARGE</b>						
	Output discharge resistor on the VOS pin	EN = GND, $I_{VOS} = -10\text{ mA}$ into the VOS pin, $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		7	11	$\Omega$
<b>THERMAL SHUTDOWN</b>						
$T_{J(SD)}$	Thermal shutdown threshold <sup>(1)</sup>	Temperature rising, PWM mode		160		$^{\circ}\text{C}$

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{IN} = 3.6\text{ V}$ . Typical values are at  $T_J = 25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{J(HYS)}$	Thermal shutdown hysteresis <sup>(1)</sup>			20		$^{\circ}\text{C}$

(1) Specified by design. Not production tested.

## 7.6 I<sup>2</sup>C Interface Timing Characteristics

PARAMETER <sup>(1)</sup>		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SCL}$	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		Fast mode plus			1	MHz
$t_{BUF}$	Bus free time between a STOP and START condition	Standard mode	4.7			$\mu\text{s}$
		Fast mode	1.3			$\mu\text{s}$
		Fast mode plus	0.5			$\mu\text{s}$
$t_{HD}, t_{STA}$	Hold time (repeated) START condition	Standard mode	4			$\mu\text{s}$
		Fast mode	600			ns
		Fast mode plus	260			ns
$t_{LOW}$	LOW period of the SCL clock	Standard mode	4.7			$\mu\text{s}$
		Fast mode	1.3			$\mu\text{s}$
		Fast mode plus	0.5			$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock	Standard mode	4			$\mu\text{s}$
		Fast mode	600			ns
		Fast mode plus	260			ns
$t_{SU}, t_{STA}$	Setup time for a repeated START condition	Standard mode	4.7			$\mu\text{s}$
		Fast mode	600			ns
		Fast mode plus	260			ns
$t_{SU}, t_{DAT}$	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
		Fast mode plus	50			ns
$t_{HD}, t_{DAT}$	Data hold time	Standard mode	0		3.45	$\mu\text{s}$
		Fast mode	0		0.9	$\mu\text{s}$
		Fast mode plus	0			$\mu\text{s}$
$t_{RCL}$	Rise time of SCL signal	Standard mode			1000	ns
		Fast mode	$20+0.1C_B$		300	ns
		Fast mode plus			120	ns
$t_{RCL1}$	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	Standard mode	$20+0.1C_B$		1000	ns
		Fast mode	$20+0.1C_B$		300	ns
		Fast mode plus			120	ns
$t_{FCL}$	Fall time of SCL signal	Standard mode	$20+0.1C_B$		300	ns
		Fast mode			300	ns
		Fast mode plus			120	ns
$t_{RDA}$	Rise time of SDA signal	Standard mode			1000	ns
		Fast mode	$20+0.1C_B$		300	ns
		Fast mode plus			120	ns

PARAMETER <sup>(1)</sup>		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>FDA</sub>	Fall time of SDA signal	Standard mode			300	ns
		Fast mode	20+0.1C B		300	ns
		Fast mode plus			120	ns
t <sub>SU</sub> , t <sub>STO</sub>	Setup time of STOP condition	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
CB	Capacitive load for SDA and SCL	Standard mode			400	pF
		Fast mode			400	pF
		Fast mode plus			550	pF

(1) All values referred to V<sub>IL</sub> MAX and V<sub>IH</sub> MIN levels in the *Electrical Characteristics* table.

## 7.7 Typical Characteristics

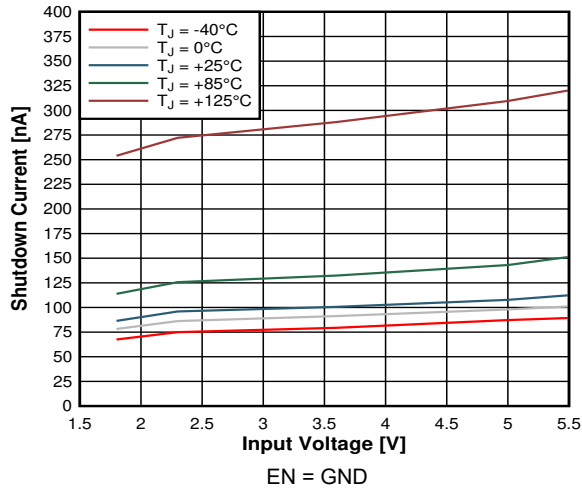


Figure 7-1. Shutdown Current  $I_{SD}$

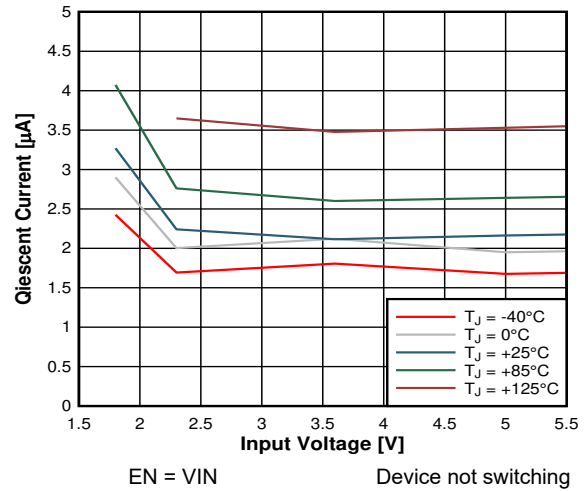


Figure 7-2. Quiescent Current  $I_Q$

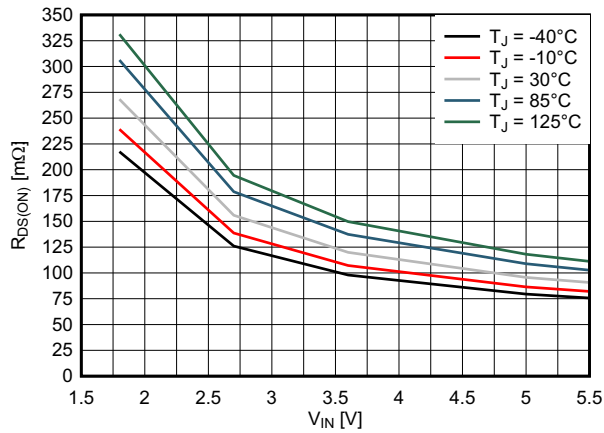


Figure 7-3. High-side Switch Drain Source Resistance  $R_{DS(ON)}$

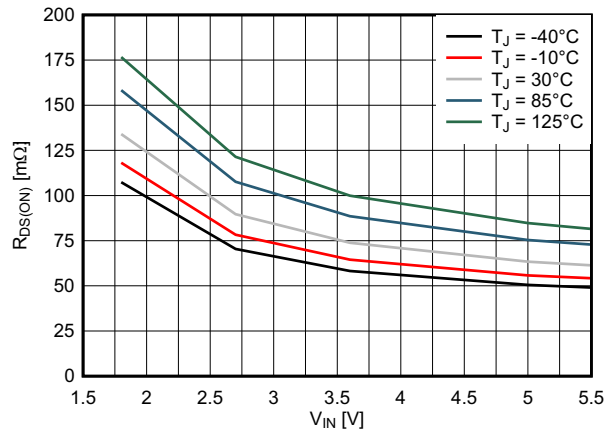


Figure 7-4. Low-side Switch Drain Source Resistance  $R_{DS(ON)}$

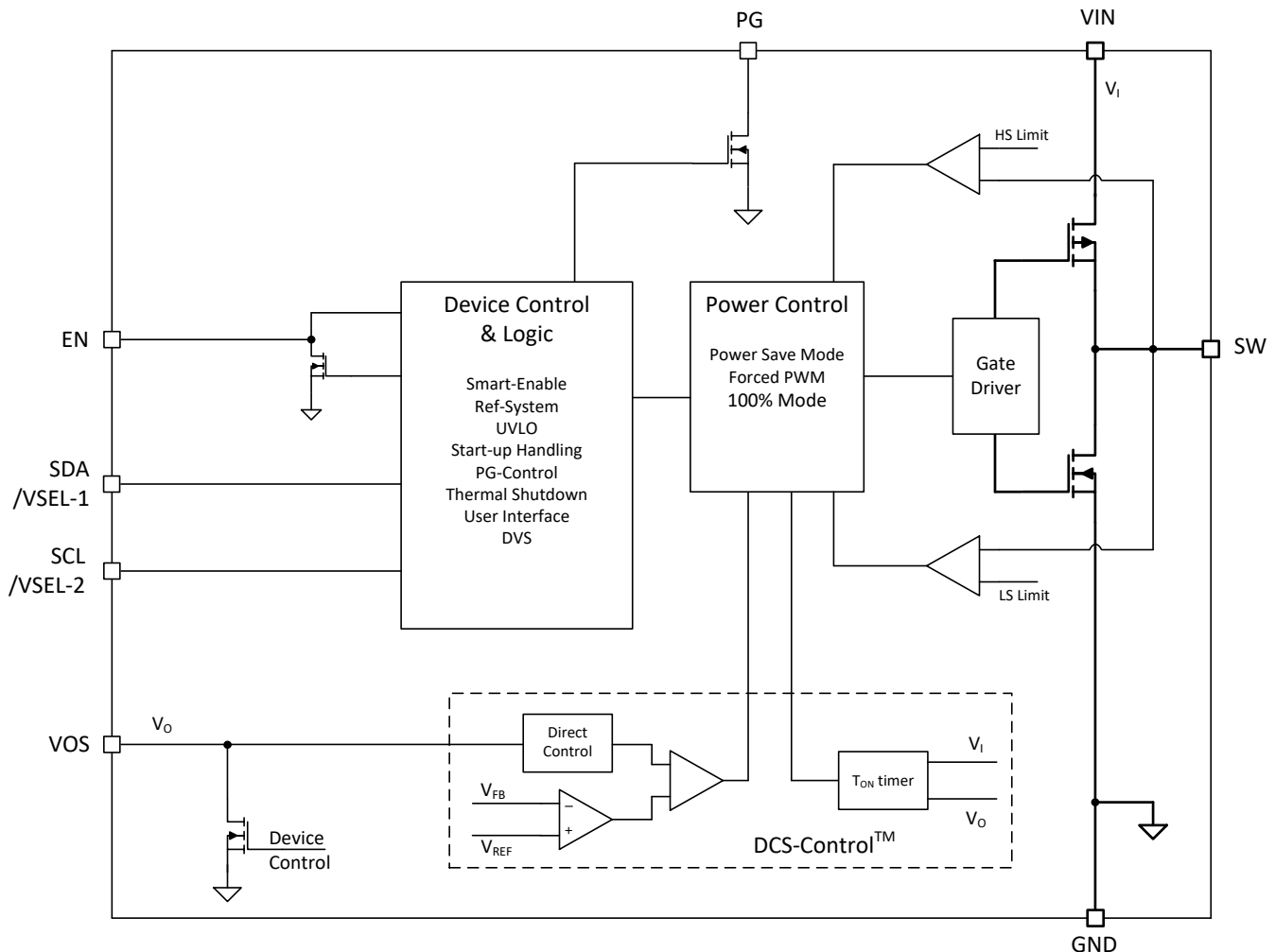


## 8 Detailed Description

### 8.1 Overview

The TPS6286x is a high-frequency synchronous step-down converter with ultra-low quiescent current consumption and flexible output voltage by I<sup>2</sup>C or VSEL interface. Using TI's DCS-Control™ topology, the device extends the high efficiency operation area down to microamperes of load current during Power Save Mode Operation. TI's DCS-Control (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM mode operation. DCS-Control includes an AC loop which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

### 8.2 Functional Block Diagram



**Figure 8-1. Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 Power Save Mode

As the load current decreases, the device enters Power Save Mode (PSM) operation. PSM occurs when the inductor current becomes discontinuous, which is when it reaches 0 A during a switching cycle. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

### 8.3.2 Forced PWM Operation

Through I<sup>2</sup>C, set the device in forced PWM (FPWM) mode by the CONTROL register. The device switches continuously, even with a light load. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications. Efficiency at light load is lower in FPWM mode.

### 8.3.3 Smart Enable and Shutdown (EN)

An internal 500-k $\Omega$  resistor pulls the EN pin to GND and avoids the pin to be floating. This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin once the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

### 8.3.4 Soft Start

Once the device has been enabled with EN high, it initializes and powers up its internal circuits. This occurs during the regulator start-up delay time,  $t_{\text{Delay}}$ . Once  $t_{\text{Delay}}$  expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time,  $t_{\text{Ramp}}$ . See Figure 8-2.

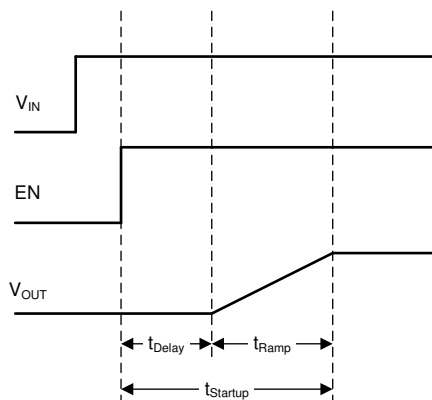


Figure 8-2. Start-up Sequence

### 8.3.5 Output Voltage Selection (VSEL) for TPS62860x

The optional VSEL Interface allows setting the output voltage by a 2-pin HIGH/LOW setting. Using and applying a digital pattern to the "VSEL-1" and "VSEL-2" pins sets the output voltage according to Table 8-1.

Table 8-1. Target Output Voltage Setting by VSEL Interface

VSEL-2	VSEL-1	TPS628601	TPS628602	OPERATION MODE
0	0	0.6 V	1.05 V	PFM Mode
0	1	0.7 V	0.9 V	PFM Mode
1	0	0.8 V	0.875 V	PFM Mode
1	1	1.0 V	0.625 V	PFM Mode

### 8.3.6 Output Voltage Selection (VSEL and I<sup>2</sup>C) for TPS628610

The TPS628610 has two options to select the output voltage.

It can be changed by the VSEL pin. Putting this pin "HIGH" selects the output voltage according to  $V_{OUT}$  register 2. Putting this pin "LOW" selects the voltage according to  $V_{OUT}$  Register 1. The pin can be toggled during operation.

It can also be selected by the value in the  $V_{OUT}$  register that is chosen by VSEL at the moment. The voltage changes right after the I<sup>2</sup>C command is received.

### 8.3.7 Forced PWM Mode During Output Voltage Change

In normal operation, the device does not force PWM operation during VOUT change after VSEL toggle or I<sup>2</sup>C command. For ramping down, this mode provides the remaining energy, stored in the output capacitor to the load of the DC/DC and save battery charge. See [Figure 9-14](#).

Through I<sup>2</sup>C, the device can be set to forced PWM (FPWM) switching during output voltage change. This allows a controlled ramp of  $V_{OUT}$  up and especially down, regardless of the load condition. See [Figure 9-15](#).

This feature follows the internal I<sup>2</sup>C ramp and is only recommended for the setting 1 mV/μs and 0.1 mV/μs. During the faster slopes (10 mV/μs and 5 mV/μs), the mode is likely to be left before the voltage reached the new target value.

### 8.3.8 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7 V (max) with falling VIN. The device starts at an input voltage of 1.8 V (max) rising VIN. Once the device re-enters operation out of an undervoltage lockout condition, it behaves like being enabled.

### 8.3.9 Power Good (PG)

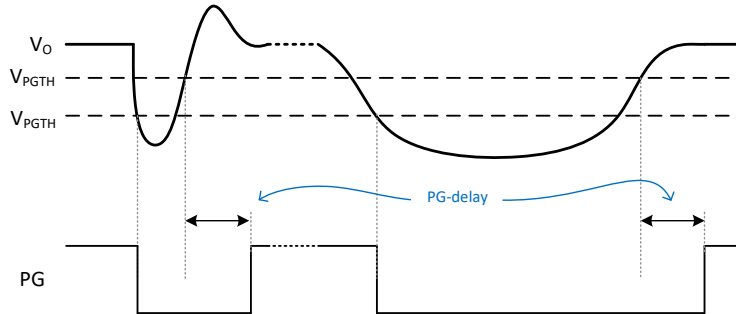
The TPS6286x has a built-in Power-Good (PG) feature to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails or to indicate any overload behavior on the output. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN or thermal shutdown. VIN must remain present for the PG pin to stay LOW. When applying VIN the first time, PG stays HIGH until the first enabling of the device.

If the power-good output is not used, it is recommended to tie to GND or leave open.

**Table 8-2. Power Good Indicator Functional Table**

LOGIC SIGNALS					PG STATUS
$V_I$	EN-PIN	THERMAL SHUTDOWN	$V_O$	DVS TRANSITION ACTIVE	
$V_I > UVLO$	HIGH	NO	$V_O$ on target	NO	High Impedance
			$V_O < target$	YES	LOW
	LOW	YES	x	x	LOW
		x	x	x	LOW
$V_I < UVLO$	x	x	x	x	Undefined

The PG indicator triggers immediately (after internal comparator delay) when  $V_O$  crosses the lower  $V_{PGTH}$  to indicate that the voltage has left the target setting. It features a delay after crossing the upper  $V_{PGTH}$  when going high to make sure  $V_O$  has reached the target again. [Figure 8-3](#) sketches the behavior.



**Figure 8-3. Power Good Transient and De-glitch Behavior**

The PG Indicator is by default pulled low during DVS transition of the output voltage without any blanking or delay time. [Figure 8-3](#) shows an example of this behavior. After  $V_O$  has reached the new target, the PG is again active as shown in [Figure 8-3](#).

### 8.3.10 Switch Current Limit / Short Circuit Protection

The TPS6286x integrates a current limit on the high-side and low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, ILIMF, trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Once the inductor current through the low-side switch decreases below the low-side MOSFET current limit, ILIMF, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

### 8.3.11 Thermal Shutdown

The junction temperature ( $T_J$ ) of the device is monitored by an internal temperature sensor. If  $T_J$  exceeds the thermal shutdown temperature TSD of 160°C (typ), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When  $T_J$  decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set VOUT. The thermal shutdown is not active in Power Save Mode.

### 8.3.12 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge feature is only active once the device has been enabled at least once since the supply voltage was applied. The output discharge function is not active if the device is disabled and the supply voltage is applied the first time. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is  $V_I > V_{TH\_UVLO}$ .

## 8.4 Programming

### 8.4.1 Serial Interface Description

I<sup>2</sup>C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see I<sup>2</sup>C-Bus Specification, Version .6, 2014). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I<sup>2</sup>C-compatible devices connect to the I<sup>2</sup>C bus through open-drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives, transmits data, or both on the bus under control of the master device.

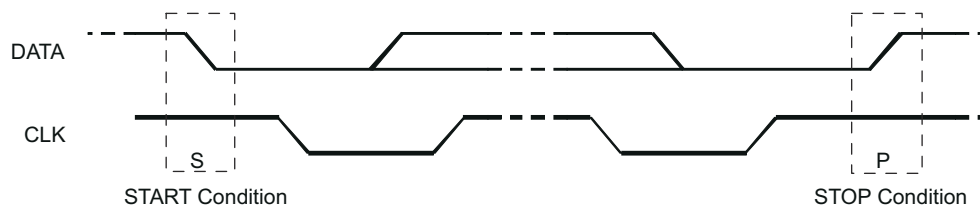
The device works as a *slave* and supports the following data transfer *modes*, as defined in the I<sup>2</sup>C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.8 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different and must not be used.

It is recommended that the I<sup>2</sup>C master initiates a STOP condition on the I<sup>2</sup>C bus after the initial power up of SDA and SCL pullup voltages to ensure reset of the I<sup>2</sup>C engine.

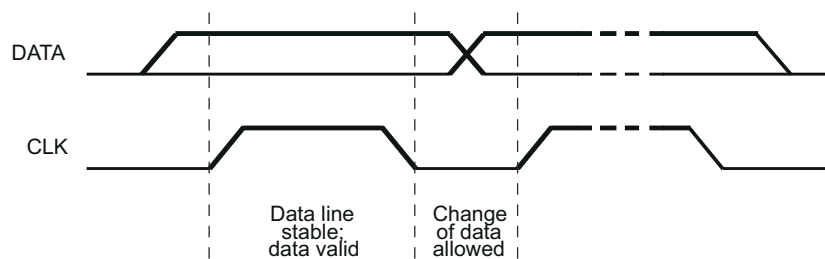
### 8.4.2 Standard- and Fast-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 8-4. All I<sup>2</sup>C-compatible devices recognize a start condition.



**Figure 8-4. START and STOP Conditions**

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 8-5). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 8-6) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.



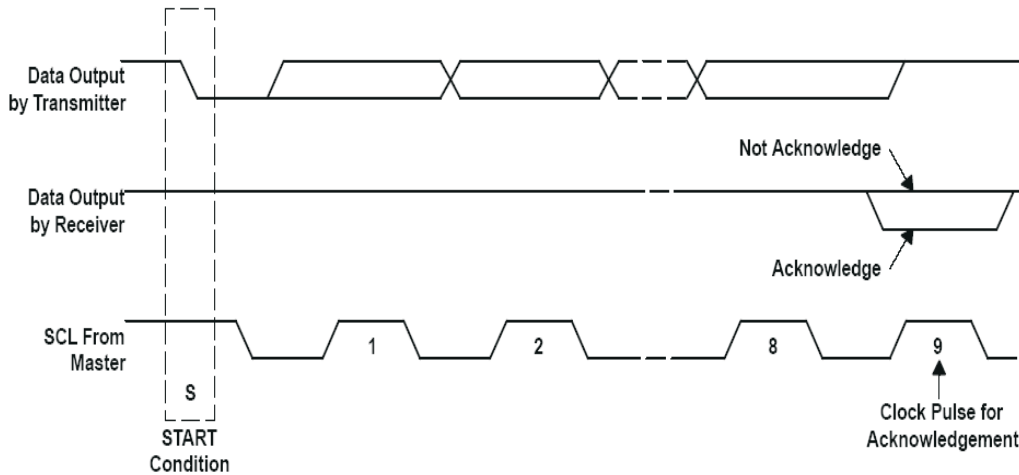
**Figure 8-5. Bit Transfer on the Serial Interface**

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An

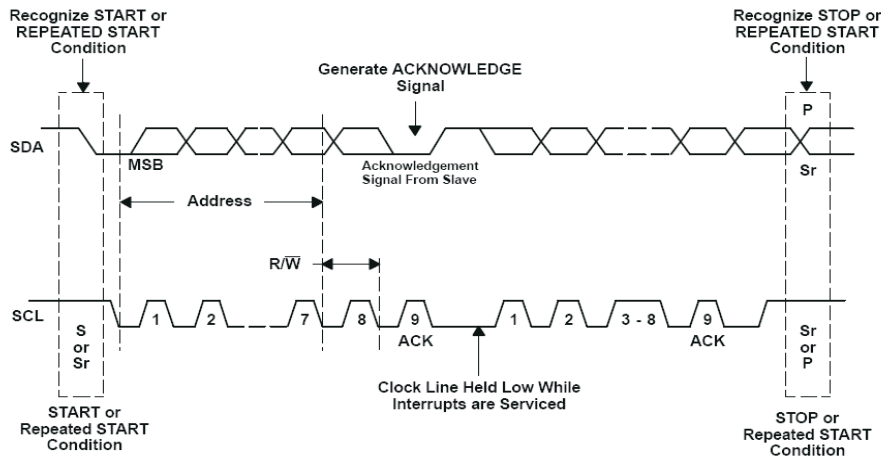
acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 8-4). This releases the bus and stops the communication link with the addressed slave. All I<sup>2</sup>C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.



**Figure 8-6. Acknowledge on the I<sup>2</sup>C Bus**



**Figure 8-7. Bus Protocol**

### 8.4.3 I<sup>2</sup>C Update Sequence

The requires the following:

- A start condition
- A valid I<sup>2</sup>C address
- A register address byte
- A data byte for a single update

After the receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the device. The device performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

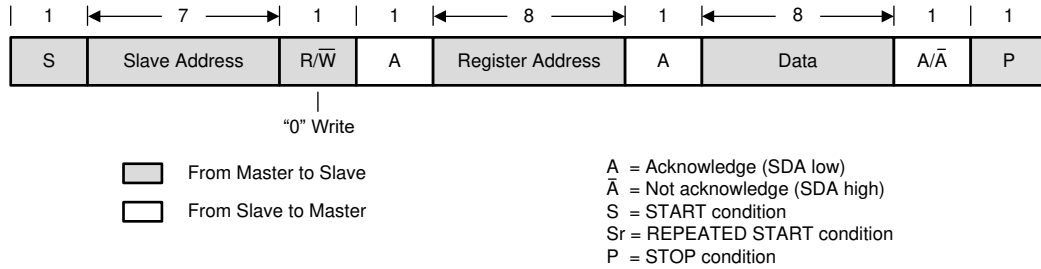


Figure 8-8. "Write" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

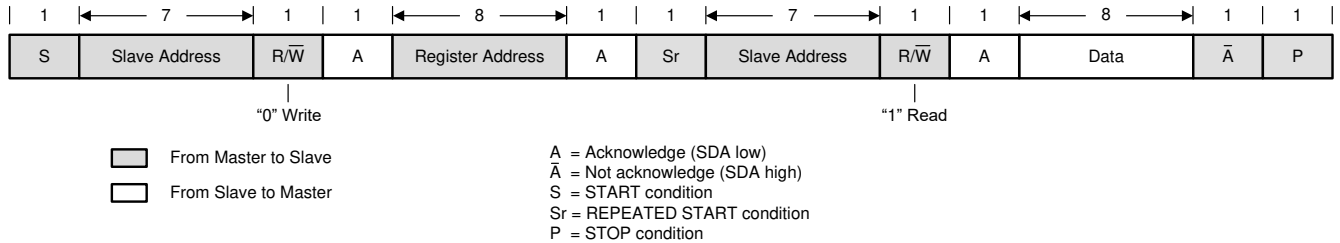


Figure 8-9. "Read" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

#### 8.4.4 I<sup>2</sup>C Register Reset

The I<sup>2</sup>C registers can be reset by the following:

- Pull the input voltage below 1.8 V (typ).
- A high to low transition on EN. The previous value of the "Enable Output Discharge" bit is latched until the next EN rising edge or pulling the input voltage below 1.0 V (typ).
- Set the Reset bit in the CONTROL register. When Reset is set to 1, all registers are reset to the default values and a new start-up begins immediately. After  $t_{Delay}$ , the I<sup>2</sup>C registers can be programmed again.

## 8.5 Register Map

**Table 8-3. Register Map**

REGISTER ADDRESS (HEX)	REGISTER NAME	FACTORY DEFAULT (HEX)	DESCRIPTION
0x01	V <sub>OUT</sub> Register 1	0x10	Sets the target output voltage
0x02	V <sub>OUT</sub> Register 2	0x38	Sets the target output voltage
0x03	CONTROL Register		Sets miscellaneous configuration bits
0x05	STATUS Register	0x00	Returns status flags, cleared on read-out

### 8.5.1 Slave Address Byte

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	R/W

The slave address byte is the first byte received following the START condition from the master device. The 7-bit slave address is 0x40 and internally set.

### 8.5.2 Register Address Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	D2	D1	D0

Following the successful acknowledgment of the slave address, the bus master sends a byte to the device, which contains the address of the register to be accessed.

### 8.5.3 V<sub>OUT</sub> Register 1

**Table 8-4. V<sub>OUT</sub> Register 1 Description**

REGISTER ADDRESS 0x01 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYP) <a href="#">Section 8.5.3</a>
6:0	VO1_SET	0x00	0.400 V
		0x01	0.4125 V
		...	
		0x10	<b>0.600 V</b> (default value)
		...	
		0x7E	1.975 V
		0x7F	1.9875 V



### 8.5.4 V<sub>OUT</sub> Register 2

**Table 8-5. V<sub>OUT</sub> Register 2 Description**

REGISTER ADDRESS 0X02 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYP) <sup>Section 8.5.4</sup>
7	Operation Mode	0x00	0 - Keep PFM/PWM selection as in CONTROL-Register 1 - sets the device in PWM operation for this Voltage selection
6:0	VO2_SET	0x00	0.400 V
		0x01	0.4125 V
		...	
		0x38	<b>1.10 V</b> (default value)
		...	
		0x7E	1.975 V
		0x7F	1.9875 V

### 8.5.5 CONTROL Register

**Table 8-6. CONTROL Register Description**

REGISTER ADDRESS 0X03 READ/WRITE				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	Reset	W	0	1 - Reset all registers to default. This bit triggers a shutdown followed by a re-reading of the internal OTP settings and a new soft start.
6	Enable FPWM Mode during Output Voltage Change	R/W	1	0 - Keep the current mode status during output voltage change. 1 - Force the device in FPWM during output voltage change.
5	Software Enable Device	R/W	1	0 - Disable the device. All registers values are still kept. 1 - Re-enable the device with a new start-up without the t <sub>Delay</sub> period.
4	Enable FPWM Mode	R/W	0	0 - Set the device in power save mode at light loads. 1 - Set the device in forced PWM mode at light loads.
3	Enable Output Discharge	R/W	1	0 - Disable output discharge. 1 - Enable output discharge. This setting is used for the next disable cycle (Software or Hardware).
2	Reserved			
0:1	Voltage Ramp Speed	R/W	11	00 - 10mV/μs 01 - 5 mV/μs 10 - 1 mV/μs 11 - 0.1 mV/μs

### 8.5.6 STATUS Register

**Table 8-7. STATUS Register Description**

REGISTER ADDRESS 0X05 READ ONLY <sup>(1)</sup>				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	Reserved			
4	Thermal Shutdown Tripped	R	0	1: Thermal Shutdown has tripped since the last reading. 0: No Thermal Shutdown event occurred during the last reading.
3	Reserved			
2	Power Bad	R	0	1: Output voltage is or was below 0.95xV <sub>O</sub> 0: No Power Bad event occurred since last reading

**Table 8-7. STATUS Register Description (continued)**

REGISTER ADDRESS 0X05 READ ONLY <sup>(1)</sup>				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
1:0	Reserved			

- (1) All bit values are latched until the device is reset, or the STATUS register is read. Then, the STATUS register is reset to its default values.

## 9 Application and Implementation

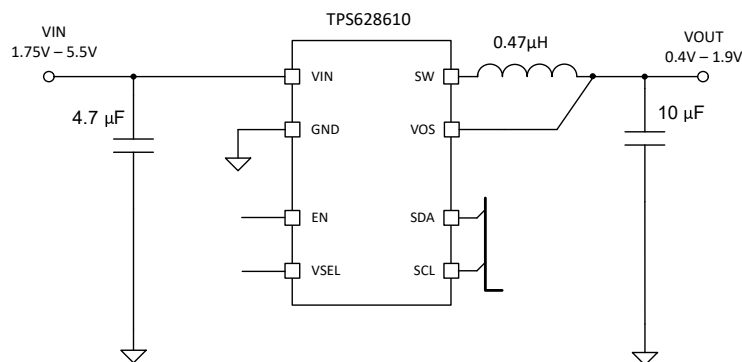
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

### 9.2 Typical Application, TPS628610



**Figure 9-1. TPS628610, Typical Application**

#### 9.2.1 Design Requirements

Table 9-1 shows the list of components for the application circuit and the characteristic application curves.

**Table 9-1. Components for Application Characteristic Curves**

REFERENCE	DESCRIPTION	VALUE	SIZE [L x W x T]	MANUFACTURER <sup>(1)</sup>
TPS628610	Step down converter, 1 A		1.4 mm x 0.70 mm x 0.4 mm max.	Texas Instruments
C <sub>IN</sub>	Ceramic capacitor, GRM155R60J475ME47D	4.7 µF	0402 (1 mm x 0.5 mm x 0.6 mm max.)	Murata
C <sub>OUT</sub>	Ceramic capacitor, GRM155R60J106ME15D	10 µF	0402 (1 mm x 0.5 mm x 0.65 mm max.)	Murata
L	Inductor DFE18SANR47MG0L	0.47 µH	0603 (1.6 mm x 0.8 mm x 1.0 mm max.)	Murata

(1) See [Third-party Products Disclaimer](#).

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Inductor Selection

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple, and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current ( $\Delta I_L$ ) decreases with higher inductance and increases with higher  $V_{IN}$  or  $V_{OUT}$  and can be estimated according to [Equation 1](#).

[Equation 2](#) calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current, as calculated with [Equation 2](#). This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high side MOSFET switch current limit,  $I_{LIMF}$ .

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- $f$  = Switching frequency
- $L$  = Inductor value
- $\Delta I_L$  = Peak-to-peak inductor ripple current
- $I_{Lmax}$  = Maximum inductor current

[Table 9-2](#) shows a list of possible inductors.

**Table 9-2. List of Possible Inductors**

INDUCTANCE [μH]	INDUCTOR SERIES	SIZE IMPERIAL (METRIC)	DIMENSIONS L x W x T	SUPPLIER <sup>(1)</sup>
0.47	DFE18SAN_G0	0603 (1608)	1.6mm x 0.8mm x 1.0mm max	Murata
0.47	HTEB16080F	0603 (1608)	1.6mm x 0.8mm x 0.6mm max.	Cyntec
0.47	HTET1005FE	0402 (1005)	1.0mm x 0.5mm x 0.65mm max.	Cyntec
0.47	TFM160808ALC	0603 (1608)	1.6mm x 0.8mm x 0.8mm max.	TDK

(1) See [Third-party Products Disclaimer](#)

### 9.2.2.2 Output Capacitor Selection

The DCS-Control™ scheme of the TPS6286x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple.

The inductor and output capacitor together provide a low-pass filter. To simplify this process, [Table 9-3](#) outlines possible inductor and capacitor value combinations.

**Table 9-3. Recommended LC Output Filter Combinations**

DEVICE	NOMINAL INDUCTOR VALUE [μH]	NOMINAL OUTPUT CAPACITOR VALUE [μF]			
		4.7 μF	10 μF	2 x 10 μF	22 μF
TPS628610	0.47 <sup>(1)</sup>	√	√ <sup>(3)</sup>	√	√
TPS62860x	1.0 <sup>(2)</sup>	√	√ <sup>(3)</sup>	√	√

- (1) An effective inductance range of 0.33 μH to 0.82 μH is recommended. An effective capacitance range of 2 μF to 26 μF is recommended.
- (2) An effective inductance range of 0.7 μH to 1.2 μH is recommended. An effective capacitance range of 3 μF to 26 μF is recommended.
- (3) Typical application configuration. Other check marks indicate alternative filter combinations.

### 9.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR ceramic input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications, a 4.7-μF input capacitor is sufficient. When operating from a high impedance source, like a coin cell, a larger input buffer capacitor ≥10 μF is recommended to avoid voltage drops during start-up and load transients. The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall current consumption.

Table 9-4 shows a selection of input and output capacitors.

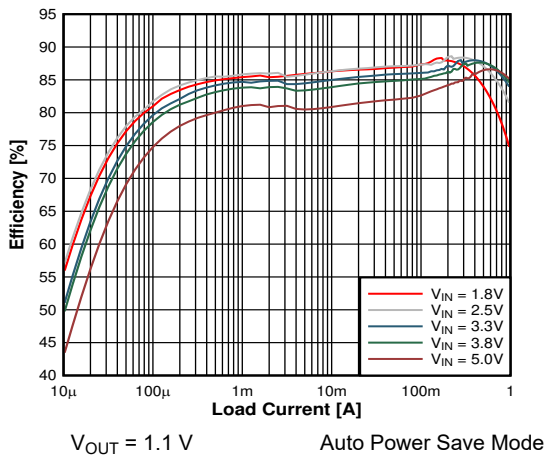
**Table 9-4. List of Possible Capacitors** [Section 9.2.2.3](#)

CAPACITANCE [μF]	CAPACITOR PART NUMBER	SIZE IMPERIAL (METRIC)	DIMENSIONS L x W x T	SUPPLIER <sup>(1)</sup>
4.7	GRM155R60J475ME47D	0402 (1005)	1.0mm x 0.5mm x 0.6mm max.	Murata
4.7	GRM035R60J475ME15	0201 (0603)	0.6mm x 0.3mm x 0.55mm max	Murata
10	GRM155R60J106ME15D	0402 (1005)	1.0mm x 0.5mm x 0.65mm max.	Murata

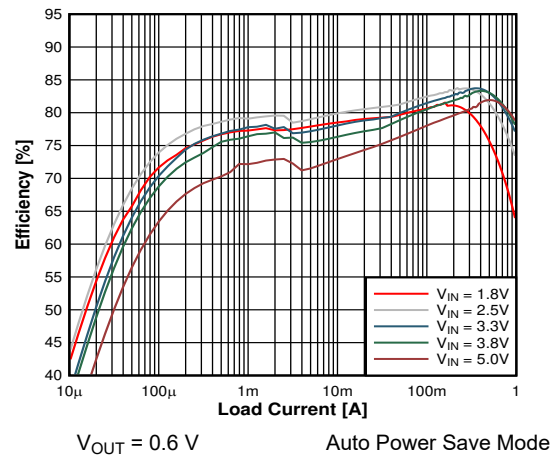
- (1) See [Third-party Products Disclaimer](#)

### 9.2.3 Application Curves

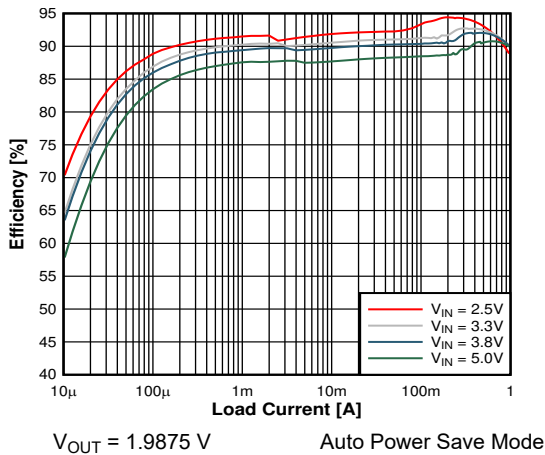
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 1.1\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , BOM = [Table 9-1](#), unless otherwise noted



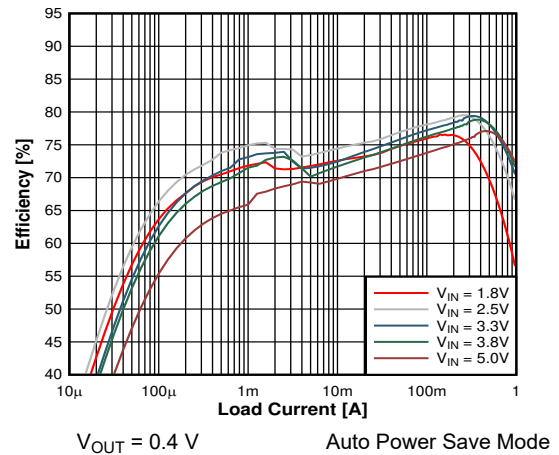
**Figure 9-2. Efficiency**



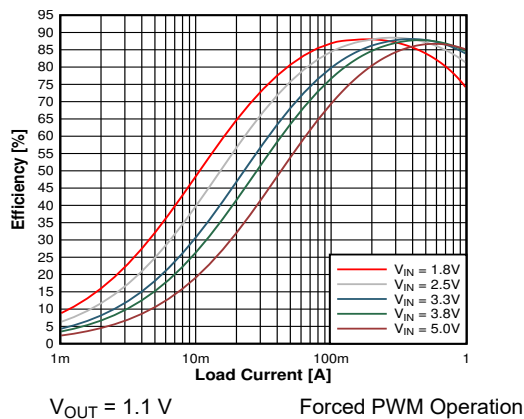
**Figure 9-3. Efficiency**



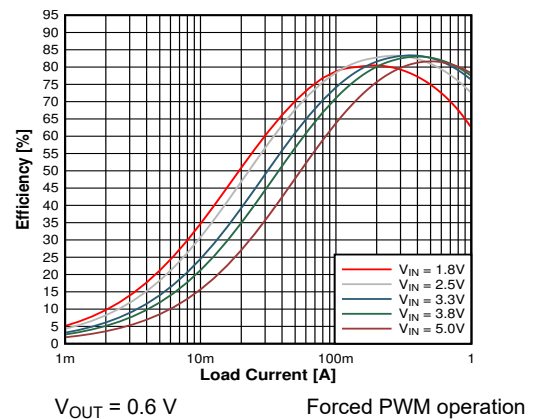
**Figure 9-4. Efficiency**



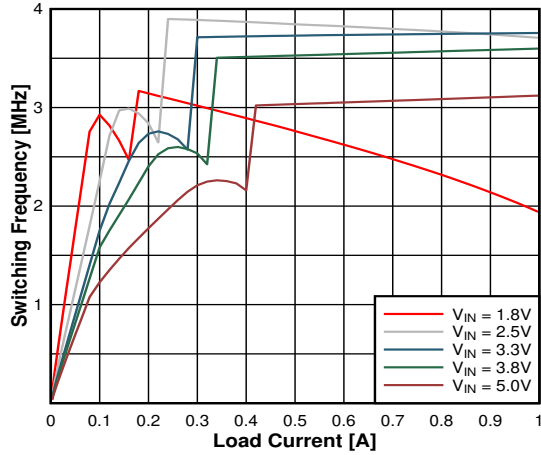
**Figure 9-5. Efficiency**



**Figure 9-6. Efficiency, Inductor Comparison**

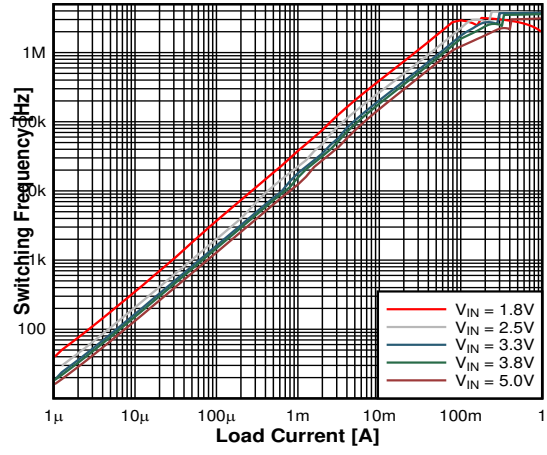


**Figure 9-7. Efficiency**



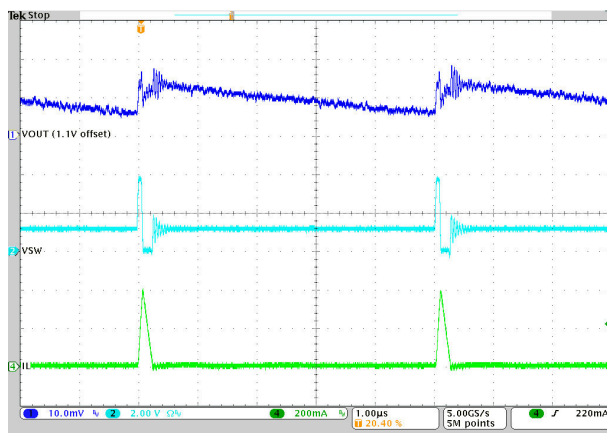
$V_{OUT} = 1.1\text{ V}$  Auto Power Save Mode

**Figure 9-8. Switching Frequency**



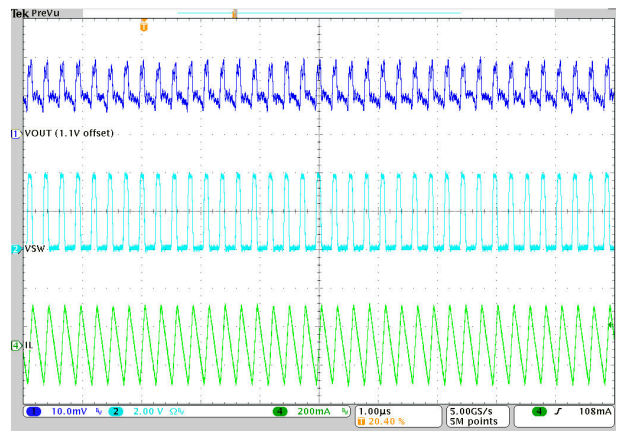
$V_{OUT} = 1.1\text{ V}$

**Figure 9-9. Switching Frequency**



VSEL = HIGH

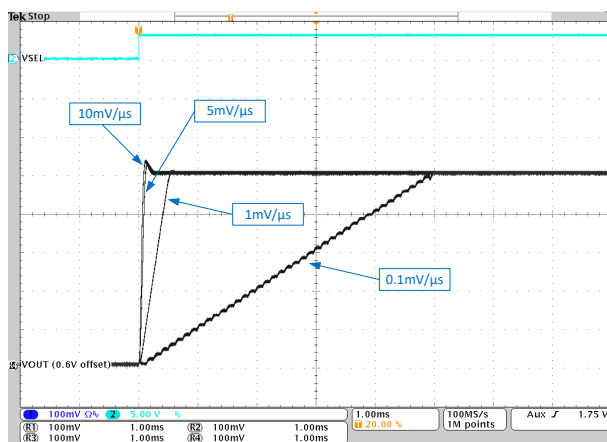
**Figure 9-10. PFM Mode Operation**



$I_{OUT} = 500\text{ mA}$

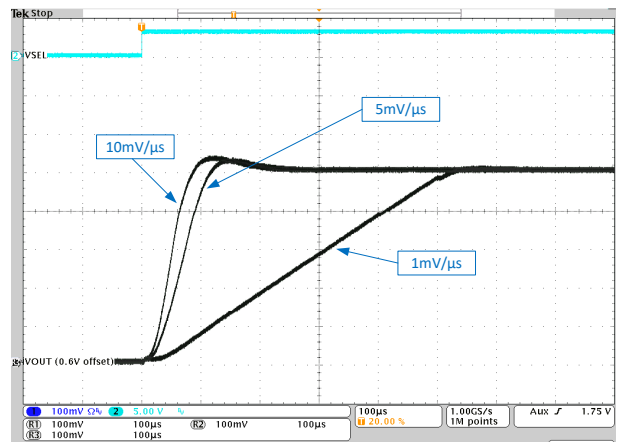
VSEL = HIGH

**Figure 9-11. PWM-Mode Operation**



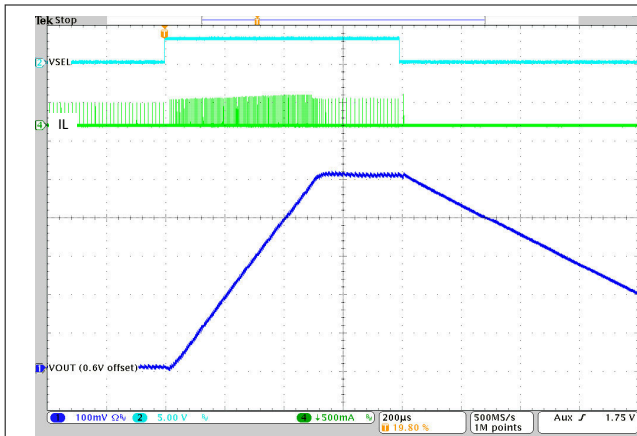
Default voltage setting

**Figure 9-12. DVS by VSEL, Different Ramp Speed Settings**



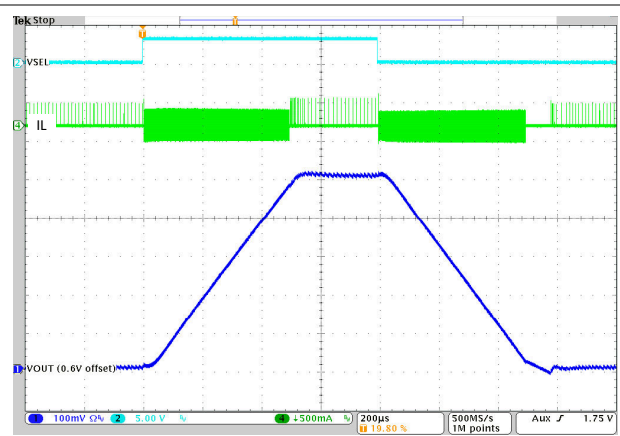
Default voltage setting

**Figure 9-13. DVS by VSEL, Different Ramp Speed Settings**



Power Save Mode is active

**Figure 9-14. Standard Operation:  $V_{OUT}$  Change**

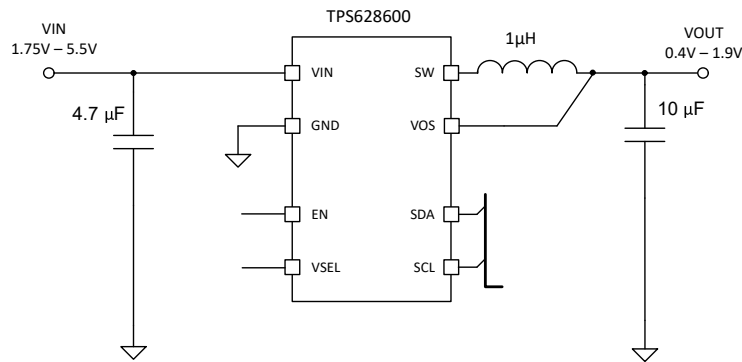


Power Save Mode is active

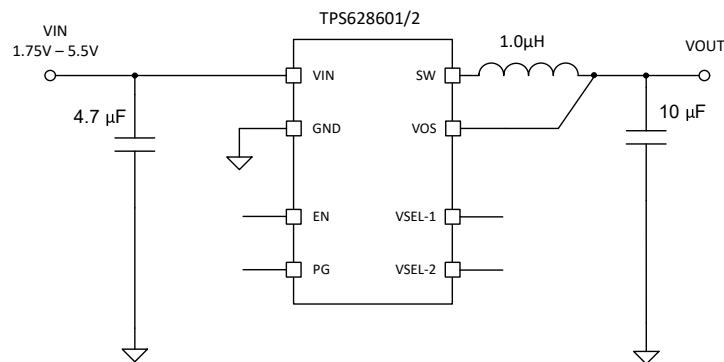
**Figure 9-15. FPWM-Mode During  $V_{OUT}$  Change Enabled**



### 9.2.4 Typical Application, TPS628600, TPS62860x



**Figure 9-16. TPS628600, Typical Application**



**Figure 9-17. TPS62860x, Typical Application**

#### 9.2.4.1 Design Requirements

Table 9-5 shows the list of components for the application circuit and the characteristic application curves.

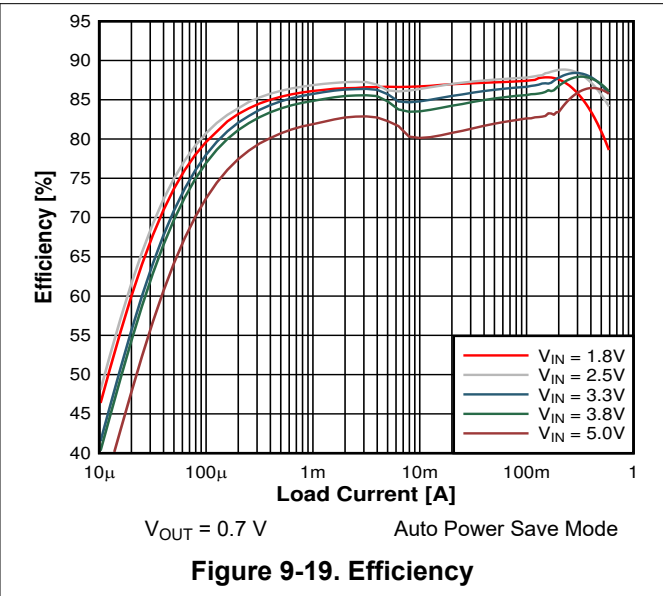
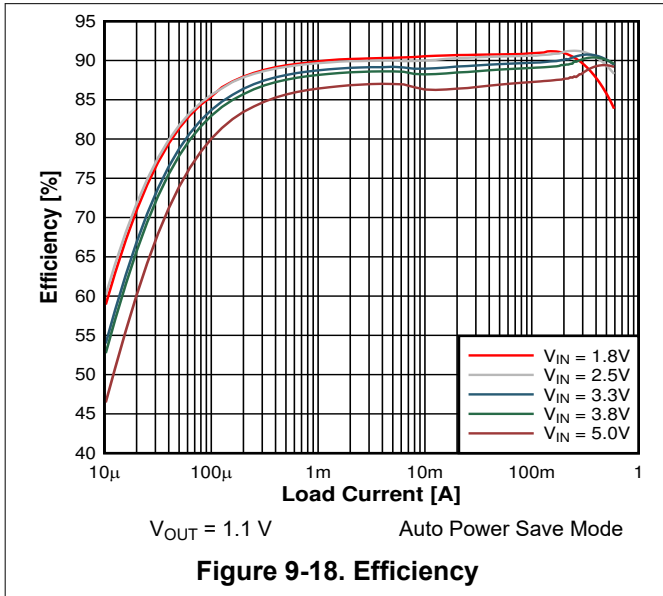
**Table 9-5. Components for Application Characteristic Curves**

REFERENCE	DESCRIPTION	VALUE	SIZE [L x W X T]	MANUFACTURER <sup>(1)</sup>
TPS628610	Step down converter, 1 A		1.4 mm x 0.70 mm x 0.4 mm max.	Texas Instruments
C <sub>IN</sub>	Ceramic capacitor, GRM155R60J475ME47D	4.7 μF	0402 (1 mm x 0.5 mm x 0.6 mm max.)	Murata
C <sub>OUT</sub>	Ceramic capacitor, GRM155R60J106ME15D	10 μF	0402 (1 mm x 0.5 mm x 0.65 mm max.)	Murata
L	Inductor DFE201610E	1 μH	0805 (2.0 mm x 1.6 mm x 1.0 mm max.)	Murata

#### 9.2.4.2 Detailed Design Procedure

See Section 9.2.2.

**9.2.4.3 Application Curves**



## 10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS6286x.

## 11 Layout

### 11.1 Layout Guidelines

The pinout of TPS6286x has been optimized to enable a single top layer PCB routing of the IC and its critical passive components such as  $C_{IN}$ ,  $C_{OUT}$ , and  $L$ . Furthermore, this pin out allows you to connect tiny components such as 0201 (0603) size capacitors and 0402 (1005) size inductor. A solution size smaller than 5 mm<sup>2</sup> can be achieved with a fixed output voltage.

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor must be placed as close as possible to the VIN and GND pins of the IC. This is the most critical component placement.
- The VOS line is a sensitive, high impedance line and must be connected to the output capacitor and routed away from noisy components and traces (for example, SW line) or other noise sources.

### 11.2 Layout Example

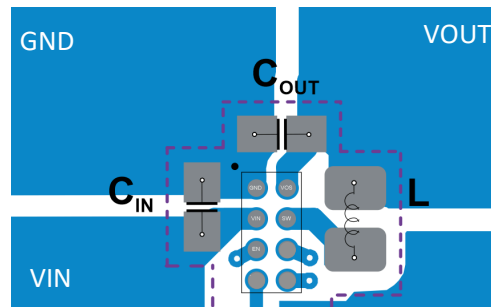


Figure 11-1. PCB Layout Example

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

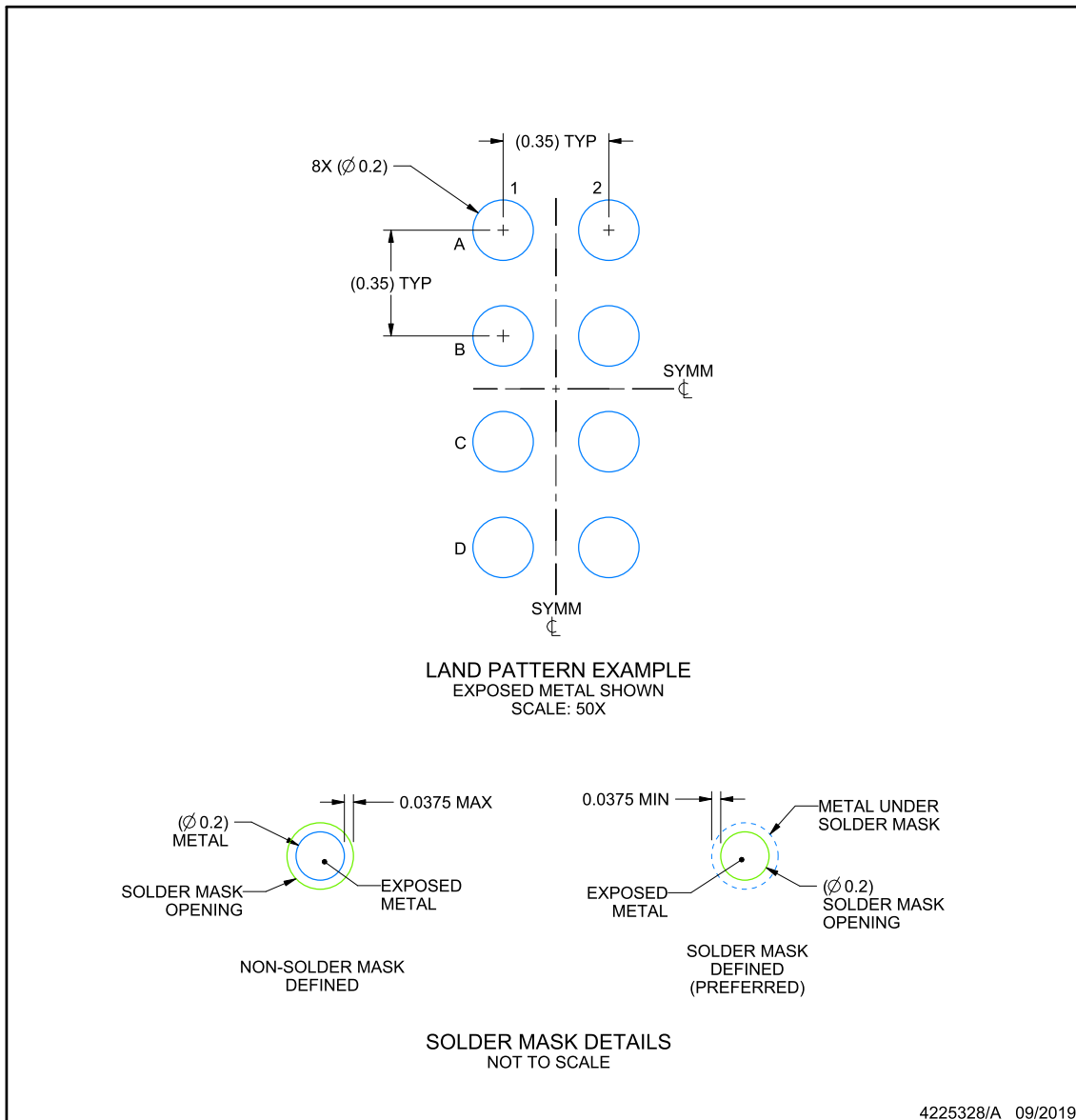


## EXAMPLE BOARD LAYOUT

**YCH0008**

**DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

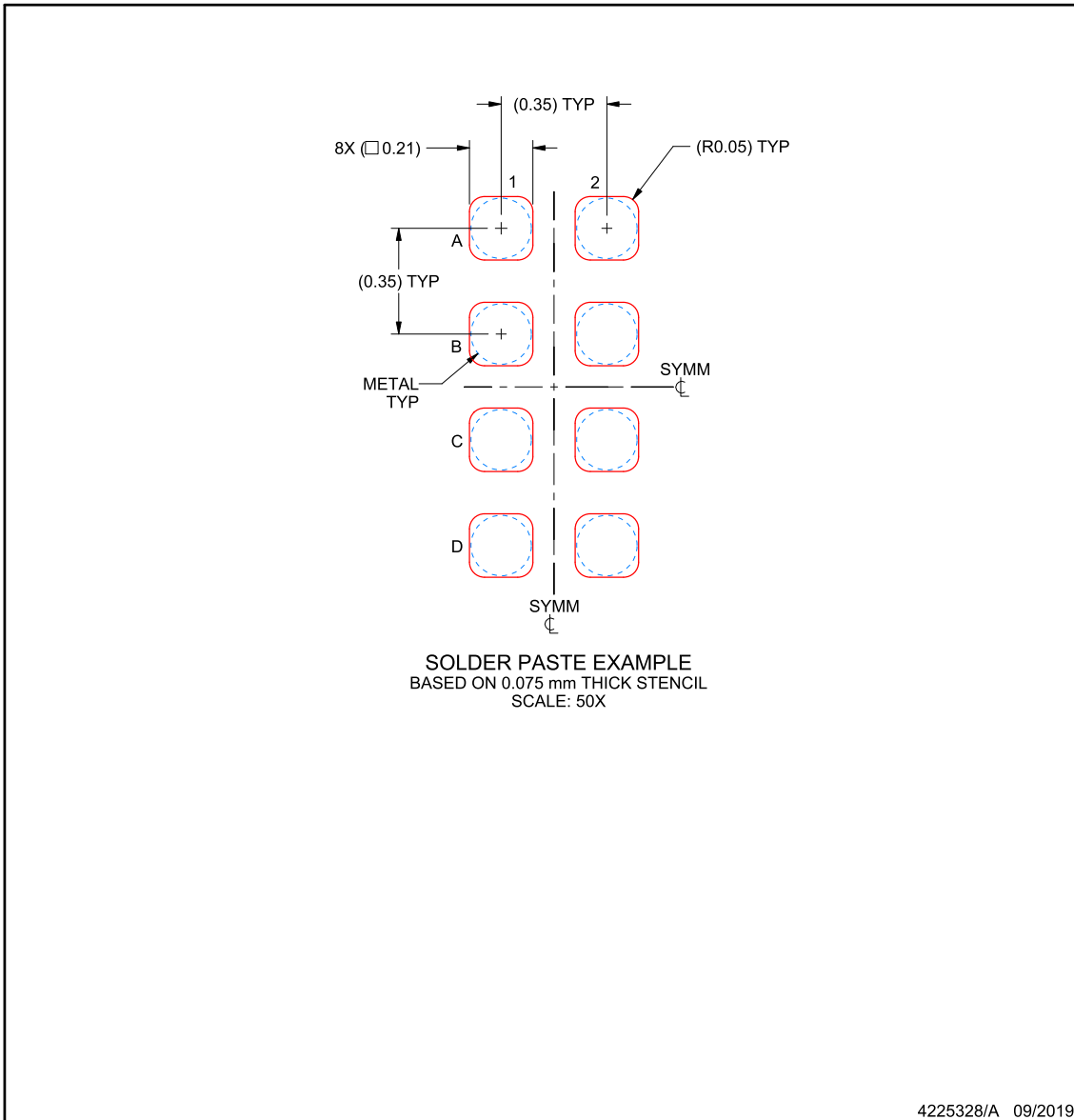


**EXAMPLE STENCIL DESIGN**

**YCH0008**

**DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS628600YCHR	ACTIVE	DSBGA	YCH	8	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	<a href="#">Samples</a>
TPS628601YCHR	ACTIVE	DSBGA	YCH	8	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	<a href="#">Samples</a>
TPS628610YCHR	ACTIVE	DSBGA	YCH	8	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628600YCHR	DSBGA	YCH	8	12000	180.0	8.4	0.8	1.5	0.47	2.0	8.0	Q1
TPS628601YCHR	DSBGA	YCH	8	12000	180.0	8.4	0.8	1.5	0.47	2.0	8.0	Q1
TPS628610YCHR	DSBGA	YCH	8	12000	180.0	8.4	0.8	1.5	0.47	2.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS628600YCHR	DSBGA	YCH	8	12000	182.0	182.0	20.0
TPS628601YCHR	DSBGA	YCH	8	12000	182.0	182.0	20.0
TPS628610YCHR	DSBGA	YCH	8	12000	182.0	182.0	20.0

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