Click **here** to ask an associate for production status of specific part numbers.

MAX25223

Automotive 36V 3.5A Buck Converter with 5μA I_Q

General Description

The MAX25223 is a small, automotive grade synchronous buck converter with integrated high-side and low-side switches. The device is designed to deliver up to 3.5A with input voltages from +3V to +36V while using only 5μA quiescent current at no load. The MAX25223 provides an accurate output voltage of ±2% within the normal operation input range of +6V to +18V. With 65ns minimum on-time capability, the converter is capable of large input-to-output conversion ratios. Voltage quality can be monitored by observing the PGOOD signal. MAX25223 can operate in drop-out by running at 99% duty cycle, making it ideal for automotive and industrial applications. The IC offers standard parts with fixed output voltages of 3.3V and 5V. Other fixed output voltages in the range of 3V to 5.5V are also available on request. Frequency is internally fixed at 2.1MHz, which allows for small external components, reduces output ripple, and guarantees that there is no AM interference. A 400kHz option is also offered to provide minimum switching losses and maximum efficiency. MAX25223 automatically enters skip mode at light loads with ultra-low quiescent current of 5μA at no load. It offers pin-enabled spread-spectrum frequency modulation designed to minimize EMI-radiated emissions due to the modulation frequency.

The MAX25223 comes in a small 4mm x 4mm 20-pin SW-TQFN package and uses very few external components. The intelligent package layout results in an extremely low-noise solution with superior EMI performance.

Applications

- Automotive
- Industrial
- High Voltage DC-DC Converters

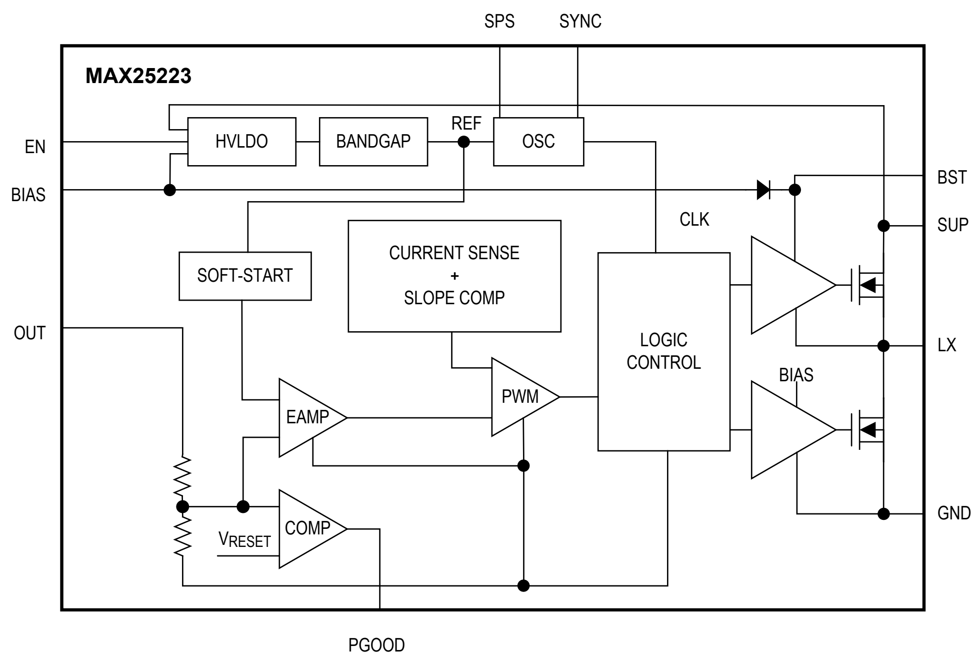
Benefits and Features

- Synchronous DC-DC Converter with Integrated FETs
  - 3.5A Output-Current Capability
  - 5μA Quiescent Current in Standby Mode
- Small Solution Size Saves Space
  - 65ns Minimum On-Time
  - 2.1MHz or 400kHz Fixed Operating Frequency Options
  - Fixed 5V / 3.3V V_{OUT} Options Available
  - Fixed 3.5ms Internal Soft-Start
  - Innovative Current-Mode-Control Architecture Minimizes Total Board Space and BOM Count
- PGOOD Output and High-Voltage EN Input Simplify Power Sequencing
  - OV/UV Monitoring on PGOOD with High Accuracy
  - Fully Programmable UVLO with Precise ENABLE Threshold
- Protection Features and Operating Range Ideal for Automotive Applications
  - 3V to 36V Operating V_{IN} Range
  - 42V Load-Dump Protection
  - Thermal Shutdown, Short Circuit Protection with Hiccup Mode and Output Overvoltage Protection
  - 99% Duty-Cycle Operation with Low Dropout
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100 Qualified

Ordering Information appears at end of data sheet.

19-101165; Rev 0; 9/21

Simplified Block Diagram



Absolute Maximum Ratings

SUP .... -0.3V to +42V
EN .... -0.3V to +42V
BST to LX .... +6V
BST .... -0.3V to +47V
FB .... -0.3V to V_{BIAS} + 0.3V
SYNC .... -0.3V to V_{BIAS} + 0.3V
SPS .... -0.3V to V_{BIAS} + 0.3V
OUT .... -0.3V to +6.0V
PGOOD .... -0.3V to +6.0V
PGND to AGND .... -0.3V to +0.3V
BIAS .... -0.3V to +6.0V

OUT Short-Circuit Duration .... Continuous
ESD Protection
Human Body Model .... ±2kV
Continuous Power Dissipation (TA = +70°C)
20-L SW TQFN (Derate 30.3 mW/°C above +70°C) 2424.2mW
Operating Ambient Temperature Range .... -40°C to +125°C
Operating Junction Temperature (Note 2) .... -40°C to +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10s) .... +300°C
Soldering Temperature (Reflow) .... +260ºC

Note 1: LX has internal clamp diodes to PGND/AGND and SUP. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J= +150°C for 5,000 hours.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to +125	°C

Note: These limits are not guaranteed.

Package Information

20-Lead Side-Wettable TQFN Package

Package Code	T2044Y+5C
Outline Number	21-100318
Land Pattern Number	90-0409
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	48
Junction to Case (θ_{JC})	2
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	33
Junction to Case (θ_{JC})	2

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, V_{SYNC} = 0V, T_J = -40°C to +150°C unless otherwise noted, V_{OUT} = 5V, (Notes 3 and 4))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}			3.5		36	V
		After start-up		3.0		36	
	V_{SUP_MAX}	t < 1s				42	
Supply Current	I_{SUP_OFF}	V_{EN} = Low			1	5	μA
	$I_{SUP, 3.3V}$	Fixed V_{OUT} (internal) = 3.3V, f_{SW} = 2.1MHz/400kHz, no load, no switching			5	10	μA
	$I_{SUP\_SW, 3.3V}$	Fixed V_{OUT} (internal) = 3.3V, f_{SW} = 2.1MHz/400kHz, no load, switching (Note 4)			6		
	$I_{SUP, 5V}$	Fixed V_{OUT} (internal) = 5V, f_{SW} = 2.1MHz/400kHz, no load, no switching			8.5	13	μA
	$I_{SUP\_SW, 5V}$	Fixed V_{OUT} (internal) = 5V, f_{SW} = 2.1MHz/400kHz, no load, switching (Note 4)			10		μA
LX Leakage	$I_{LX, leak}$	V_{SUP} = 36V, LX = 0V or 40V, T_A = +25°C		-1		+1	μA
UV Lockout	UVLO	V_{BIAS} rising		2.525	2.725	2.925	V
	$UVLO_{HYS}$	Hysteresis			0.13		
BIAS Voltage	V_{BIAS}	+5.5V ≤ V_{SUP} ≤ +36V, FPWM mode			5		V
Buck Converter							
Voltage Accuracy	$V_{OUT,5V}$	Fixed V_{OUT} (internal) = 5V, f_{SW} = 2.1MHz/400kHz	Skip mode (Note 4)	4.85	5	5.06	V
			PWM mode	4.93	5	5.07	
	$V_{OUT,3.3V}$	Fixed V_{OUT} (internal) = 3.3V, f_{SW} = 2.1MHz/400kHz	Skip mode (Note 4)	3.2	3.3	3.37	
		Fixed V_{OUT} (internal) = 3.3V, f_{SW} = 2.1MHz/400kHz	PWM mode	3.25	3.3	3.35	
Output Voltage Range	V_{OUT}			3		5.5	V
High-Side Switch ON Resistance	$R_{ON, HS}$	V_{BIAS} = 5V, I_{LX} = 1A			70	125	mΩ
Low-Side Switch ON Resistance	$R_{ON, LS}$	V_{BIAS} = 5V, I_{LX} = 1A			70	125	mΩ
High-Side Current-Limit Threshold	$ILIM_{PEAK}$			4.1	4.7	5.3	A
Low-Side Negative Current-Limit Threshold	I_{NEG}				-1.2		A
Soft-Start Ramp Time (Note 5)	$I_{SS, 2M}$	f_{SW} = 2.1MHz			3.5	5	ms
	$I_{SS, 400k}$	f_{SW} = 400kHz			5.5	7.5	
Minimum ON Time	T_{ON_MIN}				65	80	ns
Maximum Duty Cycle	DC_{MAX}			98	99		%

Electrical Characteristics (continued)

(V_{SUP} = V_{EN} = 14V, V_{SYNC} = 0V, T_J = -40°C to +150°C unless otherwise noted, V_{OUT} = 5V, (Notes 3 and 4))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Switching Frequency	$f_{SW, 2M}$	f_{SW} = 2.1MHz option	1.925	2.1	2.275	MHz
	$f_{SW, 400K}$	f_{SW} = 400kHz option	360	400	440	kHz
Spread-Spectrum Range	$SS_{6\%}$	V_{SPS} = 5V		±6		%
PGOOD						
PGOOD UV Threshold	$V_{TH\_UV\_R}$	V_{OUT} rising	91	93	95	%
	$V_{TH\_UV\_F}$	V_{OUT} falling	90	92	94	
PGOOD OV Threshold	$V_{TH\_OV\_R}$	V_{OUT} Rising	104	106	108	
	$V_{TH\_OV\_F}$	V_{OUT} Falling	103	105	107	
PGOOD Debounce	$T_{DEB\_PWM, 2M}$	PWM mode, f_{SW} = 2.1MHz option (Note 4)		60		μs
	$T_{DEB\_SKIP, 2M}$	Skip mode, f_{SW} = 2.1MHz option (Note 4)		90		μs
	$T_{DEB\_PWM, 400K}$	PWM mode, f_{SW} = 400kHz option (Note 4)		80		
	$T_{DEB\_SKIP, 400K}$	Skip mode, f_{SW} = 400kHz option (Note 4)		110		
PGOOD High Leakage Current	$I_{LEAK, PGD}$	T_A = +25 °C			1	μA
PGOOD Low Level	$V_{OUT, PGD}$	Sinking 1mA			0.4	V
Logic Levels						
EN Level	EN rising		0.725	1.050	1.450	V
	EN falling		0.550	0.875	1.150	
EN Input Current	$I_{IN, EN}$	V_{EN} = V_{SUP} = 36V, T_A = +25°C			1	μA
External Input Clock Frequency	$FSYNC_{2M, PEAK}$	f_{SW} = 2.1MHz option	1.7		2.6	MHz
	$FSYNC_{400K}$	f_{SW} = 400kHz option	325		500	kHz
SYNC Threshold	$V_{IH, SYNC}$		1.4			V
	$V_{IL, SYNC}$				0.4	
SYNC Internal Pulldown	$R_{PD, SYNC}$			1000		kΩ
SPS Threshold	$V_{IH, SPS}$		1.4			V
	$V_{IL, SPS}$				0.4	
SPS Internal Pulldown	$R_{PD, SPS}$			1000		kΩ
Thermal Protection						
Thermal Shutdown	T_{SHDN}	(Note 4)		175		°C
Thermal Shutdown Hysteresis	$T_{SHDN, HYS}$	(Note 4)		15		°C

Note 3: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

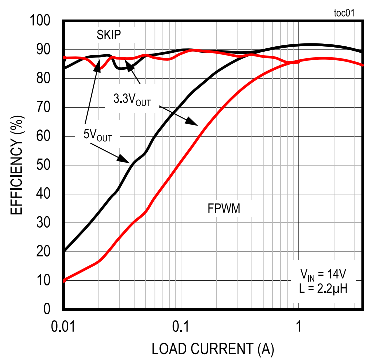
Note 4: Guaranteed by design; not production tested.

Note 5: Soft-start time is measured as the time taken from EN going high to PGOOD going high.

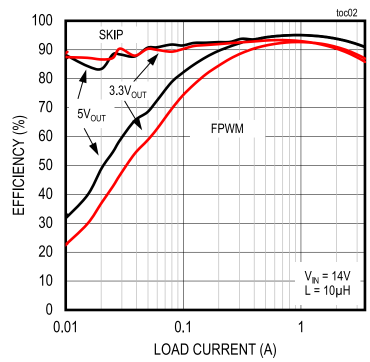
Typical Operating Characteristics

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

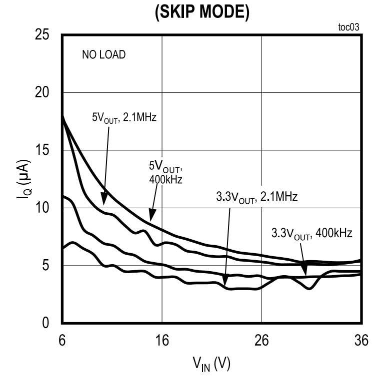
EFFICIENCY vs. LOAD (f_{SW} = 2.1MHz)



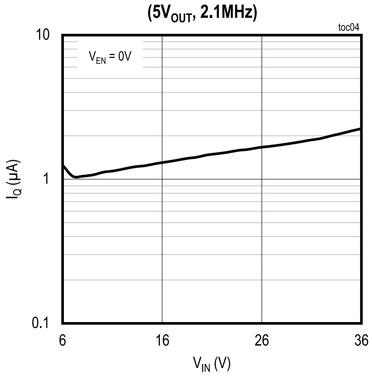
EFFICIENCY vs. LOAD (f_{SW} = 400kHz)



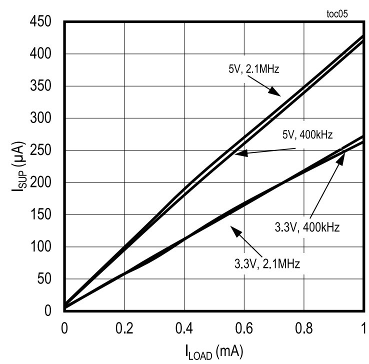
QUIESCENT SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP MODE)



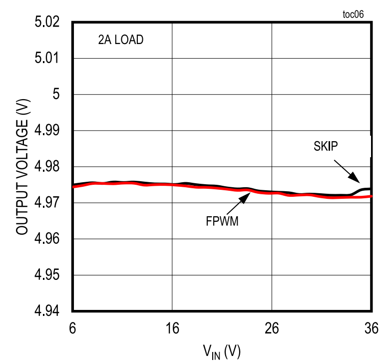
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE (5V_{OUT}, 2.1MHz)



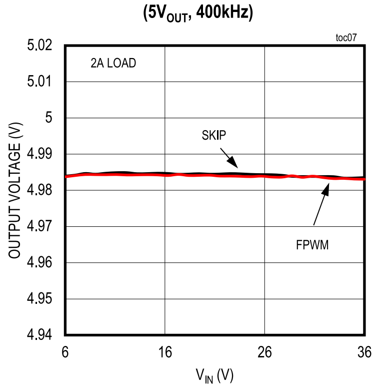
STANDBY CURRENT vs. LOAD CURRENT



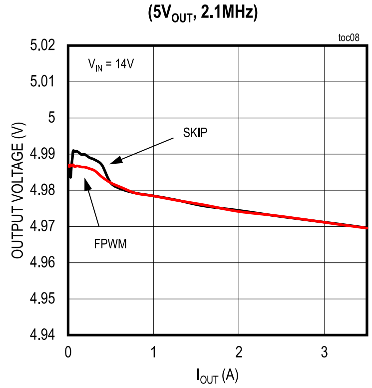
LINE REGULATION (5V_{OUT}, 2.1MHz)



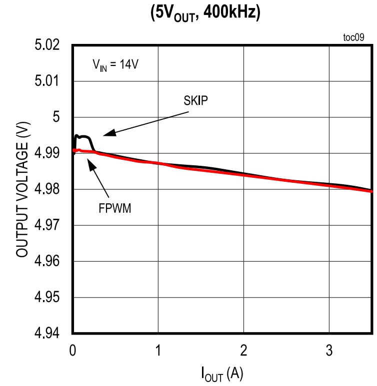
LINE REGULATION (5V_{OUT}, 400kHz)



LOAD REGULATION (5V_{OUT}, 2.1MHz)



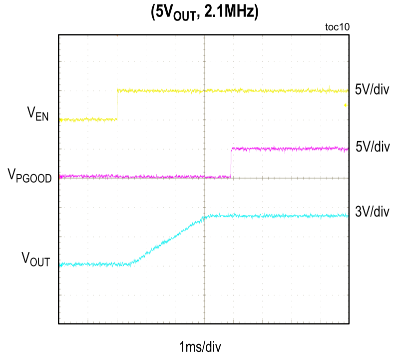
LOAD REGULATION (5V_{OUT}, 400kHz)



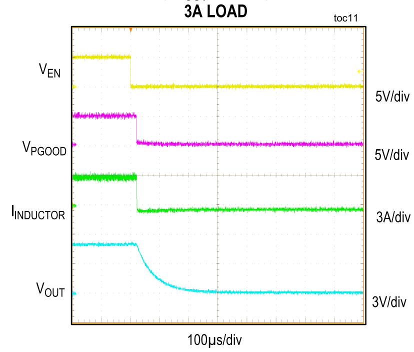
Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

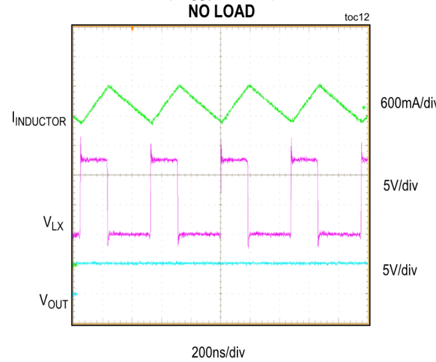
STARTUP WAVEFORM (5V_{OUT}, 2.1MHz)



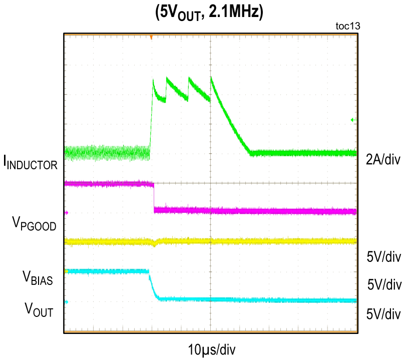
SHUTDOWN WAVEFORM (5V_{OUT}, 2.1MHz) 3A LOAD



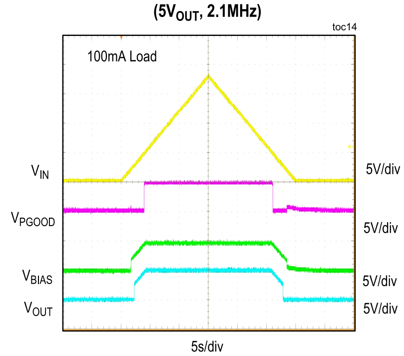
STEADY STATE SWITCHING WAVEFORM (5V_{OUT}, 2.1MHz) NO LOAD



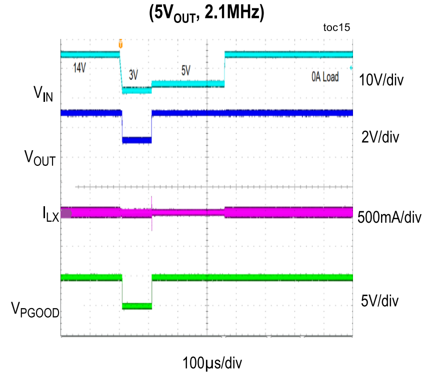
SHORT-CIRCUIT RESPONSE (5V_{OUT}, 2.1MHz)



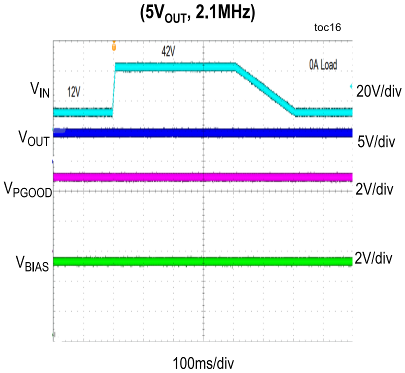
SLOW V_{IN} RAMP (5V_{OUT}, 2.1MHz)



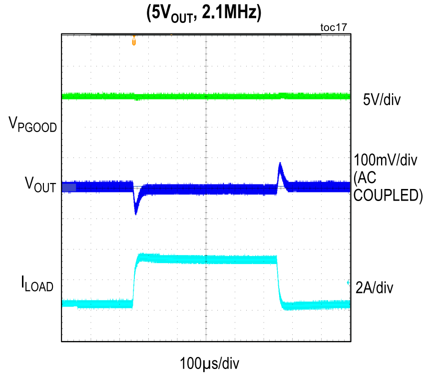
COLD CRANK (5V_{OUT}, 2.1MHz)



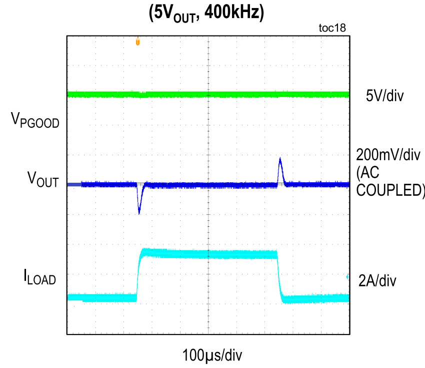
LOAD-DUMP TEST (5V_{OUT}, 2.1MHz)



LOAD-TRANSIENT RESPONSE (5V_{OUT}, 2.1MHz)

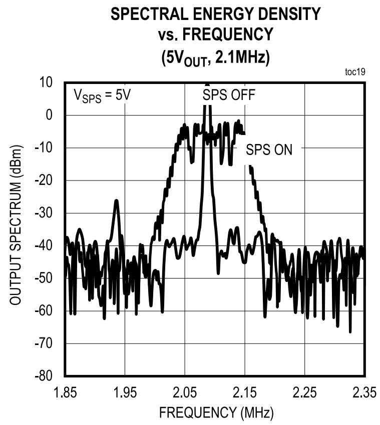


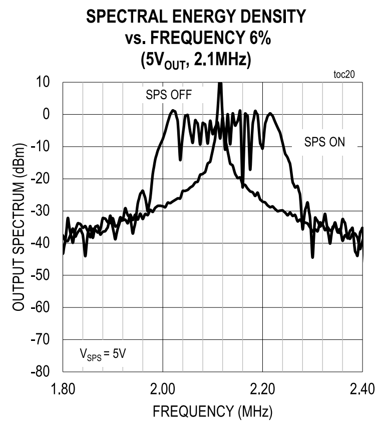
LOAD-TRANSIENT RESPONSE (5V_{OUT}, 400kHz)

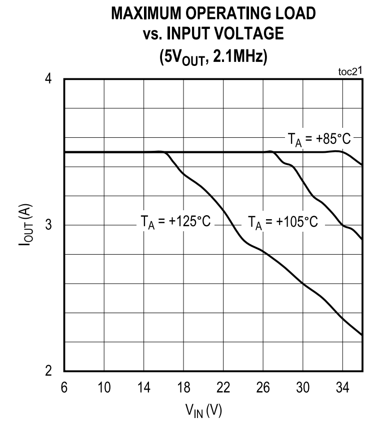


Typical Operating Characteristics (continued)

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

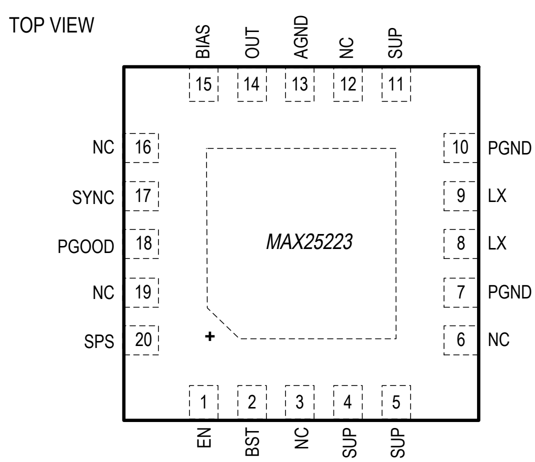






Pin Configuration

MAX25223



TQFN
4mm × 4mm

Pin Description

PIN	NAME	FUNCTION
1	EN	High-Voltage-Compatible Enable Input. If this pin is low, the part is off.
2	BST	Bootstrap pin for HS driver. It is recommended to use a 0.1µF capacitor from BST to LX.
4, 5, 11	SUP	Supply Input. Connect a 4.7µF ceramic capacitor from SUP to ground.
8, 9	LX	Buck Switching Node. Connect inductor between LX and OUT. See the *Inductor Selection* section. If the part is off, this node is high impedance.
15	BIAS	5V Internal BIAS supply. Connect a 1µF (minimum) ceramic capacitor to ground.
17	SYNC	Sync Input. If connected to ground or left floating, skip-mode operation is enabled under light loads. If connected to BIAS, forced PWM mode is enabled. This pin has a 1MΩ internal pulldown resistor.
18	PGOOD	Open-Drain Reset Output. External pullup resistor required.
3, 6, 12, 16, 19	NC	No Connect
20	SPS	Spread-Spectrum Enable. Connect logic-high to enable spread spectrum of internal oscillator or logic-low to disable spread spectrum. This pin has a 1MΩ internal pulldown.
7, 10	PGND	Power Ground.
13	AGND	Analog Ground. Connect it to PGND with a short and thick trace.
14	OUT	Buck Regulator Output-Voltage-Sense Input. Bypass OUT to PGND with ceramic capacitors.

Detailed Description

The MAX25223 family of small, current-mode-controlled buck converters features synchronous rectification and requires no external compensation network. The MAX25223 is designed for 3.5A output current and can stay in dropout by running at 99% duty cycle. Each device provides an accurate output voltage of ±2% within the 6V to 18V input range. Voltage quality can be monitored by observing the PGOOD signal. The devices operate at 2.1MHz (typ) frequency, which allows for small external components, reduces output ripple, and guarantees that there is no AM-band interference. The devices are also available at 400kHz (typ) for minimum switching losses and maximum efficiency.

Each device features an ultra-low 5μA (typ) quiescent supply current in standby mode. The device enters standby mode automatically at light loads if the high-side FET (HSFET) does not turn on for eight consecutive clock cycles. The devices operate from a 3.5V to 36V supply voltage and can tolerate transients up to 42V, making them ideal for automotive applications. The devices are available in factory-trimmed output voltages of 3.3V and 5V. For other fixed-output voltages between 3V to 5.5V, contact the factory for availability.

The symmetrical design of the 4mm x 4mm 20-pin side-wettable TQFN package enables a design with extremely low noise, high efficiency, and superior EMI performance.

Enable Input (EN)

Each device is activated by driving EN high. EN is compatible from a 3.3V logic level to automotive battery levels. EN can be controlled by microcontrollers and automotive KEY or CAN inhibit signals. The EN input has no internal pullup/pulldown current, minimizing the overall quiescent supply current. To realize a programmable undervoltage-lockout level, use a resistor-divider from SUP to EN to AGND.

Bias/UVLO

Each device features undervoltage lockout. When the device is enabled, an internal bias generator turns on. LX begins switching after V_{BIAS} has exceeded the internal undervoltage-lockout level, V_{UVLO} = 2.73V (typ).

Soft-Start

Each device features an internal soft-start timer. The output voltage soft-start time is 3.5ms (typ), which includes the delay in PGOOD. If a short circuit or undervoltage is encountered after the soft-start timer has expired, the device is disabled for 7ms (typ) for 2.1MHz or 11ms (typ) for 400kHz, and then reattempts soft-start. This pattern repeats until the short circuit has been removed.

Oscillator/Synchronization and Efficiency (SYNC)

Each device has an on-chip oscillator that provides a 2.1MHz (typ) or 400kHz (typ) switching frequency. There are two modes of operation, depending on the condition of SYNC. If SYNC is at AGND, the device operates in highly efficient pulse-skipping mode. If SYNC is connected to BIAS or has a clock applied to it, the device is in forced-PWM mode (FPWM). The device can be switched during operation between FPWM mode and skip mode by switching SYNC.

Skip Mode Operation

Skip mode is active when the SYNC pin is connected to ground or is unconnected and the peak load current is less than 600mA (typ). In this mode, the HSFET is turned on until the inductor current ramps up to 600mA (typ) peak value and the internal feedback voltage is above the regulation voltage (1V, typ). At this point, both the HSFETs and low-side FETs (LSFETs) are turned off. Depending on the choice of the output capacitor and the load current, the HSFET turns on when OUT (valley) drops below the 1V (typ) feedback voltage.

When the device is in skip mode, the internal high-voltage LDO is turned off to save current. V_{BIAS} is supplied by the output after the soft-start is completed.

Achieving High Efficiency at Light Loads

Each device operates with very low-quiescent current at light loads to enhance efficiency and conserve battery life. When the device enters skip mode, the output current is monitored to adjust the quiescent current. The lowest quiescent-current standby mode is only available for factory-trimmed devices between 3.0V and 5.5V output voltages. When the output current is less than approximately 5mA, the device operates in the lowest quiescent-current mode (also called standby mode). In this mode, the majority of the internal circuitry in the device (excluding what is necessary to maintain regulation) is turned off to save current. Under no load and with skip mode enabled, the device typically draws 5µA for the 3.3V parts, and 8.5µA for the 5.0V parts. For load currents greater than 5mA, the device enters normal skip mode and still maintains very high efficiency.

Output Voltage Overshoot and Overvoltage Protection

The MAX25223 comes with output overvoltage (OV) protection and output voltage overshoot protection.

If the output voltage exceeds the OV protection rising threshold, a fault signal is sent to the PGOOD pin which asserts low. Normal operation resumes when the output voltage goes below the falling OV threshold.

During dropout, the output voltage closely follows the input voltage but is below the regulation point. The device runs at maximum duty cycle to satisfy the loop, and the internal error-amplifier output is railed high. When the input voltage rises above the output, the device exits dropout but the internal error-amplifier output takes some time to return to steady state. This causes an overshoot in the output voltage. To limit this overshoot, the device clamps the output of the error amplifier while exiting dropout, causing it to discharge faster and limiting the output-voltage overshoot. The actual value of the overshoot depends on the output capacitor, inductor, and load. In case output voltage increases above the OV rising threshold, OV protection will be activated.

Controlled EMI with Forced-Fixed Frequency

In FPWM mode, the device attempts to operate at a constant switching frequency for all load currents. For tightest frequency control, apply the operating frequency to SYNC. The advantage of FPWM is a constant switching frequency, which improves EMI performance; the disadvantage is that considerable current can be discarded.

Extended Input Voltage Range

In some cases, the device is forced to deviate from its operating frequency, independent of the state of SYNC. For input voltages above 18V (for $3.3V_{OUT}$ or lower), the required duty cycle to regulate its output might be smaller than the minimum on-time (65ns, typ). In this event, the device is forced to lower its switching frequency by skipping pulses.

If the input voltage is reduced and the device approaches dropout, it continuously tries to turn on the HSFET. To maintain gate charge on the HSFET, the BST capacitor must be periodically recharged. To ensure proper charge on the BST capacitor when in dropout, the HSFET is turned off every 20µs and the LSFET is turned on for approximately 200ns. This gives an effective duty cycle of greater than 99%, and a switching frequency of 50kHz when in dropout.

Spread-Spectrum Option

Each device has an optional spread spectrum enabled by the SPS pin. If SPS is pulled high, the internal operating frequency varies by ±6% relative to the internally generated operating frequency. ±3% Spread-spectrum option is also possible, contact the factory for availability. Spread spectrum is offered to improve EMI performance of the device.

The internal spread spectrum does not interfere with the external clock applied on the SYNC pin. It is active only when the device is running with an internally generated switching frequency.

Power-Good (PGOOD)

Each device features an open-drain power-good output. PGOOD is an active-high output that pulls low when the output voltage is below 92% (typ) of its nominal value or above 106% (typ). PGOOD is high impedance when the output voltage is between 93% (typ) and 105% (typ) of its nominal value. Connect a 10kΩ (typ) pullup resistor to an external supply or to the on-chip BIAS output.

Overcurrent Protection

Each device limits the peak output current to 4.7A (typ). The accuracy of the current limit is ±12%, making selection of external components very easy. To protect against short-circuit events, the device shuts off when OUT is below 50% of V_{OUT} and an overcurrent event is detected. The device attempts a soft-start restart every 7ms and remains off if the short circuit has not been removed. When the current limit is no longer present, it reaches the output voltage by following the normal soft-start sequence. If the device's die reaches the thermal limit of +175°C (typ) during the current-limit event, it immediately shuts off.

Thermal-Overload Protection

Each device features thermal-overload protection. The device turns off when the junction temperature exceeds +175°C (typ). Once the device cools by 15°C (typ), it turns back on with a soft-start sequence.

Applications Information

Setting the Output Voltage

MAX25223 comes with an internally fixed output voltage setting. The output voltage can be programmed anywhere between 3V to 6V in 100mV steps. Default options of 5V and 3.3V are available. Contact the factory for other fixed V_{OUT} options.

Input Capacitor

The discontinuous input current of the buck converter causes large input-ripple current. Switching frequency, peak inductor current, and the allowable peak-to-peak input-voltage ripple dictate the input-capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak-to-average current ratio, yielding a lower input-capacitance requirement.

MAX25223 incorporates a symmetrical pinout that can be leveraged for better EMI performance. Connect two high-frequency 0603 or smaller capacitors on two SUP pins on either side of the package for good EMI performance. Connect a high-quality, 4.7µF low-ESR ceramic capacitor (or equivalent value in capacitance) on the SUP pin for low-input voltage ripple.

The input ripple is primarily composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Assume that input-voltage ripple from the ESR and the capacitor discharge is equal to 50% each. The following equations show the ESR and capacitor requirement for a target voltage ripple at the input:

Equations 1:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT} + (\Delta I_{P-P}/2)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

$$\text{where } \Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$$\text{and } D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output current, D is the duty cycle, and f_{SW} is the switching frequency. Use additional input capacitance at lower input voltages to avoid possible undershoot below the UVLO threshold during transient loading.

Inductor Selection

Inductor design is a compromise between the size, efficiency, control-loop bandwidth, and stability of the converter. Insufficient inductance value would increase the inductor current ripple, causing higher conduction losses and higher output voltage ripple. Since the slope compensation is fixed internally for MAX25223, it might also cause current-mode-control instability to appear. A large inductor reduces the ripple, but increases the size and cost of the solution and slows the response. Table 1 provides optimized inductor values for respective switching frequency. The nominal standard value selected should be within ±50% of the specified inductance.

Note: Choosing an inductor higher than the recommended value might slow down the transient response of the converter and increase the overshoot/undershoot of output voltage during load transients. Recommended inductance in the following table is an optimum value based on the closed loop design of this converter and PGOOD thresholds.

Table 1. Inductor Selection

PART	RECOMMENDED INDUCTANCE (µH)
f_{SW} = 2.1MHz	2.2
f_{SW} = 400kHz	8.2

Output Capacitor

Output capacitance is selected to satisfy the output load-transient requirements. During a load step, the output current changes almost instantaneously whereas the inductor is slow to react. During this transition time, the load-charge requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. For a buck converter that is controlled by peak-current (as employed in the MAX25223), output capacitance also affects the control-loop stability.

Based on the internal-compensation design of MAX25223, the recommended output capacitances for optimal phase margin (>60°, typ) are shown in Table 2. Recommended values are the actual capacitances, after accounting for voltage derating. If a lower or higher output capacitance is required for the application, contact the factory for an optimized solution. Specifically, if a sharp load step at low Vin is expected in the application, that can cause a higher undershoot/overshoot causing PGOOD to toggle. In such a scenario, a higher output capacitance might be required to avoid PGOOD toggling.

Table 2. Output-Capacitance Selection

SWITCHING FREQUENCY	RECOMMENDED NOMINAL OUTPUT CAPACITANCE (μF)	RECOMMENDED MINIMUM OUTPUT CAPACITANCE (μF)
f_{SW} = 2.1MHz	35	25
f_{SW} = 400kHz	44	34

The allowable output-voltage ripple and the maximum deviation of the output voltage during step-load currents determine the output capacitance and its ESR. The output ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use Equation 2 to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output-ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

Equations 2:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P\_P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

where $\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$ and $V_{OUT\_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above, and f_{SW} is the converter's switching frequency. The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient-load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equations 3:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} \geq \left(I_{STEP}^2 \times \frac{L}{2 \times (V_{IN} - V_{OUT}) \times D_{MAX} \times \Delta V_Q}\right) + \left(I_{STEP} \times \frac{t_{DELAY}}{\Delta V_Q}\right)$$

where I_{STEP} is the load step and t_{DELAY} is the delay for the PWM mode, the worst-case delay would be (1 - D) x t_{SW} when the load step occurs immediately after a turn-on cycle. This delay is greater in skip mode.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching-power losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity. The package for MAX25223 offers a unique symmetrical design, which helps cancel the magnetic field generated in the opposite direction. Adhere the following guidelines to ensure a low-noise PCB layout:

1. Place two high-frequency ceramic capacitors (C_{IN}) on two SUP pins, on opposite sides of the IC and close to the device. High-frequency AC current flows on the loop formed by the input capacitor and the half-bridge MOSFETs internal to the device (see Figure 1). A small loop would reduce the radiating effect of high switching currents and improve EMI functionality. Two capacitors placed on opposite sides create current loops in the opposite direction, which cancels the magnetic field to reduce radiated EMI.
2. Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as a heat exchanger between the PCB and ambient environment, expose the copper area on the top and bottom. Add a few small vias (or one large via) on the copper pad for efficient heat transfer.
3. Connect PGND and AGND pins directly to the exposed pad under the IC. This ensures the shortest connection path between AGND and PGND.
4. Keep the power traces and load connections short. This practice is essential for high efficiency. Use a thick copper PCB to enhance full-load efficiency and power-dissipation capability.
5. Using internal PCB layers as ground planes helps to improve the EMI functionality, as ground planes act as a shield against radiated noise. Spread multiple vias around the board (especially near the ground connections) for better overall ground connection.
6. Keep the bias capacitor (C_{BIAS}) close to the device to reduce the bias current loop. This helps to reduce noise on the bias for smooth operation.
7. Place output capacitors (C_{OUT}) symmetrically on the opposite sides of the inductor. This further reduces the radiated noise.

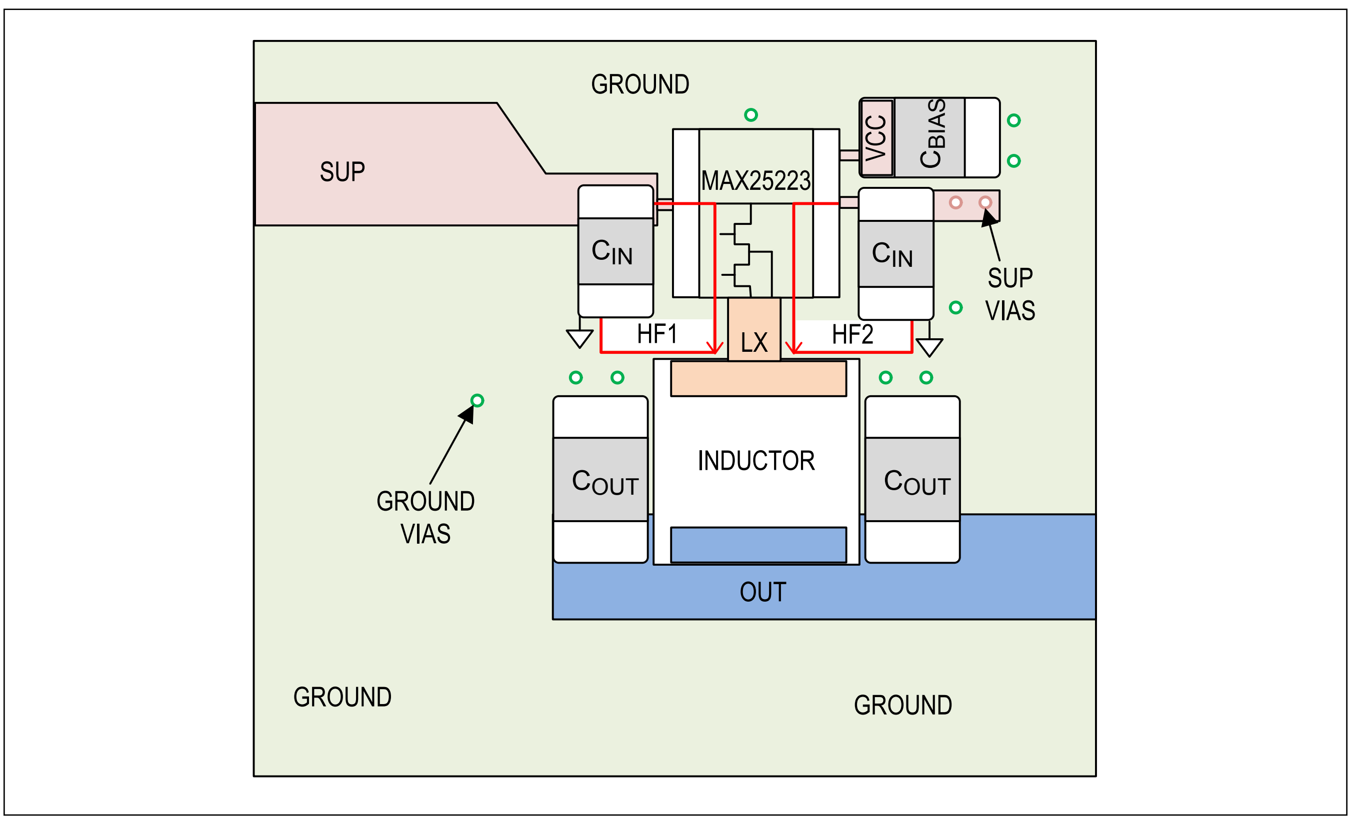
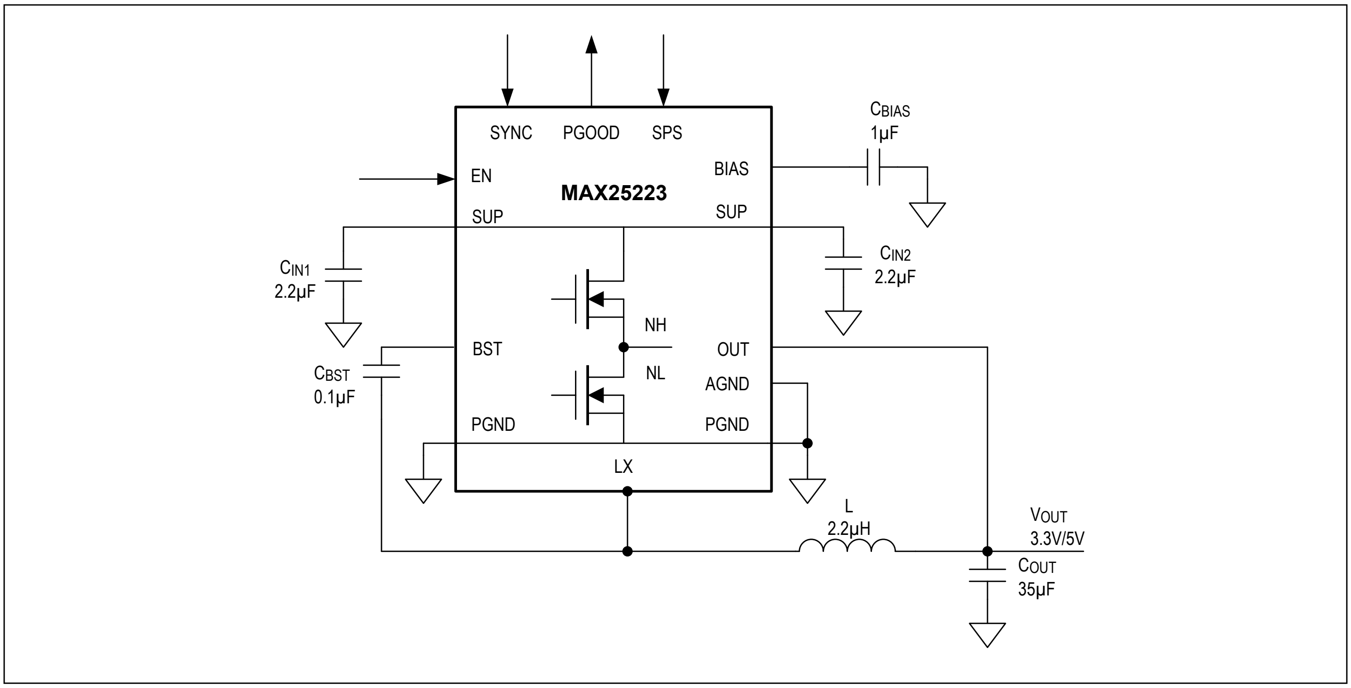


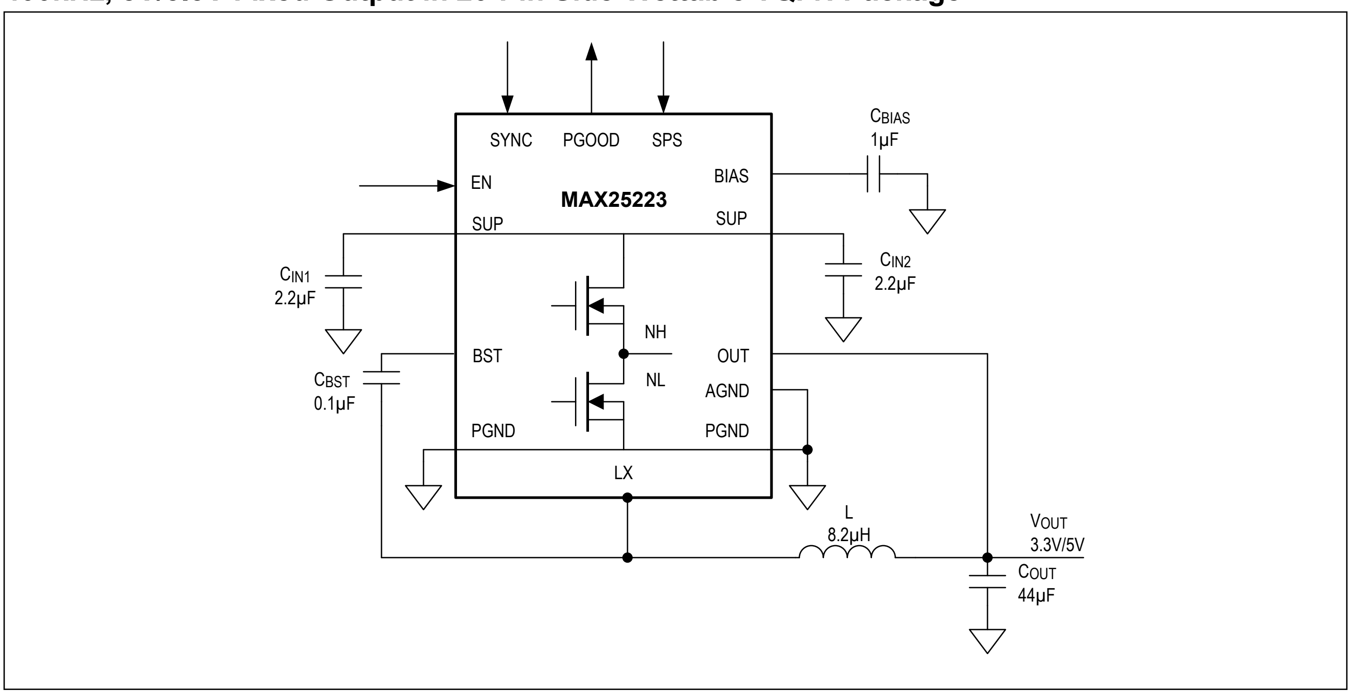
Figure 1. Recommended PCB Layout for MAX25223

Typical Application Circuits

2.1MHz, 5V/3.3V Fixed Output in 20-Pin Side-Wettable TQFN Package



400kHz, 5V/3.3V Fixed Output in 20-Pin Side-Wettable TQFN Package



Ordering Information

PART	V_{OUT} [1]	f_{SW}	PIN-PACKAGE	SPREAD SPECTRUM [2]	I_{OUT} (A)
MAX25223ATPA/VY+	5.0V (fixed)	2.1MHz	T2044Y+5C	±6%	3.5
MAX25223ATPB/VY+	3.3V (fixed)	2.1MHz	T2044Y+5C	±6%	3.5
MAX25223ATPD/VY+*	5.0V (fixed)	400kHz	T2044Y+5C	±6%	3.5
MAX25223ATPE/VY+*	3.3V (fixed)	400kHz	T2044Y+5C	±6%	3.5
MAX25223ATPF/VY+*	5.0V (fixed)	2.1MHz	T2044Y+5C	±3%	3.5
MAX25223ATPG/VY+*	4.8V (fixed)	2.1MHz	T2044Y+5C	±6%	3.5
MAX25223ATPH/VY+*	4.8V (fixed)	2.1MHz	T2044Y+5C	±3%	3.5

Note: All part numbers are OTP versions, no metal mask differences.

1. Other V_{OUT} options possible between 3V to 6V in 100mV steps - Contact factory for availability

2. Contact factory for ±3% Spread Spectrum option

/V Denotes an automotive qualified part.

/VY Denotes a Side-Wettable automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Future Product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/21	Initial release	—