# 74AHC373; 74AHCT373

## Octal D-type transparant latch; 3-state

Rev. 03 — 20 May 2008 Product data sheet

## 1. General description

The 74AHC373; 74AHCT373 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC373; 74AHCT373 consists of eight D-type transparent latches featuring separate D-type inputs for each latch and 3-state true outputs for bus oriented applications. A latch enable input (LE) and an output enable input ($\overline{OE}$) are common to all latches.

When pin LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding Dn input changes. When pin LE is LOW, the latches store the information that is present at the Dn inputs, after a set-up time preceding the HIGH-to-LOW transition of LE.

When pin $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When pin $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74AHC373; 74AHCT373 is functionally identical to the 74AHC573; 74AHCT573, but has a different pin arrangement.

## 2. Features

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Common 3-state output enable input
- Inputs accepts voltages higher than $V_{CC}$
- Functionally identical to the 74AHC573; 74AHCT573
- Input levels:
  - For 74AHC373: CMOS input level
  - For 74AHCT373: TTL input level
- ESD protection:
  - HBM EIA/JESD22-A114E exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| **74AHC373** | | | | |
| 74AHC373D | –40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74AHC373PW | –40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| **74AHCT373** | | | | |
| 74AHCT373D | –40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74AHCT373PW | –40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |

## 4. Functional diagram

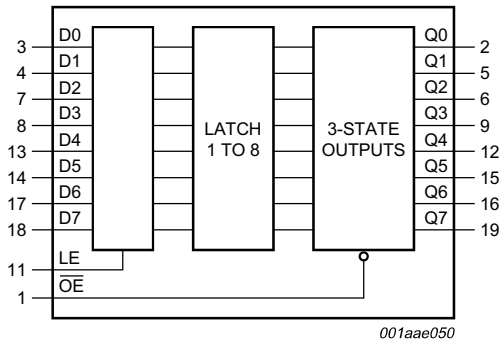



**Fig 1. Functional diagram**

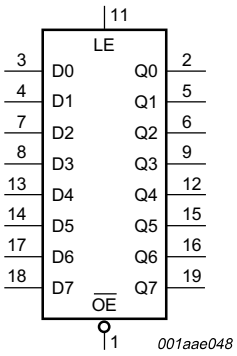



Fig 2. Logic symbol

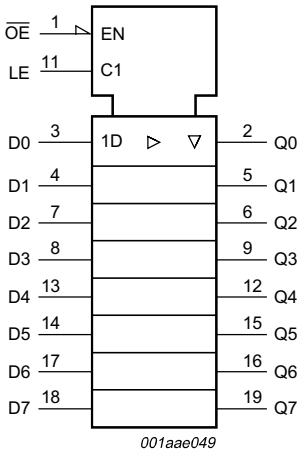



Fig 3. IEC logic symbol

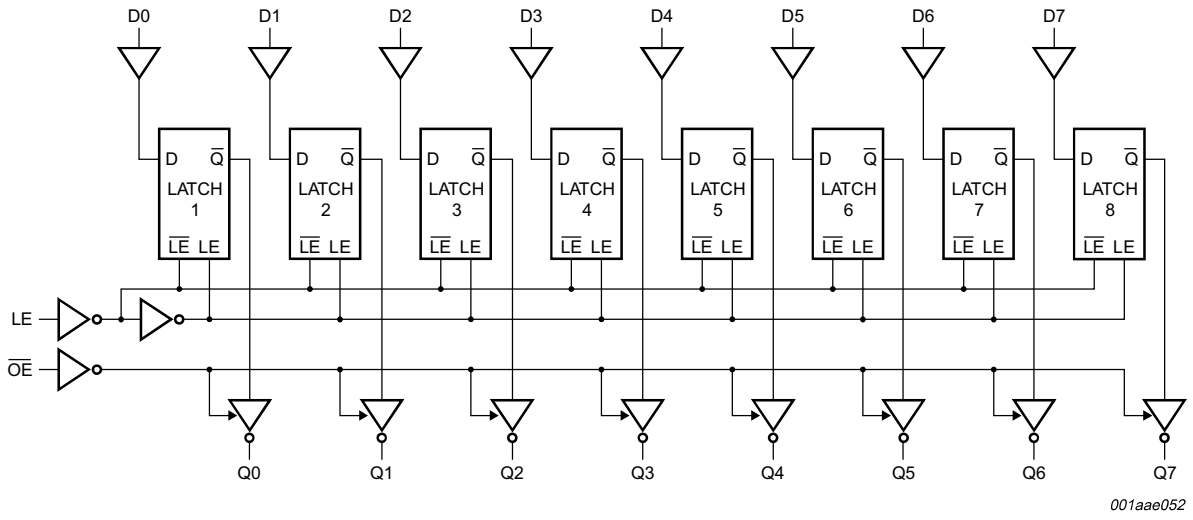



Fig 4. Logic diagram

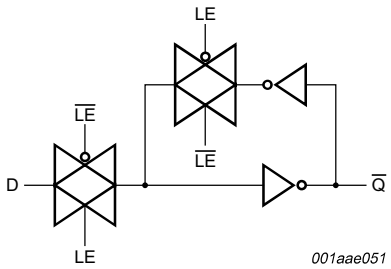



Fig 5. Logic diagram (one latch)

# 5. Pinning information

## 5.1 Pinning

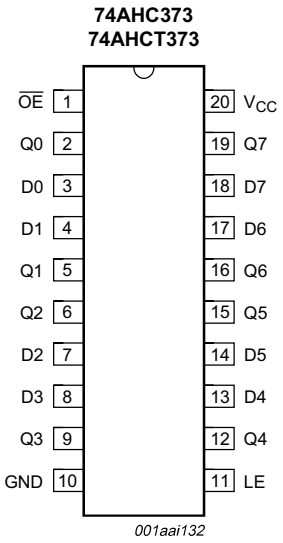



**Fig 6. Pin configuration SO20 and TSSOP20**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $\overline{OE}$ | 1 | 3-state output enable input (active LOW) |
| Q0 | 2 | 3-state latch output |
| D0 | 3 | data input |
| D1 | 4 | data input |
| Q1 | 5 | 3-state latch output |
| Q2 | 6 | 3-state latch output |
| D2 | 7 | data input |
| D3 | 8 | data input |
| Q3 | 9 | 3-state latch output |
| GND | 10 | ground (0 V) |
| LE | 11 | latch enable input (active HIGH) |
| Q4 | 12 | 3-state latch output |
| D4 | 13 | data input |
| D5 | 14 | data input |
| Q5 | 15 | 3-state latch output |
| Q6 | 16 | 3-state latch output |
| D6 | 17 | data input |

**Table 2. Pin description** *…continued*

| Symbol | Pin | Description |
|---|---|---|
| D7 | 18 | data input |
| Q7 | 19 | 3-state latch output |
| $V_{CC}$ | 20 | supply voltage |

## 6. Functional description

**Table 3. Function table[1]**

| Operating mode | Control | | Input | Internal latch | Output |
|---|---|---|---|---|---|
| | $\overline{OE}$ | LE | Dn | | Q0 to Q7 |
| Enable and read register (transparent mode) | L | H | L | L | L |
| | | | H | H | H |
| Latch and read register | L | L | l | L | L |
| | | | h | H | H |
| Latch register and disable outputs | H | X | X | X | Z |
| | | | X | X | Z |

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
X = don't care;
Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7.0 | V |
| $V_I$ | input voltage | | | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V | [1] | –20 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | –20 | +20 | mA |
| $I_O$ | output current | $V_O = –0.5$ V to $(V_{CC} + 0.5$ V) | | –25 | +25 | mA |
| $I_{CC}$ | supply current | | | - | +75 | mA |
| $I_{GND}$ | ground current | | | –75 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = –40$ °C to +125 °C | [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO20 packages: above 70 °C the value of $P_{tot}$ derates linearly at 8 mW/K.
For TSSOP20 packages: above 60 °C the value of $P_{tot}$ derates linearly at 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **74AHC373** | | | | | | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 100 | ns/V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 20 | ns/V |
| **74AHCT373** | | | | | | |
| $V_{CC}$ | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 20 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74AHC373** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | $V_{CC}$ = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | $V_{CC}$ = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = –50 µA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = –50 µA; $V_{CC}$ = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | $I_O$ = –50 µA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –4.0 mA; $V_{CC}$ = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | | $I_O$ = –8.0 mA; $V_{CC}$ = 4.5 V | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 50 µA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 µA; $V_{CC}$ = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 µA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | $I_O$ = 8.0 mA; $V_{CC}$ = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |

**Table 6. Static characteristics** *…continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | µA |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | µA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| $C_I$ | input capacitance | $V_I = V_{CC}$ or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| $C_O$ | output capacitance | | - | 4 | - | - | - | - | 10 | pF |
| **74AHCT373** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = –50 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –8.0 mA | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 50 µA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | µA |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | µA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I = V_{CC}$ – 2.1 V; other pins at $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 4.5 V to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | µA |
| $C_I$ | input capacitance | $V_I = V_{CC}$ or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| $C_O$ | output capacitance | | - | 4 | - | - | - | - | 10 | pF |

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.*

| Symbol | Parameter | Conditions | | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| **74AHC373** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | Dn to Qn; see Figure 7 | [2] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 6.0 | 11.4 | 1.0 | 13.5 | 1.0 | 14.5 | ns |
| | | $C_L$ = 50 pF | | - | 7.8 | 14.9 | 1.0 | 17.0 | 1.0 | 19.0 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.0 | 7.2 | 1.0 | 8.5 | 1.0 | 9.0 | ns |
| | | $C_L$ = 50 pF | | - | 5.3 | 9.2 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| | | LE to Qn; see Figure 8 | [2] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 6.3 | 11.0 | 1.0 | 13.0 | 1.0 | 14.0 | ns |
| | | $C_L$ = 50 pF | | - | 8.3 | 14.5 | 1.0 | 16.5 | 1.0 | 18.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.3 | 7.2 | 1.0 | 8.5 | 1.0 | 9.0 | ns |
| | | $C_L$ = 50 pF | | - | 5.6 | 9.7 | 1.0 | 11.1 | 1.0 | 12.5 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to Qn; see Figure 9 | [3] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 5.6 | 11.4 | 1.0 | 13.5 | 1.0 | 14.5 | ns |
| | | $C_L$ = 50 pF | | - | 7.5 | 14.9 | 1.0 | 17.0 | 1.0 | 19.0 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 3.8 | 8.1 | 1.0 | 9.5 | 1.0 | 10.5 | ns |
| | | $C_L$ = 50 pF | | - | 5.2 | 10.1 | 1.0 | 11.5 | 1.0 | 13.0 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to Qn; see Figure 9 | [4] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 5.6 | 10.0 | 1.0 | 12.0 | 1.0 | 13.0 | ns |
| | | $C_L$ = 50 pF | | - | 9.2 | 13.3 | 1.0 | 15.0 | 1.0 | 17.0 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.3 | 7.2 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| | | $C_L$ = 50 pF | | - | 6.4 | 9.2 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| $t_W$ | pulse width | LE HIGH or LOW; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| $t_{su}$ | set-up time | Dn to LE; see Figure 10 | | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 4.0 | - | - | 4.0 | - | 4.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 4.0 | - | - | 4.0 | - | 4.0 | - | ns |

**Table 7. Dynamic characteristics** *…continued*

*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 11.*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| $t_h$ | hold time | Dn to LE; see Figure 10 | | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 1.0 | - | - | 1.0 | - | 1.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 1.0 | - | - | 1.0 | - | 1.0 | - | ns |
| $C_{PD}$ | power dissipation capacitance | $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ | [5] | - | 10 | - | - | - | - | - | pF |
| **74AHCT373; $V_{CC}$ = 4.5 V to 5.5 V** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | Dn to Qn; see Figure 7 | [4] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.0 | 8.5 | 1.0 | 9.5 | 1.0 | 11.0 | ns |
| | | $C_L$ = 50 pF | | - | 5.2 | 9.5 | 1.0 | 10.5 | 1.0 | 12.0 | ns |
| | | LE to Qn; see Figure 8 | | | | | | | | | |
| | | $C_L$ = 15 pF | [4] | - | 4.3 | 12.3 | 1.0 | 13.5 | 1.0 | 15.5 | ns |
| | | $C_L$ = 50 pF | | - | 5.5 | 13.3 | 1.0 | 14.5 | 1.0 | 17.0 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to Qn; see Figure 9 | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.0 | 10.9 | 1.0 | 12.5 | 1.0 | 14.0 | ns |
| | | $C_L$ = 50 pF | [4] | - | 5.2 | 11.9 | 1.0 | 13.5 | 1.0 | 15.0 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to Qn; see Figure 9 | | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.4 | 10.2 | 1.0 | 11.0 | 1.0 | 13.0 | ns |
| | | $C_L$ = 50 pF | | - | 6.5 | 11.2 | 1.0 | 12.0 | 1.0 | 14.0 | ns |
| $t_W$ | pulse width | LE HIGH; see Figure 8 | [4] | 6.5 | - | - | 6.5 | - | 6.5 | - | ns |
| $t_{su}$ | set-up time | Dn to LE; see Figure 10 | | 3.5 | - | - | 3.5 | - | 3.5 | - | ns |
| $t_h$ | hold time | Dn to LE; see Figure 10 | | 1.5 | - | - | 1.5 | - | 1.5 | - | ns |
| $C_{PD}$ | power dissipation capacitance | $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ | [5] | - | 12 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage ($V_{CC}$ = 3.3 V and $V_{CC}$ = 5.0 V).

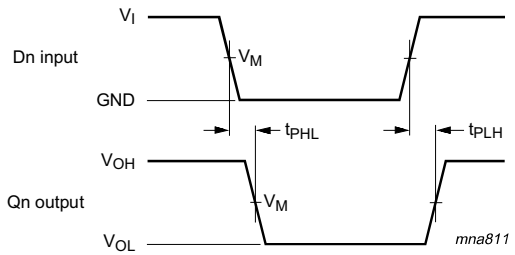
[2] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.

[3] $t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$.

[4] $t_{dis}$ is the same as $t_{PHZ}$ and $t_{PLZ}$.

[5] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

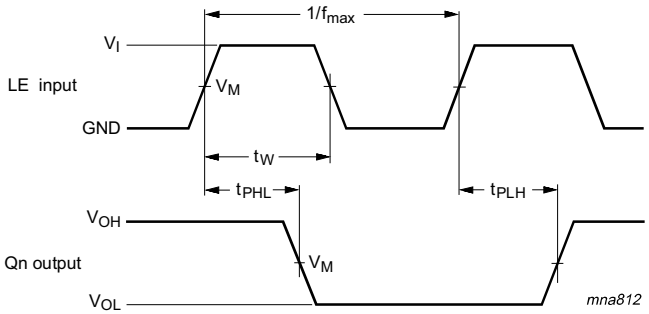
## 11. Waveforms




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

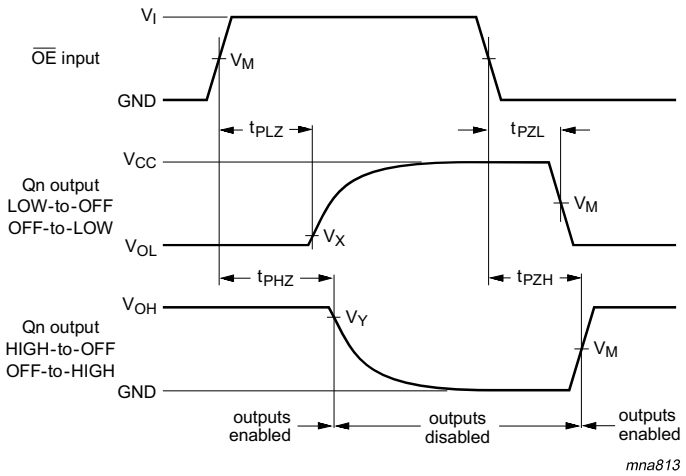
**Fig 7. Data input to output propagation delays**




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

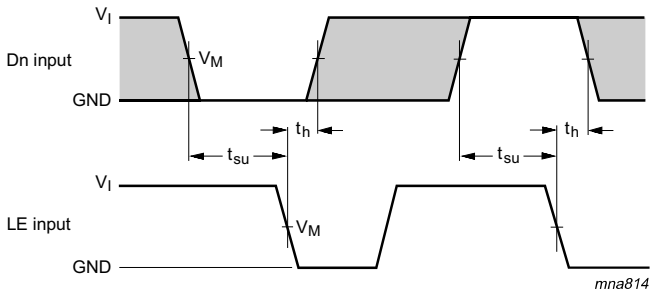
**Fig 8. Latch enable pulse width and input to output propagation delays**




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 9. Enable and disable times**




Measurement points are given in Table 8.

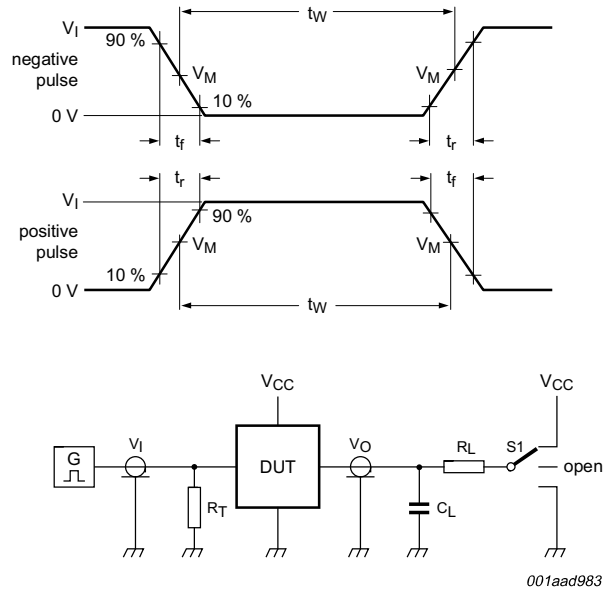
$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predicable output performance.

**Fig 10. Data set-up and hold times**

**Table 8. Measurement points**

| Type | Input | Output | | |
|---|---|---|---|---|
| | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 74AHC373 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |
| 74AHCT373 | 1.5 V | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = load capacitance including jig and probe capacitance.

$R_L$ = load resistance.

S1 = test selection switch.

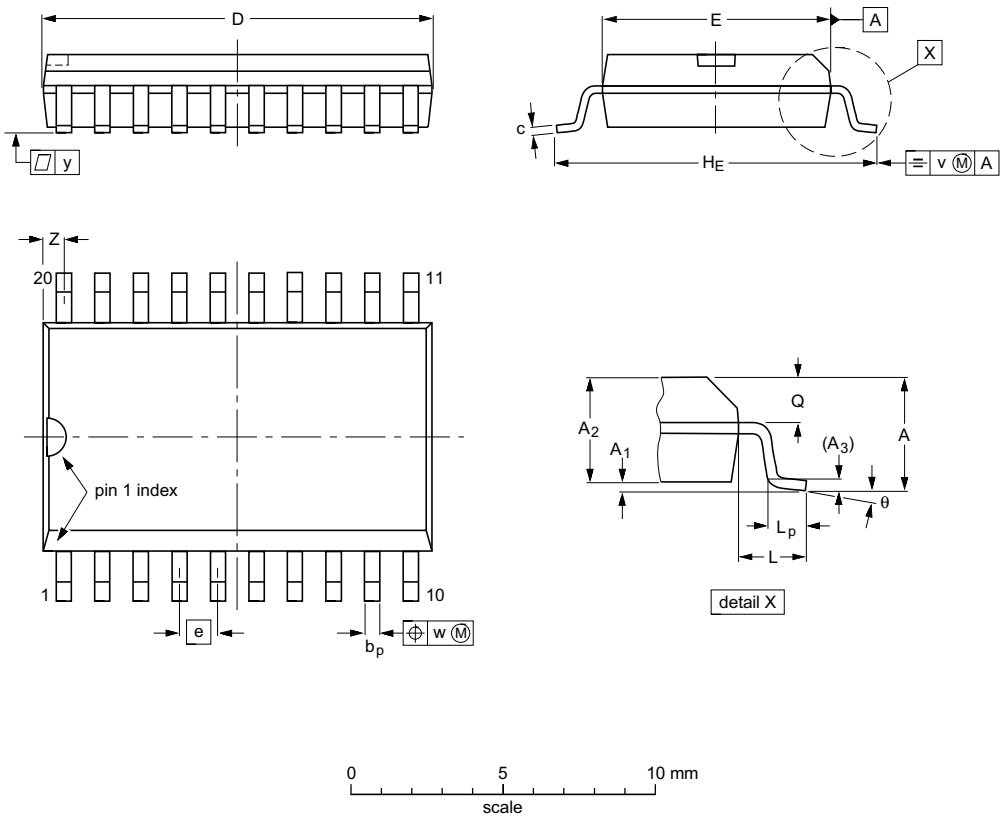
**Fig 11. Test circuitry for switching times**

**Table 9. Test data**

| Type | Input | | Load | | S1 position | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 74AHC373 | $V_{CC}$ | ≤ 3.0 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |
| 74AHCT373 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |

## 12. Package outline

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | 8°<br>0° |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

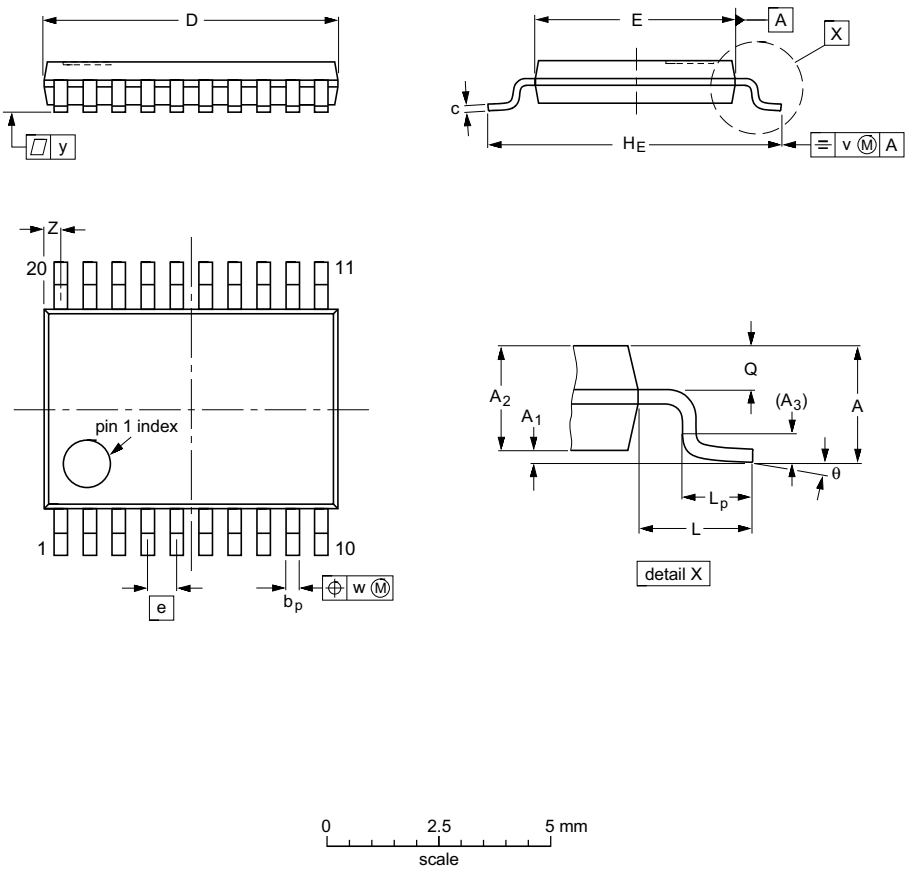
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 12. Package outline SOT163-1 (SO20)**

**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT360-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 13. Package outline SOT360-1 (TSSOP20)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74AHC_AHCT373_3 | 20080520 | Product data sheet | - | 74AHC_AHCT373_2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Table 6: conditions for the input leakage current have been changed. | | | |
| 74AHC_AHCT373_2 | 19991123 | Product specification | - | 74AHC_AHCT373_1 |
| 74AHC_AHCT373_1 | 19981211 | Product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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