A product Line of
Diodes Incorporated

PI6CDBL401B

4-Output Low Power PCIE GEN1-2-3 Buffer

Features

- 4x 100MHz low power HCSL or LVDS compatible outputs
- PCIe 3.0, 2.0 and 1.0 compliant
- Programmable output amplitude and slew rate
- Core supply voltage of 3.3V +/-10%
- Output supply voltage of 1.8V, 2.5V and 3.3V
- Industrial ambient operation temperature
- Available in lead-free package: 32-TQFN

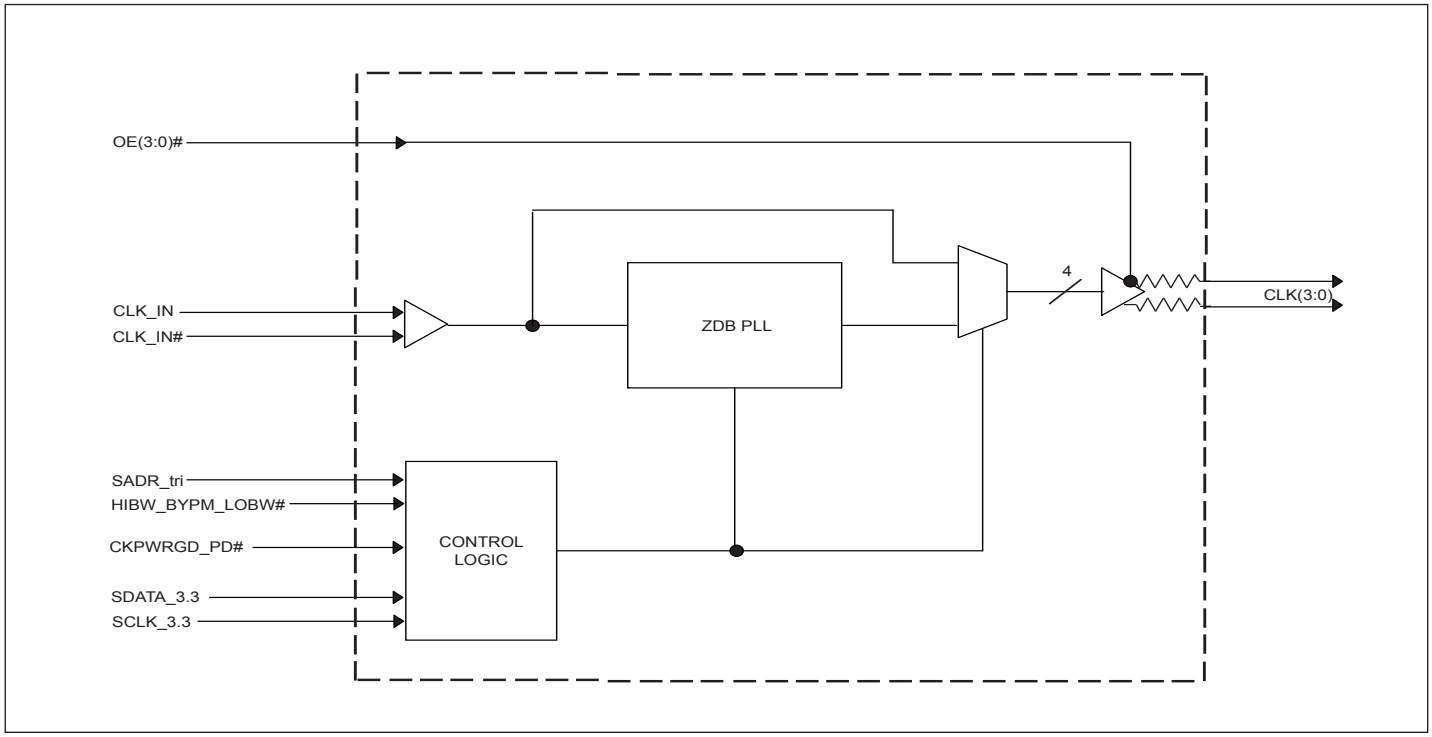
Description

The PI6CDBL401B is a 4-output low power buffer for 100MHz PCIe Gen1, Gen2 and Gen3 applications with integrated output terminations providing Zo=100Ω. The device has 4 output enables for clock management, and 3 selectable SMBus addresses.

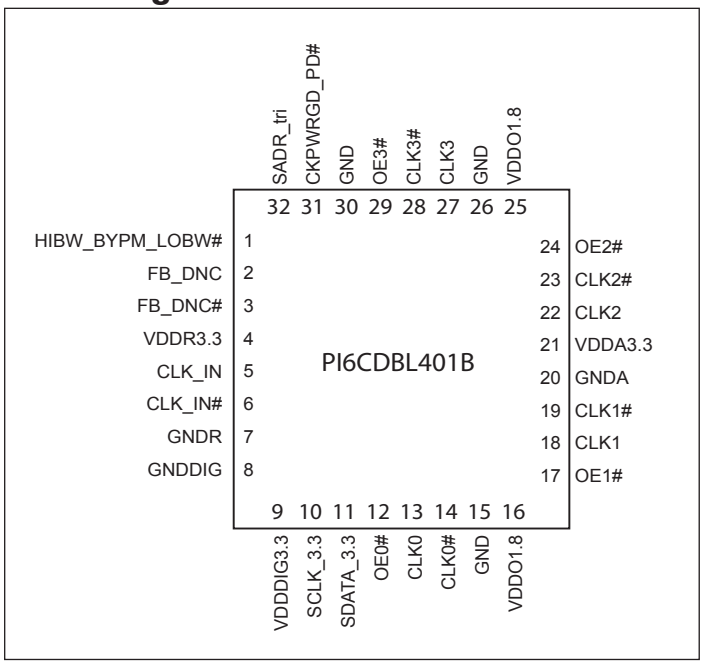
Applications

- PCIe 3.0/2.0/1.0 clock distribution

Block Diagram



Pin Configuration



SMBus Address Selection Table

	SADR	Address	+ Read / Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	1/0
	M	1101100	1/0
	1	1101101	1/0

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	CLKx		PLL
				True O/P	Comp. O/P	
0	x	x	x	Low	Low	Off
1	Running	0	x	Low	Low	On[1]
1	Running	1	0	Running	Running	On[1]
1	Running	x	1	Low	Low	On[1]

1. If bypass mode is selected, the PLL will be off, and outputs will be running

Power Connections

Pin Number		
VDD	GND	Description
4	7	Input receiver analog
9	8	Digital Power
16, 25	15, 26, 30	DIF outputs
21	20	PLL Analog

PLL Operating Mode

HiBW_BypM_LoBW#	MODE	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	PLL Lo BW	00, 10	00, 10
M	Bypass	01	01
1	PLL Hi BW	11	11

Pin Descriptions

Pin#	Pin Name	Type	Description
1	HIBW_BYPM_ LOBW#	Input	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
2	FB_DNC	Output	True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
3	FB_DNC#	Output	Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
4	VDDR3.3	Power	3.3V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
5	CLK_IN	Input	True Input for differential reference clock.
6	CLK_IN#	Input	Complementary Input for differential reference clock.
7	GNDR	Power	Analog Ground pin for the differential input (receiver)
8	GNDDIG	Power	Ground pin for digital circuitry
9	VDDDIG3.3	Power	3.3V digital power (dirty power)
10	SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.
11	SDATA_3.3	Input/Output	Data pin for SMBus circuitry, 3.3V tolerant.
12	OE0#	Input	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
13	CLK0	Output	Differential true clock output
14	CLK0#	Output	Differential Complementary clock output
15	GND	Power	Ground pin.
16	VDDO1.8	Power	Power supply for outputs, range from 1.8V~3.3V.
17	OE1#	Input	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
18	CLK1	Output	Differential true clock output
19	CLK1#	Output	Differential Complementary clock output
20	GNDA	Power	Ground pin for the PLL core.
21	VDDA3.3	Power	3.3Vpower for the PLL core.
22	CLK2	Output	Differential true clock output
23	CLK2#	Output	Differential Complementary clock output
24	OE2#	Input	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
25	VDDO1.8	Power	Power supply for outputs, range from 1.8V~3.3V.
26	GND	Power	Ground pin.
27	CLK3	Output	Differential true clock output
28	CLK3#	Output	Differential Complementary clock output
29	OE3#	Input	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
30	GND	Power	Ground pin.

Pin Descriptions Cont...

Pin#	Pin Name	Type	Description
31	CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
32	SADR_tri	Input	Tri-level latch to select SMBus Address. See SMBus Address Selection Table.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential.....4.6V
All Inputs and Output..... -0.5V toV_{DD}+0.5V
Ambient Operating Temperature..... -40 to +85°C
Storage Temperature..... –65°C to +150°C
Junction Temperature ..... 125°C
Soldering Temperature.....260°C
ESD Protection (Input) .....2000V(HBM)

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics–Clock Input Parameters (T_A = -40~85°C; VDD = 3.3V+/-10%; VDDO = 3.3V+/-10%; VDDO = 2.5V+/-10%; VDDO = 1.8V+/-10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
V_{IHDIF}	Input High Voltage - CLK_IN[1]	Differential inputs (single-ended measurement)	600	800	1150	mV
V_{ILDIF}	Input Low Voltage - CLK_IN[1,3]	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV
V_{COM}	Input Common Mode Voltage - CLK_IN[1]	Common Mode Input Voltage	300		725	mV
V_{SWING}	Input Amplitude - CLK_IN[1]	Peak to Peak value (V_{IHDIF} - V_{ILDIF})	300		1450	mV
dv/dt	Input Slew Rate - CLK_IN[1,2]	Measured differentially	0.4			V/ns
I_{IN}	Input Leakage Current[1]	V_{IN} = V_{DD} , V_{IN} = GND	-5		5	uA
d_{tin}	Input Duty Cycle[1]	Measurement from differential wavefrom	45		55	%
J_{DIFIn}	Input Jitter - Cycle to Cycle[1]	Differential Measurement	0		150	ps

Note:
1. Guaranteed by design and characterization, not 100% tested in production.
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven from a single ended clock by driving the true clock and biasing the complement clock input to the VBIAS, where VBIAS is (VIHHIGH - VIHLOW)/2

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

(T_A = -40~85°C; VDD = 3.3V+/-10%; VDDO = 3.3V+/-10%; VDDO = 2.5V+/-10%; VDDO = 1.8V+/-10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
V_{DDX}	Supply Voltage[1]	Supply voltage for core, analog	3.0	3.3	3.6	V
V_{DDO}	Supply Voltage[1]	Supply voltage outputs	2.97	3.3	3.63	V
			2.25	2.5	2.75	
			1.62	1.8	1.98	
T_A	Ambient Operating Temperature[1]		-40	25	85	°C

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions Cont...

Symbol	Parameters	Condition	Min.	Type	Max.	Units
V_{IH}	Input High Voltage[1]	Single-ended inputs, except SMBus, SADR_tri	0.65 V_{DD}		V_{DD} +0.3	V
V_{IM}	Input Mid Voltage[1]	SADR_tri	0.4 V_{DD}		0.6 V_{DD}	V
V_{IL}	Input Low Voltage[1]	Single-ended inputs, except SMBus, SADR_tri	-0.3		0.35 V_{DD}	V
V_{H}	Hysteresis Voltage[1]	V_{T+} - V_{T-}	0.05 V_{DD}		0.2 V_{DD}	V
V_{OH}	Output High Voltage[1]	Single-ended outputs, except SMBus. I_{OH} = -2mA	V_{DD} -0.45			V
V_{OL}	Outputt Low Voltage[1]	Single-ended outputs, except SMBus. I_{OL} = -2mA			0.45	V
I_{IN}	Input Current[1]	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA
I_{INP}		Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA
fin	Input Frequency[1]	Bypass mode	1		400	MHz
		100MHz PLL mode	95	100	105	MHz
Lpin	Pin Inductance[1]				7	nH
C_{IN}	Capacitance[1]	Control Inputs	1.5		5	pF
Cout		Output pin capacitance			6	pF
t_{STAB}	Clock output Stabilization[1, 2]	From V_{DD} Power-Up and after input clock stabilization or de-assertion of CKPWRGD_PD# to 1st clock		0.6	1	ms
f_{MODIN}	Input SS Modulation Frequency[1]	Allowable Frequency (Triangular Modulation)	30	31.500	33	kHz
$t_{LATOE\#}$	OE# Latency[1, 3]	CLK start after OE# assertion CLK stop after OE# deassertion	1		3	clocks
t_{DRVPD}	Tdrive_PD#[1, 3]	CLK output enable after CKPWRGD_PD# de-assertion			300	us
t_{F}	Fall time[1, 2]	Control inputs			5	ns
t_{R}	Rise time[1, 2]	Control inputs			5	ns
V_{ILSMB}	SMBus Input Low Voltage[1]				0.8	V
V_{IHSMB}	SMBus Input High Voltage[1]		2.1		3.6	V

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions Cont...

Symbol	Parameters	Condition	Min.	Type	Max.	Units
V_{OLSMB}	SMBus Output Low Voltage[1]	@ I_{PULLUP}			0.4	V
I_{PULLUP}	SMBus Sink Current[1]	@ V_{OL}	4			mA
V_{DDSMB}	Nominal Bus Voltage[1]	3.3V bus voltage	2.7		3.6	V
t_{RSMB}	SCLK/SDATA Rise Time[1]	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns
t_{FSMB}	SCLK/SDATA Fall Time[1]	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns
f_{MAXSMB}	SMBus Operating Frequency[1, 5]	Maximum SMBus operating frequency			400	kHz

Note:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Control input must be monotonic from 20% to 80% of input swing. Input Frequency Capacitance
3. Time from deassertion until outputs are >200 mV
4. The differential input clock must be running for the SMBus to be active

Electrical Characteristics–CLK 0.7V Low Power HCSL Outputs (T_A = -40~85°C; VDD = 3.3V+/-10%; VDDO = 3.3V+/-10%; VDDO = 2.5V+/-10%; VDDO = 1.8V+/-10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
Trf	Slew rate[1,2,3]	Scope averaging on 2.0V/ns setting @100MHz output	1	2	3	V/ns
		Scope averaging on 3.0V/ns setting @100MHz output	2	3	4.5	V/ns
ΔTrf	Slew rate matching[1,2,4]	Slew rate matching, Scope averaging on		7	20	%
V_{HIGH}	Voltage High[1,7]	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660		880	mV
V_{LOW}	Voltage Low[1,7]		-150		150	mV
Vmax	Max Voltage[1]	Measurement on single ended signal using absolute value. (Scope averaging off)			1150	mV
Vmin	Min Voltage[1]		-300			mV
Vswing	Vswing[1,2,7]	Scope averaging off	300			mV
Vcross_abs	Crossing Voltage (abs)[1,5,7]	Scope averaging off	250		550	mV
Δ-Vcross	Crossing Voltage (var)[1,6]	Scope averaging off			140	mV

Note:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.
4. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
5. Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
6. The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.
7. At default SMBus settings.

Electrical Characteristics–Current Consumption (T_A = -40~85°C; See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
I_{DDAOP}	Operating Supply Current[1]	VDDA+VDDR, PLL Mode, @100MHz, typical value under VDDO = 1.8V		37	45	mA
I_{DDOP}		VDD1.8, All outputs active @100MHz, typical value under VDDO = 1.8V		52	60	mA
I_{DDAPD}	Powerdown Current[1,2]	VDDA+VDDR, PLL Mode, @100MHz			1	mA
I_{DDPD}		VDD1.8, Outputs Low			1.8	mA

Note:
1. Guaranteed by design and characterization, not 100% tested in production.
2. Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characterisitics

(T_A = -40~85°C; VDD = 3.3V+/-10%; VDDO = 3.3V+/-10%; VDDO = 2.5V+/-10%; VDDO = 1.8V+/-10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
t_{DC}	Duty Cycle[1]	Measured differentially, PLL Mode	45		55	%
t_{DCD}	Duty Cycle Distortion[1,3]	Measured differentially, Bypass Mode@100MHz	-1	0	1	%
t_{pdBYP}	Skew, Input to Output[1,4]	Bypass Mode, VT = 50%	2500		4500	ps
t_{pdPLL}		PLL Mode VT = 50%	-250		250	ps
t_{skew}	Skew, Output to Output[1,2]	VT = 50%		25	50	ps
$t_{jcyc-cyc}$	Jitter, Cycle to cycle[1,2]	PLL mode @100MHz output			50	ps
		Additive Jitter in Bypass Mode @100MHz output		0.1	25	ps

Note:
1. Guaranteed by design and characterization, not 100% tested in production.
2. Measured from differential waveform
3. Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
4. All outputs at default slew rate
5. The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

Electrical Characteristics–Phase Jitter Parameters

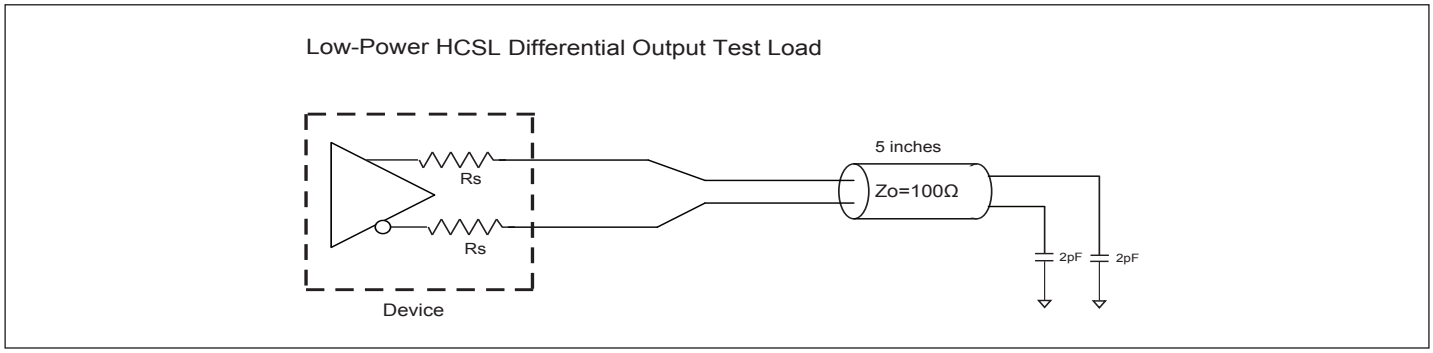
(T_A = -40~85°C; VDD = 3.3V+/-10%; VDDO = 3.3V+/-10%; VDDO = 2.5V+/-10%; VDDO = 1.8V+/-10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	INDUSTRY LIMIT	Units
$t_{jphPCIeG1}$	Phase Jitter, PLL Mode	PCIe Gen 1[1,2,3]		34	86	ps (p-p)
$t_{jphPCIeG2}$		PCIe Gen 2 Low Band 10kHz < f < 1.5MHz[1,2]		0.9	3	ps (rms)
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)[1,2]		2.2	3.1	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)[1,2,4]		0.5	1	ps (rms)
$t_{jphSGMII}$		125MHz, 1.5MHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz[1,6]		1.9	NA	ps (rms)
$t_{jphPCIeG1}$	Additive Phase Jitter, Bypass Mode	PCIe Gen 1[1,2,3]		0.6	N/A	ps (p-p)
$t_{jphPCIeG2}$		PCIe Gen 2 Low Band 10kHz < f < 1.5MHz[1,2,5]		0.1	N/A	ps (rms)
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)[1,2,5]		0.05	N/A	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)[1,2,4,5]		0.05	N/A	ps (rms)
$t_{jphSGMII}$		125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz[1,6]		0.15	N/A	ps (rms)

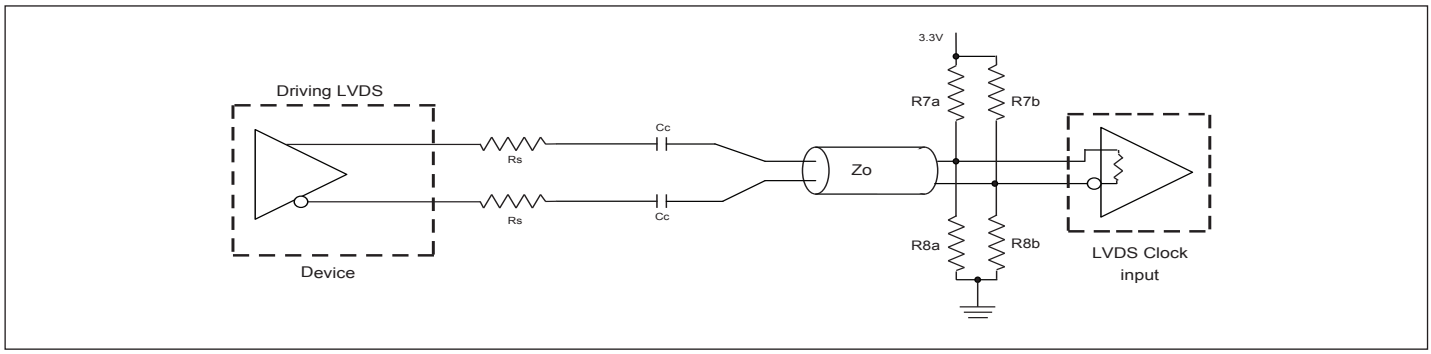
Note:

1. Applies to all outputs, with device driven by a clean clock source.
2. See http://www.pcisig.com for complete specs
3. Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.
4. Subject to final ratification by PCI SIG.
5. For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2]
6. Applies to all differential outputs

Test Loads



Driving LVDS



Driving LVDS inputs with the PI6CDBL401B

Component	Value	
	Receiver has termination	Receiver does not have termination
R7a, R7b	10K Ω	140 Ω
R8a, R8b	5.6K Ω	75 Ω
Cc	0.1 uF	0.1 uF
Vcm	1.2 volts	1.2 volts

Serial Data Interface (SMBus)

This part is a slave only device that supports blocks read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer by issuing STOP.

Address Assignment

Refer to SMBus Address Selection Table.

Data Protocol

(Write)

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr: D4	Ack	Register offset	Ack	Byte Count=N	Ack	Data Byte 0	Ack	…	Data Byte N-1	Ack	Stop bit

(Read)

1 bit	8 bits	1	8 bits	1	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr: D4	Ack	Register offset	Ack	Repeat start	Slave Addr: D5	Ack	Byte Count=N	Ack	Data Byte 0	Ack	…	Data Byte N-1	NOT Ack	Stop bit

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

SMBus Table: Output Enable Register [1]

Byte 0	Name	Control Function	Type	0	1	Default
7	Reserved					1
6	OE3	Output Enable	RW	Low	Enabled	1
5	OE2	Output Enable	RW	Low	Enabled	1
4	Reserved					1
3	OE1	Output Enable	RW	Low	Enabled	1
2	Reserved					1
1	OE0	Output Enable	RW	Low	Enabled	1
0	Reserved					1

1. A low on these bits will overide the OE# pin and force the differential output Low.

SMBus Table: PLL Operating Mode and Output Amplitude Control Register

Byte 1	Name	Control Function	Type	0	1	Default
7	PLL-MODERB1	PLL Mode Readback Bit 1	R	See PLL Operating Mode Table		Latch
6	PLL-MODERB0	PLL Mode Readback Bit 0	R			Latch
5	PLLMODE_SWCNTRL	Enable SW control of PLL Mode	RW	Values in B1[7:6] set PLL Mode	Values in B1[4:3] set PLL Mode	0
4	PLLMODE1	PLL Mode Control Bit 1	RW[1]	See PLL Operating Mode Table		0
3	PLLMODE0	PLL Mode Control Bit 0	RW[1]			0
2	Reserved					1
1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01 = 0.7V	1
0	AMPLITUDE 0		RW	10= 0.8V	11 = 0.9V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
7	Reserved					1
6	SLEWRATE-SEL DIF3	Slew Rate Selection	RW	2 V/ns	3 V/ns	1
5	SLEWRATE-SEL DIF2	Slew Rate Selection	RW	2 V/ns	3 V/ns	1
4	Reserved					1
3	SLEWRATE-SEL DIF1	Slew Rate Selection	RW	2 V/ns	3 V/ns	1
2	Reserved					1

SMBus Table: DIF Slew Rate Control Register Cont...

Byte 2	Name	Control Function	Type	0	1	Default
1	SLEWRATE-SEL DIF0	Slew Rate Selection	RW	2 V/ns	3 V/ns	1
0	Reserved					1

SMBus Table: Frequency Select Control Register

Byte 3	Name	Control Function	Type	0	1	Default
7	Reserved					1
6	Reserved					1
5	Reserved					0
4	Reserved					0
3	Reserved					0
2	Reserved					1
1	Reserved					1
0	Reserved					1

Byte 4 is Reserved and reads back 'hFF

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
7	RID3	Revision ID	R	A rev = 0000		0
6	RID2		R			0
5	RID1		R			0
4	RID0		R			0
3	VID3	VENDOR ID	R			0
2	VID2		R			0
1	VID1		R			0
0	VID0		R			0

SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
7	Device Type1	Device Type	R	00 = FGV, 01 = DBV,		0
6	Device Type0		R	10 = DMV, 11= Reserved		1
5	Device ID5	Device ID	R	000100 binary or 04 hex		0
4	Device ID4		R			0
3	Device ID3		R			0
2	Device ID2		R			1
1	Device ID1		R			0
0	Device ID0		R			0

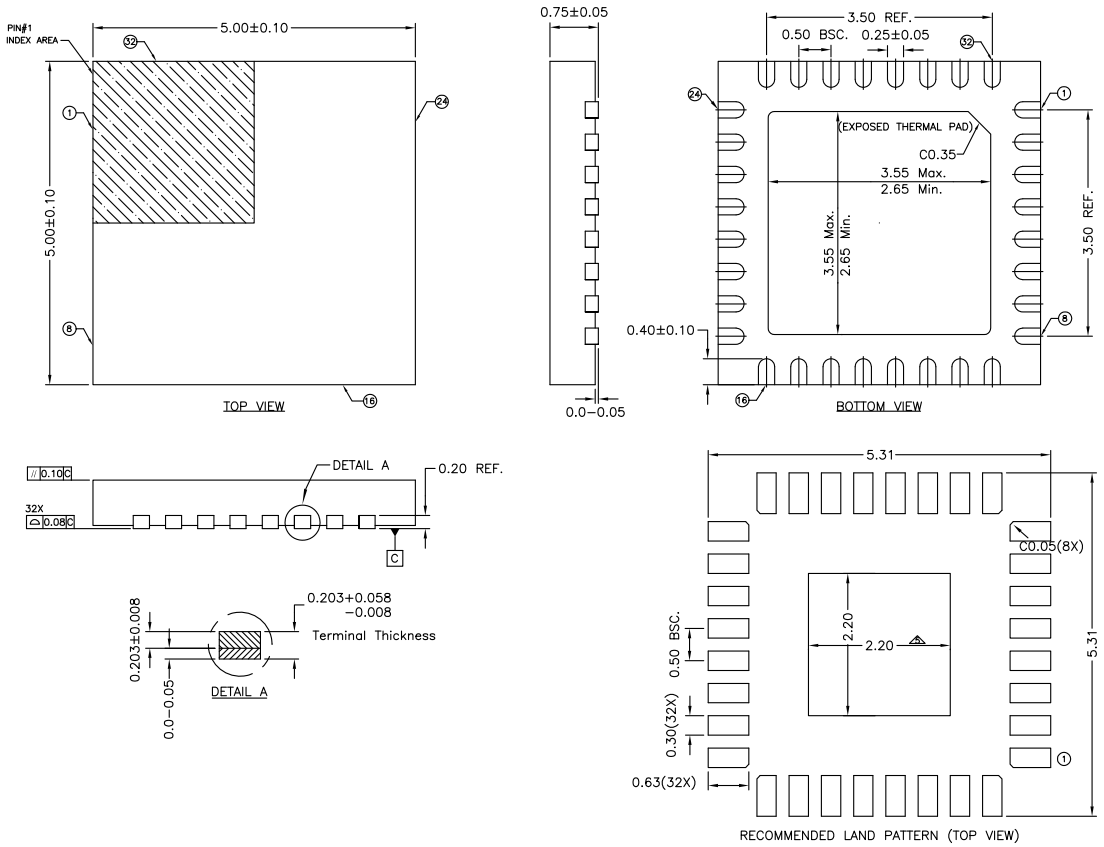
SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
7	Reserved					0
6	Reserved					0
5	Reserved					0
4	Reserved					0
3	Reserved					0
2	Reserved					0
1	Reserved					0
0	Reserved					0

Thermal Characteristics

Symbol	Parameter	Condition	Min.	Type	Max.	Units
θ_{JA}	Thermal Resistance Junction to Ambient	Still air		44.7		°C/W
θ_{JA}	Thermal Resistance Junction to Case			21.7		°C/W

Packaging Mechanical : TQFN (ZH32)



Notes:
1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area (mesh stencile design is recommended)

PERICOM Enabling Serial Connectivity	DATE: 06/30/11
DESCRIPTION: 32-contact, Thin Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZH32	
DOCUMENT CONTROL #: PD-2070	REVISION: B

11-0147

Note: For latest package info, please check: https://www.diodes.com/design/support/packaging/pericom-packaging/

Ordering Information(1-3)

Ordering Code	Package Code	Package Description
PI6CDBL401BZHIEX	ZH	32-contact, Thin Quad Flat No-Lead (TQFN), Tape & Reel

Notes:

1. Thermal characteristics can be found on the company web site at https://www.diodes.com/design/support/packaging/pericom-packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

IMPORTANT NOTICE

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