Signal Integrity

The GT1706/04 is a multi-lane BERT solution designed to operate from 1.25Gbps to 14.5Gbps on each channel.

The GT1706/04 offers many benefits such as plug and play - hard-wired blocks providing industry standard patterns, single bit counting error checker and 3D eye monitor, FracN PLL enabling
wide data rate range and a small footprint. This high integration enables low-cost production of BERT solutions.

Overview

Features

- A BERT chip solution with up to twelve inputs and outputs, designed to operate from 1.25Gbps to 14.5Gbps
- PRBS Generator and Checker

1. Supports PRBS7, PRBS9, PRBS11, PRBS15, PRBS23 & PRBS31 and custom patterns
2. PRBS checker allows for single bit error checking for precise bit error rate measurements

- FracN PLL allows all channels to run independent data rates using one reference clock with a 20-bit resolution
- Accepts up to two input reference clocks

- Front-end linear input equalization
- 3D Eye Monitor on each input to allow advanced measurements such as BER contours and eye parameters
- Multi-tap output de-emphasis
- Programmable output swing
- Programmable Input CDR Loop bandwidth
- I2C control
- Low power dissipation: 3.5W typical @ 10.3125Gbps
- 0.9V core supply; 1.8V I/O supply
- 13mm x 13mm BGA package

Applications

- HD/3G/4K/8K Video Broadcast testing
- Fibre Channel/Infiniband/Ethernet Link Testing
- General purpose lab tester
- Functional and Production BERT developments

Packaging

GT1706-IBE3 | 144-ball FcBGA | 0°C to +70°C
GT1704-IBE3 |144-ball FcBGA | 0°C to +70°C