

RH850 Evaluation Platform



RH850/X1x Network MainBoard

32

Y-RH850-X1X-MB-T2-V1

Y-RH850-X1X-MB-T2-V2

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Chapter 1 Introduction

The RH850/X1x Network Mainboard serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/X1x microcontrollers. The Network Main Board (Y-RH850-X1X-MB-T2-V1) is used in conjunction with one of several PiggyBoards (e.g. Y-RH850-F1X-176PIN-PB-T1-V2).

Features:

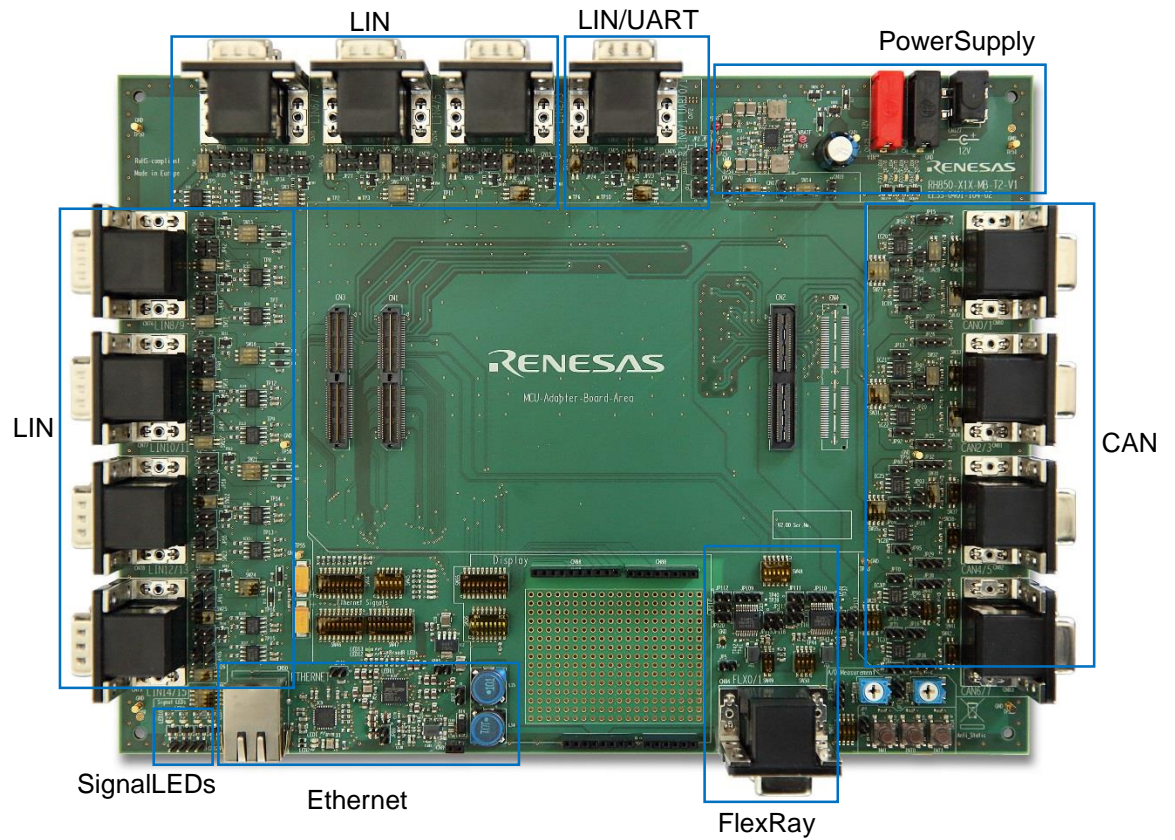
- User interaction through switches, buttons and LEDs
- 16 LIN interfaces
- 8 CAN interfaces (ready for CAN-FD)
- 2 UART interfaces
- Dual FlexRay interface
- Ethernet interface, usable with RJ45 or BroadR-Reach™ drivers
- High density PiggyBoard connectors
- Display interface
- Single 12V board power supply with onboard voltage regulators
- Through-hole prototyping area

This document will describe the functionality provided by the Application Board and guide the user through its operation. For details regarding the operation of the microcontroller, refer to the RH850/X1x User Manual.

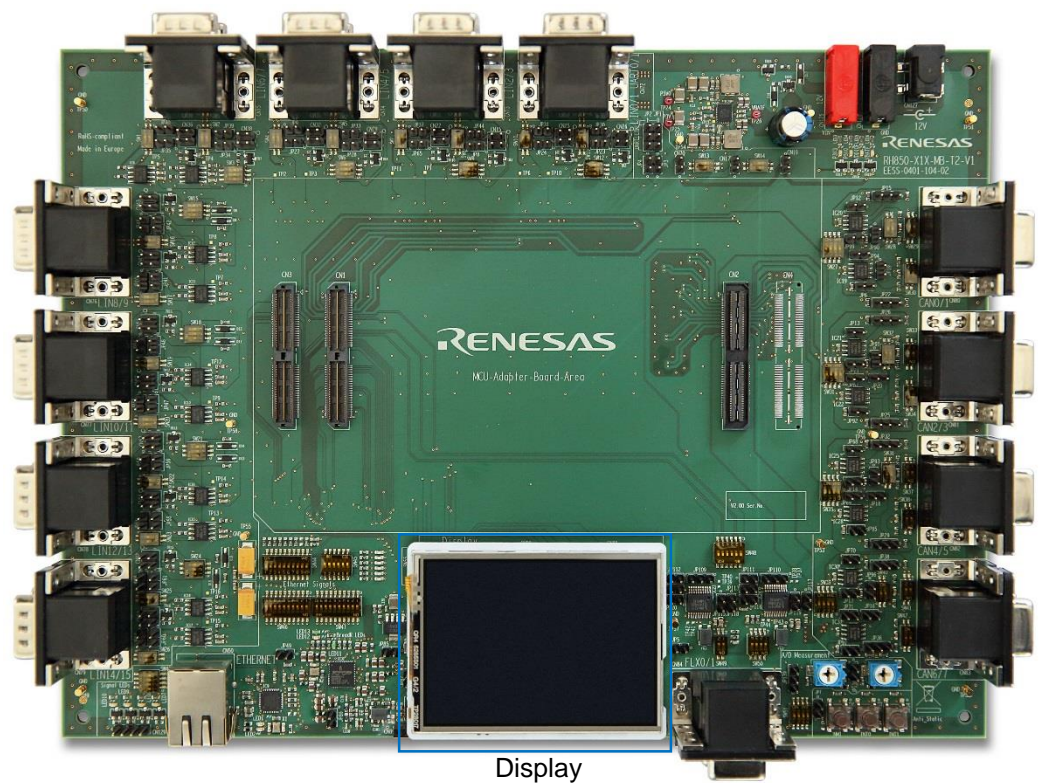
1.1 Board Overview

The figures below provide a view of the two Network Main Board versions:

Y-RH850-X1X-MB-T2-V1: Network Main Board without TFT display



Y-RH850-X1X-MB-T2-V2: Network Main Board including TFT display



Chapter 2 Power Supply

A voltage of 12V (typ) must be supplied to the board. The required voltages for operation of the onboard modules (3.3V and 5.0V) are derived from this voltage by dedicated voltage regulators.

Details of the board power supply are described in the chapters below.

2.1 Power connectors

The board operation voltage is supplied to the board by the following connectors:

Table 2-1

Connector	Description	Function
CN125	4mm red laboratory connector	12V supply
CN126	4mm black laboratory connector	VSS/GND supply
CN127	2.1mm coaxial connector	12 V & VSS/GND supply:: Tip: 12V Barrel: VSS/GND

A blue LED (LED6) signals the availability of the 12V board supply voltage.

Caution:

Do not supply different voltages to CN125 and CN127 simultaneously.

2.2 Voltage Regulators

A DC/DC regulator is implemented for generation of 1.2V, 3.3V and 5.0V for use by device modules. Blue LEDs will signal the availability of the voltages.

Table 2-2

Voltage	Signal LED
+5.0V (typical)	LED4
+3.3V (typical)	LED3, LED5
+1.2V (typical)	-

2.3 Other voltages

2.3.1 IO voltage

For some of the board modules, it is possible to input a dedicated IO voltage different from the module supply voltage.

This IO voltage (named VDDIOF) is not generated on the MainBoard, but must be set on the PiggyBoard. Still, availability of the voltage is signaled by the blue LED5.

Refer to the documentation of the PiggyBoard on how to set the IO voltage.

2.3.2 Module supply voltage

The supply voltage of each module must be set by jumper. Refer to the description of each module within this document for details.

For some modules the signal voltage level is defined by its supply voltage, e.g. 3.3V for Ethernet. Therefore the related port voltage of the device on the PiggyBoard must be configured for the same voltage level as the module's supply voltage.

2.3.3 Miscellaneous settings

The supply voltage of the microcontroller device on the PiggyBoard is derived from the output of the two DC/DC regulators on the MainBoard. The selection on which voltage the device will operate from, must be done on the PiggyBoard. Therefore, refer to the documentation of the PiggyBoard voltage supply for details.

Chapter 3 Board functions

This section describes functions and modules that are available on the MainBoard.

Cautions:

- a) Take notice that the usage of each function depends on its availability on the mounted PiggyBoard/Device.
- b) Also notice that simultaneous usage of multiple functions depends on the alternative function sharing of the device and applied function selection by the PiggyBoard.

Refer to the documentation of the used PiggyBoard for details.

3.1 UART Interface

Two UART interfaces, with RS232 signal level drivers are provided on the board.

To connect the UART signals of the device available on CN1 (PiggyBoard device connector) to the UART transceivers, close SW14 for UART0 and SW13 for UART1.

In case different device signals shall be connected to the UART transceivers, the headers CN17 (for UART0) and CN70 (for UART1) can be used. Connect a small wire between the related signals of the device on the PiggyBoard and the UART transceiver.

To supply the voltage for the UART transceiver (MAX3222), the pin header CN19 must be closed.

To enable an on-board loop of UART0 to UART1, the switch JP3 and JP4 can be closed.

The table 3-1 shows the signal mapping of the UART DSUB connectors:

Table 3-1

DSUB Connector	UART Interface	Pin Number	Function
CN72 Lower	UART0	2	Tx (T1OUT)
		3	Rx (R1IN)
		5	GND
		Others	-
CN72 Upper	UART1	2	Tx (T2OUT)
		3	Rx(R2IN)
		5	GND
		Others	-

3.2 LIN Interface

Sixteen LIN interfaces with LIN signal level are provided on the board. They are named LIN0 to LIN15.

For operation of the LIN interfaces jumpers and switches described in the table below need to be closed.

To connect the LIN signals of the device available on CN1 and CN2 (PiggyBoard device connector) to the LIN drivers of this MainBoard, the switches of the column 'LIN signal connectors to PiggyBoard' need to be closed.

In case other device signals than the ones of CN1 or CN2 shall be connected to the LIN drivers, the headers of the column 'Alternative LIN signal connectors' in the table below can be used. Connect a small wire between the related signals of the device on the PiggyBoard and those headers.

The IO voltage of the LIN driver (TJA1020T) must be set by closing the jumpers in column 'Supply voltage pin header'.

To enable an on-board loop of LIN_n to LIN_{n+1} (n=0,2,4...) the switches of column 'On-board loop switches' can be closed.

Several pin headers are provided to configure the inputs of the LIN driver (TJA1020T), e.g. NSLP and NWAKE. For details refer to the schematic and the reference documentation of the LIN driver.

LIN Interface	LIN signal connectors to PiggyBoard	Alternative LIN signal connectors	Supply voltage pin header	On-board loop switches	LIN driver configuration
LIN0	SW10	JP24	JP31	SW12	CN25
LIN1	SW11	JP23	JP30		CN26
LIN2	SW8	JP8	JP44	SW9	CN15
LIN3	SW7	JP65	JP37		CN22
LIN4	SW5	JP28	JP33	SW6	CN29
LIN5	SW4	JP27	JP9		CN32
LIN6	SW1	JP35	JP40	SW3	CN36
LIN7	SW2	JP34	JP39		CN38
LIN8	SW16	JP42	JP46	SW15	CN43
LIN9	SW17	JP41	JP10		CN45
LIN10	SW19	JP48	JP54	SW18	CN51
LIN11	SW20	JP47	JP53		CN52
LIN12	SW22	JP56	JP59	SW21	CN57
LIN13	SW23	JP55	JP11		CN58
LIN14	SW25	JP61	JP66	SW24	CN62
LIN15	SW26	JP60	JP64		CN63

This table 3-2 shows the signal mapping of the LIN signals on the DSUB connectors:

Table 3-2

LIN Interface	DSUB connector	LIN/UART signal selection
LIN0	CN72, lower	LIN: Pin3 GND: Pin 3, 5
LIN1	CN72, upper	LIN: Pin3 GND: Pin 3, 5
LIN2	CN73, lower	LIN: Pin3 GND: Pin 3, 5
LIN3	CN73, upper	LIN: Pin3 GND: Pin 3, 5

LIN4	CN74, lower	LIN: Pin3 GND: Pin 3, 5
LIN5	CN74, upper	LIN: Pin3 GND: Pin 3, 5
LIN6	CN75, lower	LIN: Pin3 GND: Pin 3, 5
LIN7	CN75, upper	LIN: Pin3 GND: Pin 3, 5
LIN8	CN76, lower	LIN: Pin3 GND: Pin 3, 5
LIN9	CN76, upper	LIN: Pin3 GND: Pin 3, 5
LIN10	CN77, lower	LIN: Pin3 GND: Pin 3, 5
LIN11	CN77, upper	LIN: Pin3 GND: Pin 3, 5
LIN12	CN78, lower	LIN: Pin3 GND: Pin 3, 5
LIN13	CN78, upper	LIN: Pin3 GND: Pin 3, 5
LIN14	CN79, lower	LIN: Pin3 GND: Pin 3, 5
LIN15	CN79, upper	LIN: Pin3 GND: Pin 3, 5

3.3 CAN Interface

Eight CAN interfaces with CAN signal levels are provided on the board. They are named CAN0 to CAN7.

For operation of the CAN interfaces jumpers and switches described in the table below need to be closed.

To connect the CAN signals of the device available on CN1 and CN2 (PiggyBoard device connector) to the CAN drivers of this MainBoard, the switches of the column 'CAN signal connectors to PiggyBoard' need to be closed.

In case other device signals than the ones of CN1 or CN2 shall be connected to the CAN drivers, the headers of the column 'Alternative CAN signal connectors' in the table below can be used. Connect a small wire between the related signals of the device on the PiggyBoard and those headers.

The supply voltage of the CAN transceiver must be set by closing the jumpers shown in the column 'Supply voltage pin header'.
For boards equipped with the CAN driver TJA100GT the transceiver supply voltage also sets their IO voltage. Take care that the related port voltages of the device on the mounted PiggyBoard is set to the same voltage level.
For boards equipped with the CAN transceiver ATA6561 its IO voltage level can be set by the jumpers shown in the column 'IO supply voltage pin header'.

To enable an on-board loop of CAN_n to CAN_{n+1} (n=0,2,4...) the switches of column 'On-board loop switches' can be closed.

Several pin headers are provided to configure the inputs of the CAN driver, e.g. STB. For details refer to the schematic and the reference documentation of the CAN driver.

CAN Interface	CAN signal connectors to PiggyBoard	Alternative CAN signal connectors	Supply voltage pin header	IO supply voltage pin header	On-board loop switches	CAN driver configuration
CAN0	SW27.1, SW27.2	JP94	JP19	JP6	SW30	STB: JP22 Pin5: JP6
CAN1	SW27.3, SW27.4	JP12	JP99	JP90		STB: JP15 Pin5: JP90
CAN2	SW31.1, SW31.2	JP13	JP21	JP91	SW34	STB: JP26 Pin5: JP91
CAN3	SW31.3, SW31.4	JP67	JP20	JP92		STB: JP25 Pin5: JP92
CAN4	SW35.1, SW31.2	JP68	JP14	JP93	SW36	STB: JP32 Pin5: JP93
CAN5	SW35.3, SW31.4	JP69	JP18	JP95		STB: JP29 Pin5: JP95
CAN6	SW39.1, SW31.2	JP70	JP17	JP96	SW40	STB: JP38 Pin5: JP96
CAN7	SW39.3, SW31.4	JP71	JP16	JP97		STB: JP36 Pin5: JP97

The table 3-3 shows the signal mapping of the two DSUB connectors:

Table 3-3

CAN Interface	DSUB connector	LIN/UART signal selection
CAN0	CN80, lower	CANH: Pin7, CANL: PIN2 GND: Pin 3
CAN1	CN80, upper	CANH: Pin7, CANL: PIN2 GND: Pin 3
CAN2	CN81, lower	CANH: Pin7, CANL: PIN2 GND: Pin 3
CAN3	CN81, upper	CANH: Pin7, CANL: PIN2 GND: Pin 3
CAN4	CN82, lower	CANH: Pin7, CANL: PIN2 GND: Pin 3
CAN5	CN82, upper	CANH: Pin7, CANL: PIN2 GND: Pin 3
CAN6	CN83, lower	CANH: Pin7, CANL: PIN2 GND: Pin 3
CAN7	CN83, upper	CANH: Pin7, CANL: PIN2 GND: Pin 3

3.4 FlexRay Interface

Two FlexRay interfaces with FlexRay signal level are provided on the board. They are named FLEX0 to FLEX1.

For operation of the FlexRay interfaces jumpers and switches described in the table below need to be closed.

To connect the FlexRay signals of the device available on CN1 (PiggyBoard device connector) to the FlexRay drivers of this MainBoard, the switches of the column 'FlexRay signal connectors to PiggyBoard' need to be closed.

In case other device signals than the ones of CN1 shall be connected to the FlexRay drivers, the headers of the column 'Alternative FlexRay signal connectors' in the table below can be used. Connect a small wire between the related signals of the device on the PiggyBoard and those headers.

The IO voltage of the FlexRay driver (TJA1080) must be set by closing the jumpers in column 'Supply voltage pin header'.

To enable an on-board loop of FLEX0 to FLEX1 the switches of column 'On-board loop switches' can be closed.

Several pin headers are provided to configure the inputs of the FlexRay driver, e.g. STBN. The related jumpers are described in the column 'FlexRay driver configuration'. For further details refer to the schematic and the reference documentation of the FlexRay driver.

FlexRay Interface	FlexRay signal connectors to PiggyBoard	Alternative FlexRay signal connectors	Supply voltage pin header	On-board loop switches	FlexRay driver configuration	Bus pull-down
FLEX0	SW48.1-12 SW48.2-11 SW48.3-10	JP110	JP111	SW50.3-6 SW50.4-5	EN: JP117 STBN: JP113 BGE: JP116 WAKE: JP119	SW50.1-8 SW50.2-7
FLEX1	SW48.4-9 SW48.5-8 SW48.6-7	JP109	JP112		EN: JP118 STBN: JP115 BGE: JP114 WAKE: JP120	SW49.1-4 SW49.2-3

This table 3-4 shows the signal mapping of the two DSUB connectors:

Table 3-4

DSUB Connector	FlexRay Interface	Pin Number	Function
CN84 Lower	FLEX0	2	FLEX0_BM
		4	FLEX1_BM
		7	FLEX0_BP
		8	FLEX1_BP
		Others	-
CN84 Upper	FLEX1	2	FLEX1_BM
		7	FLEX1_BP
		Others	-

3.5 Ethernet interface

One Ethernet interface that can be configured either as twisted pair (10Base-T/100Base-TX) signal levels or as BroadR-Reach™ signal level is available on the board.

3.5.1 Ethernet over twisted pair signal level

To connect the MII Ethernet signals of the device available on CN1 (PiggyBoard device connector), to the twisted pair 10Base-T/100Base-TX interface, close SW46 and SW47.

To enable the 3.3V power for operation of the twisted pair Ethernet Phy (LAN8700), close the header JP49.

Caution:

The ports of the device on the PiggyBoard that hold the Ethernet signals must also be configured for 3.3V operation. Check the UM of the PiggyBoard for details.

The RJ45 connector CN50 is used for connection of the Ethernet cable. For available signals on the RJ45 connector, refer to the related chapter of the schematic.

3.5.2 BroadR-Reach™ Interface

One Ethernet interface, with BroadR-Reach™ signal level, is provided on the board.

To connect the MII Ethernet signals of the device available on CN1 (PiggyBoard device connector), to the BroadR-Reach™ interface, close all switches on SW44 and SW45.

To enable the 3.3V power for operation of the BroadR-Reach™ Phy (BCM89810), close the header JP85.

Caution:

The ports of the device on the PiggyBoard that hold the Ethernet signals must also be configured for 3.3V operation. Check the UM of the PiggyBoard for details.

To enable the 1.2V power for operation of the BroadR-Reach™ Phy (BCM89810), close the header JP86.

The pin header CN89 is used for connection of the Ethernet cable.

CN89.1: TRD0_P (positive BroadR-Reach™ signal)
CN89.2: TRD0_N (negative BroadR-Reach™ signal)

3.6 Push Buttons

To trigger user actions as device interrupts, three push button are available. The push buttons can trigger the following interrupts:

- SW52: Triggers NMI
- SW53: Triggers INT0
- SW54: Triggers INT1

To connect the interrupt signals of the device available on CN1 (PiggyBoard device connector) to the push buttons, close SW51.

To supply the IO voltage for the push buttons, the pin header JP7 must be closed.

In case different device signals shall be connected to the push buttons, the headers JP139 can be used. Connect a small wire between the related signals of the device on the PiggyBoard and the push buttons drivers.

Table 3-8

Push button	Default signal on CN1	Switch to enable the default connection	Header for alternative connection
SW52	NMI	SW51.1-8	JP139.1
SW53	INT0	SW51.2-7	JP139.2
SW54	INT1	SW51.3-6	JP139.3

3.7 Analog measurements

In order to perform some sample measurement with the PiggyBoard device Analog/Digital Converter, three potentiometers are provided.

To supply the IO voltage for the potentiometers and the multiplexer, the pin header JP138 must be closed.

3.8 Signal LEDs

Four LEDs, LED7 to LED10, are provided to allow visual observation of microcontroller output port states.

The power supply of the LEDs is derived directly from the primary board supply voltage (typical 12V).

To connect the signals of the device available at CN1 (PiggyBoard device connector) to the LEDs, close the switches on SW43 (see table below).

In case different device signals shall be connected to the signal LEDs, the headers CN129 can be used. Connect a small wire between the related signals of the device on the PiggyBoard and the signal LEDs. See the table below for details.

Table 3-11

LED	Switch SW43	Alternative signal connection	CN1 signal
LED10	1-8	CN129.1	DIGIO_0
LED9	2-7	CN129.2	DIGIO_1
LED8	3-6	CN129.3	DIGIO_2
LED7	4-5	CN129.4	DIGIO_3

3.9 LCD Interface

An interface is provided to for the purpose of connecting a graphics LCD to the mainboard.

Related signals can be found on the connectors CN88, CN98, CN100 and CN101

To connect the signals of the device available at CN1 (PiggyBoard device connector) to the Display, close the switches on SW55 and SW56.

The power supply of the display be selected by closing the pin headers JP5 or JP87.

Connector and pin	Display function	CN1/CN3 signal	Device pin / -function
CN88.5	Display SD Card CS	CN3_10 PWM9	P9_1 CSIH2CSS1
CN88.6	Display Controller ChipSelect	CN3_21 PWM20	P9_2 CSIH2CSS2
CN88.7	Display Controller RW Control	CN3_26 PWM25	P11_0 Digital I/O
CN88.8		CN3_39 PWM38	P8_7 Digital I/O
CN98.1		CN3_22	P9_3

		PWM21	CSIH2CSS3
CN98.2		CN3_26 PWM25	P11_0 Digital I/O
CN98.3		CN3_21 PWM20	P9_2 CSIH2CSS2
CN98.4	Display Controller MOSI	CN3_28 PWM27	P11_2 CSIH2SO
CN98.5	Display Controller MISO	CN3_30 PWM29	P11_4 CSIH2SI
CN98.6	Display Controller SCK	CN3_29 PWM28	P11_3 CSIH2SC
CN100.1	Touch Y- Input	CN1_109 ADC2	ADC2
CN100.2	Touch X- Input	CN1_110 ADC3	ADC3
CN100.3	Touch Y+ Input	CN1_111 ADC4	ADC4
CN100.4	Touch X+ Input	CN1_112 ADC5	ADC5
CN100.5		CN1_25 IIC0SDA	P10_2 IIC0SDA
CN100.6		CN1_23 IIC0SCL	P10_3 IIC0SCL
CN101.2	GND	-	
CN101.3	GND	-	
CN101.4		-	
CN101.5	Reset	CN1_89 DIGIO_4	P8_4 Digital I/O
CN101.6		-	

For technical details of the supplied LCD, please visit the following support website:

http://linksprite.com/wiki/index.php5?title=Touch_LCD_Shield

Chapter 4 Revision History

The table provides information about the major changes of the document versions.

Date	Version	Description
2015-07-15	1.0	Initial version
2016-03-30	1.10	<ul style="list-style-type: none">• Added CAN6 and CAN7 to CN2 (appendix B)• Corrected DSUB naming for UART channels in Table 3-1• Corrected LIN channel assignment on DSUB connectors in Table 3-2• Corrected CAN channel assignment on DSUB connectors in Table 3-3• Corrected Ethernet signal assignment on CN1 in Appendix A

Chapter 5 Appendix A: PiggyBoard connector CN1

Pin	Function	Pin	Function
1	VDDA	2	VDDA
3	VDDA	4	VDDA
5	RESET	6	NMI
7	WAKE	8	-
9	INT0	10	INT1
11	INT2	12	INT3
13	-	14	-
15	UART0TX	16	UART1TX
17	UART0RX	18	UART1RX
19	LIN0TX	20	LIN1TX
21	LIN0RX	22	LIN1RX
23	IIC0SDL	24	IIC1SDL
25	IIC0SDA	26	IIC1SDA
27	CAN0TX	28	CAN1TX
29	CAN0RX	30	CAN1RX
31	SENTIN0	32	SENTIN1
33	SENTOUT0	34	SENTOUT1
35	PSI50Rx	36	PSI51Rx
37	PSI50Tx	38	PSI51Tx
39	PSI50Ssync	40	PSI51Sync
41	FLX0TX	42	FLX0EN
43	FLX0RX	44	-
45	FLX1TX	46	FX1EN
47	FLX1RX	48	FLX reserved
49	-	50	-
51	ETH0MDIO	52	ETH0MDC
53	ETH0RXD0	54	EH0TXD0
55	ETH0RXD1	56	EH0TXD1
57	ETH0RXD2	58	EH0TXD2
59	ETH0RXD3	60	EH0TXD3
61	ETH0RXDCLK	62	ETH0TXCLK
63	ETH0RXER	64	ETH0TXER
65	ETH0CRSDV	66	ETH0TXEN
67	ETH0RXDV	68	ETH0COL
69	ETH0RESET	70	ETH0LINK
71	-	72	-
73	USB0UDMF	74	USB0UDMH
75	USB0UDPF	76	USB0UDPH
77	-	78	-

79	-	80	-
81	-	82	-
83	-	84	-
85	DIGIO_0	86	DIGIO_1
87	DIGIO_2	88	DIGIO_3
89	DIGIO_4	90	DIGIO_5
91	DIGIO_6	92	DIGIO_7
93	DIGIO_8	94	DIGIO_9
95	DIGIO_10	96	DIGIO_11
97	DIGIO_12	98	DIGIO_13
99	DIGIO_14	100	DIGIO_15
101	-	102	-
103	MUX0	104	MUX1
105	MUX2	106	-
107	ADC0	108	ADC1
109	ADC2	110	ADC3
111	ADC4	112	ADC5
113	ADC6	114	ADC7
115	IOVDD	116	IOVDD
117	VDDDB	118	VDDDB
119	VDDDB	120	VDDDB

Chapter 6 Appendix B: PiggyBoard connector CN2

Pin	Function	Pin	Function
1	CAN2Tx	2	CAN3Tx
3	CAN2Rx	4	CAN3Rx
5	CAN4Tx	6	CAN5Tx
7	CAN4Rx	8	CAN5Rx
9	LIN2Tx	10	LIN3Tx
11	LIN2Rx	12	LIN3Rx
13	LIN4Tx	14	LIN5Tx
15	LIN4Rx	16	LIN5Rx
17	LIN6Tx	18	LIN7Tx
19	LIN6Rx	20	LIN7Rx
21	LIN8Tx	22	LIN9Tx
23	LIN8Rx	24	LIN9Rx
25	LIN10Tx	26	LIN11Tx
27	LIN10Rx	28	LIN11Rx
29	LIN12Tx	30	LIN13Tx
31	LIN12Rx	32	LIN13Rx
33	LIN14Tx	34	LIN15Tx
35	LIN14Rx	36	LIN15Rx
37	-	38	-
39	-	40	-
41	MLBCLK	42	MLBRESET
43	MLBSIG	44	MLBDAT
45	-	46	-
47	CAN6Tx	48	CAN7Tx
49	CAN6Rx	50	CAN7Rx
51	-	52	-
53	-	54	-
55	-	56	-
57	-	58	-
59	-	60	-
61	-	62	-
63	-	64	-
65	-	66	-
67	-	68	-
69	-	70	-
71	-	72	-
73	-	74	-
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77	-	78	-

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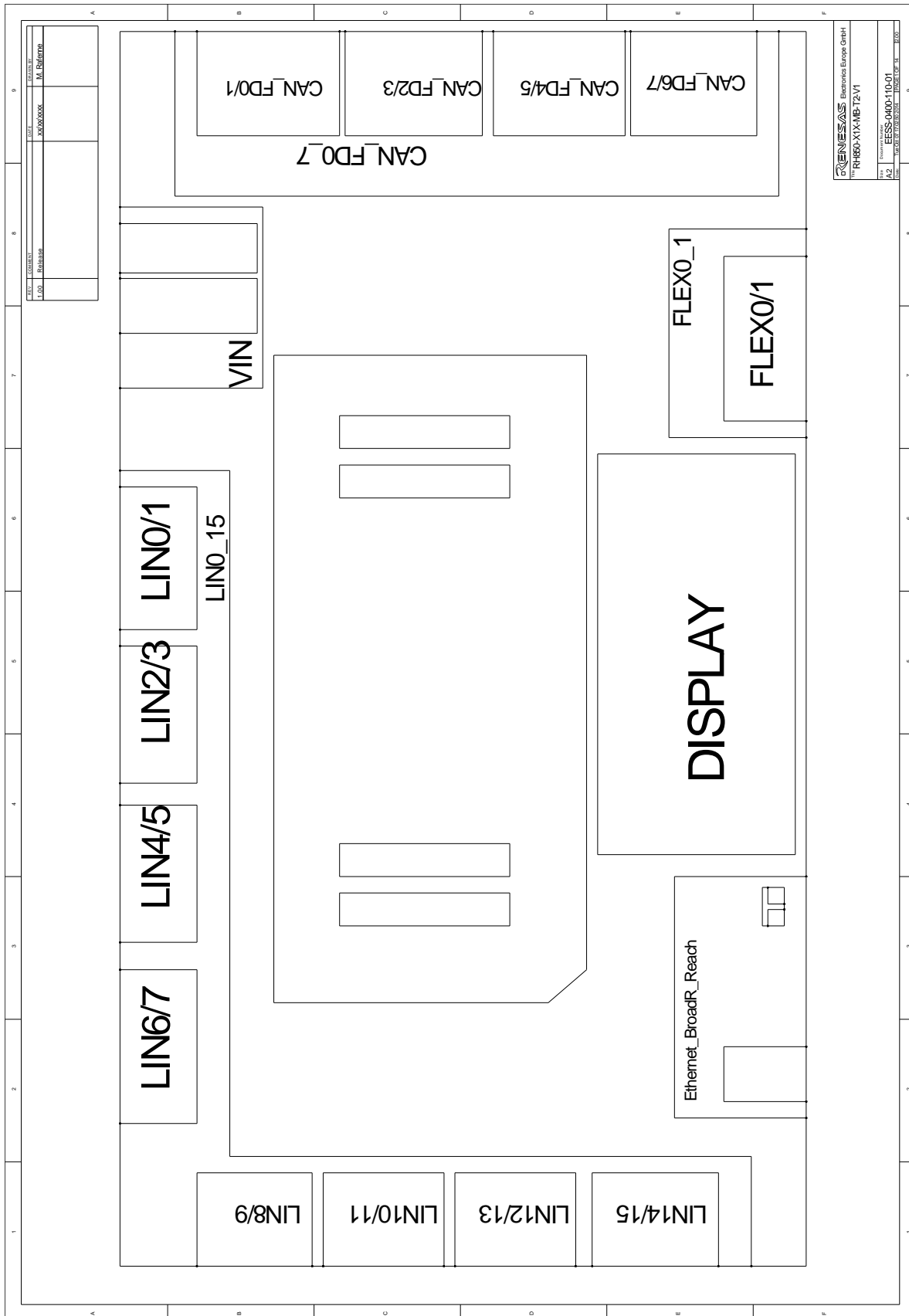
Chapter 7 Appendix C: PiggyBoard connector CN3

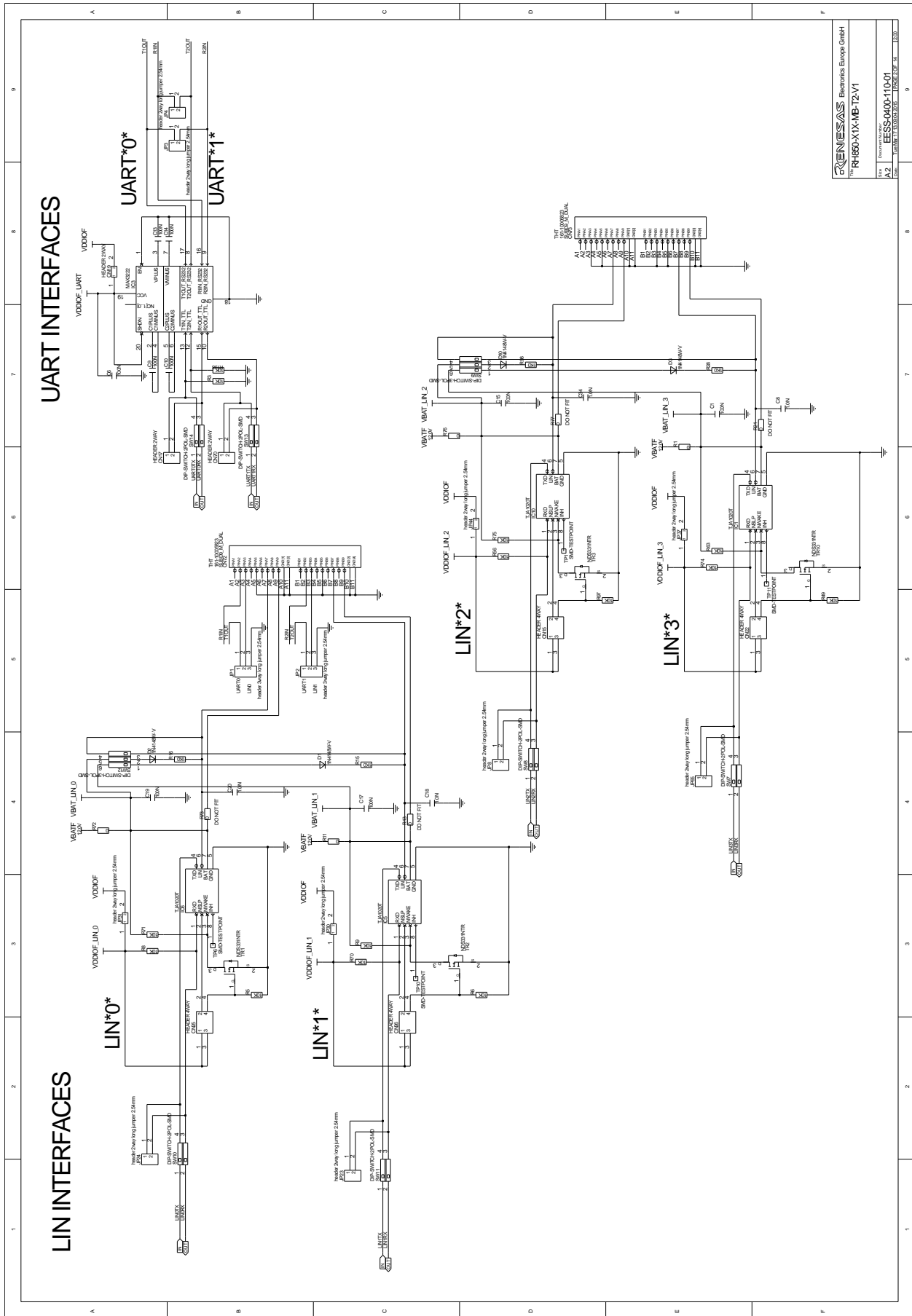
Pin	Function	Pin	Function
1	PWM00	2	PWM01
3	PWM02	4	PWM03
5	PWM04	6	PWM05
7	PWM06	8	PWM07
9	PWM08	10	PWM09
11	PWM10	12	PWM11
13	PWM12	14	PWM13
15	PWM14	16	PWM15
17	PWM16	18	PWM17
19	PWM18	20	PWM19
21	PWM20	22	PWM21
23	PWM22	24	PWM23
25	PWM24	26	PWM25
27	PWM26	28	PWM27
29	PWM28	30	PWM29
31	PWM30	32	PWM31
33	PWM32	34	PWM33
35	PWM34	36	PWM35
37	PWM36	38	PWM37
39	PWM38	40	PWM39
41	PWM40	42	PWM41
43	PWM42	44	PWM43
45	PWM44	46	PWM45
47	PWM46	48	PWM47
49	PWM48	50	PWM49
51	PWM50	52	PWM51
53	PWM52	54	PWM53
55	PWM54	56	PWM55
57	PWM56	58	PWM57
59	PWM58	60	PWM59
61	PWM60	62	PWM61
63	PWM62	64	PWM63
65	PWM64	66	PWM65
67	PWM66	68	PWM67
69	PWM68	70	PWM69
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75	PWM74	76	PWM75
77	PWM76	78	PWM77

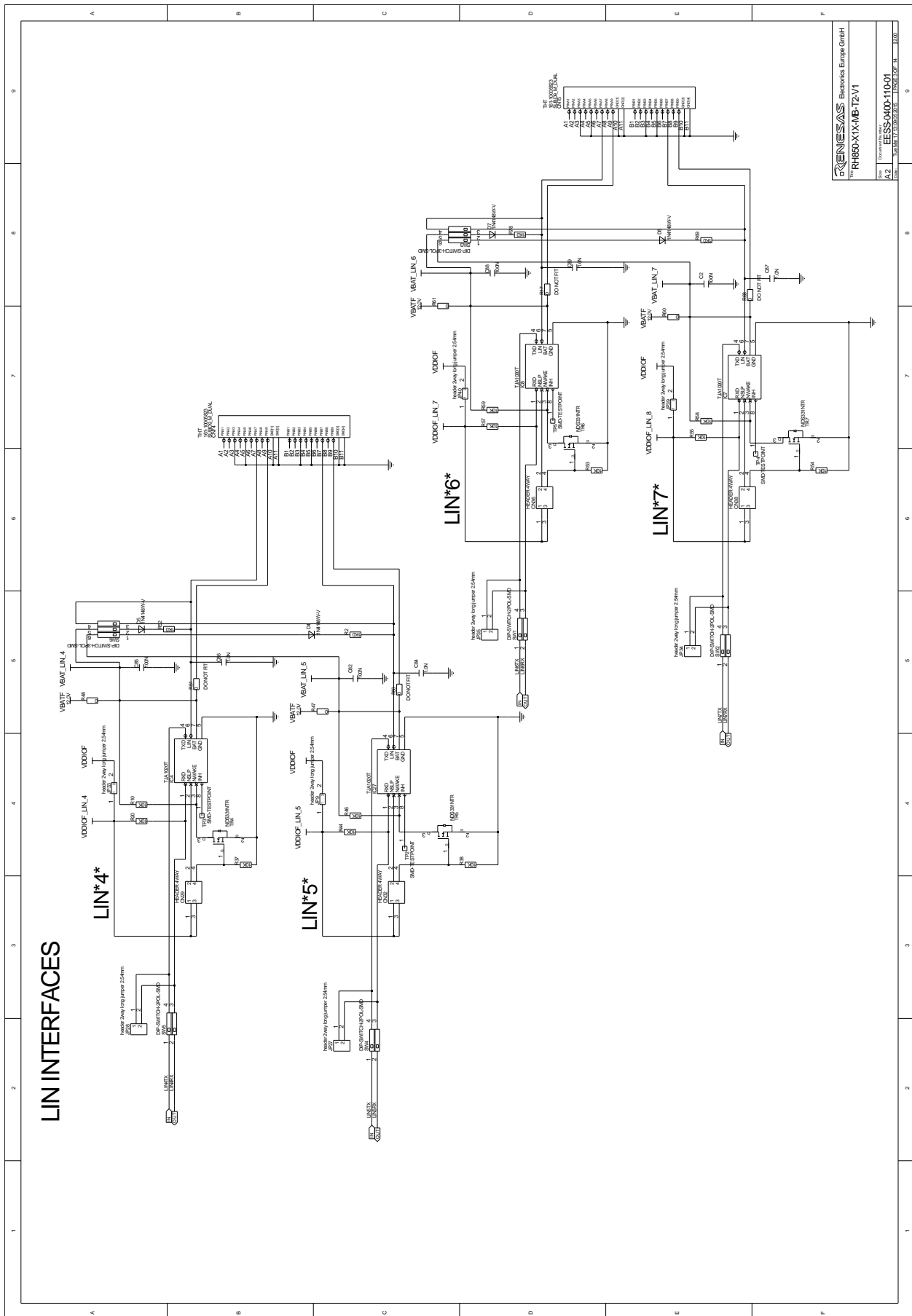
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87	PWMADC06	88	PWMADC07
89	PWMADC08	90	PWMADC09
91	PWMADC10	92	PWMADC11
93	PWMADC12	94	PWMADC13
95	PWMADC14	96	PWMADC15
97	-	98	-
99	-	100	-
101	-	102	-
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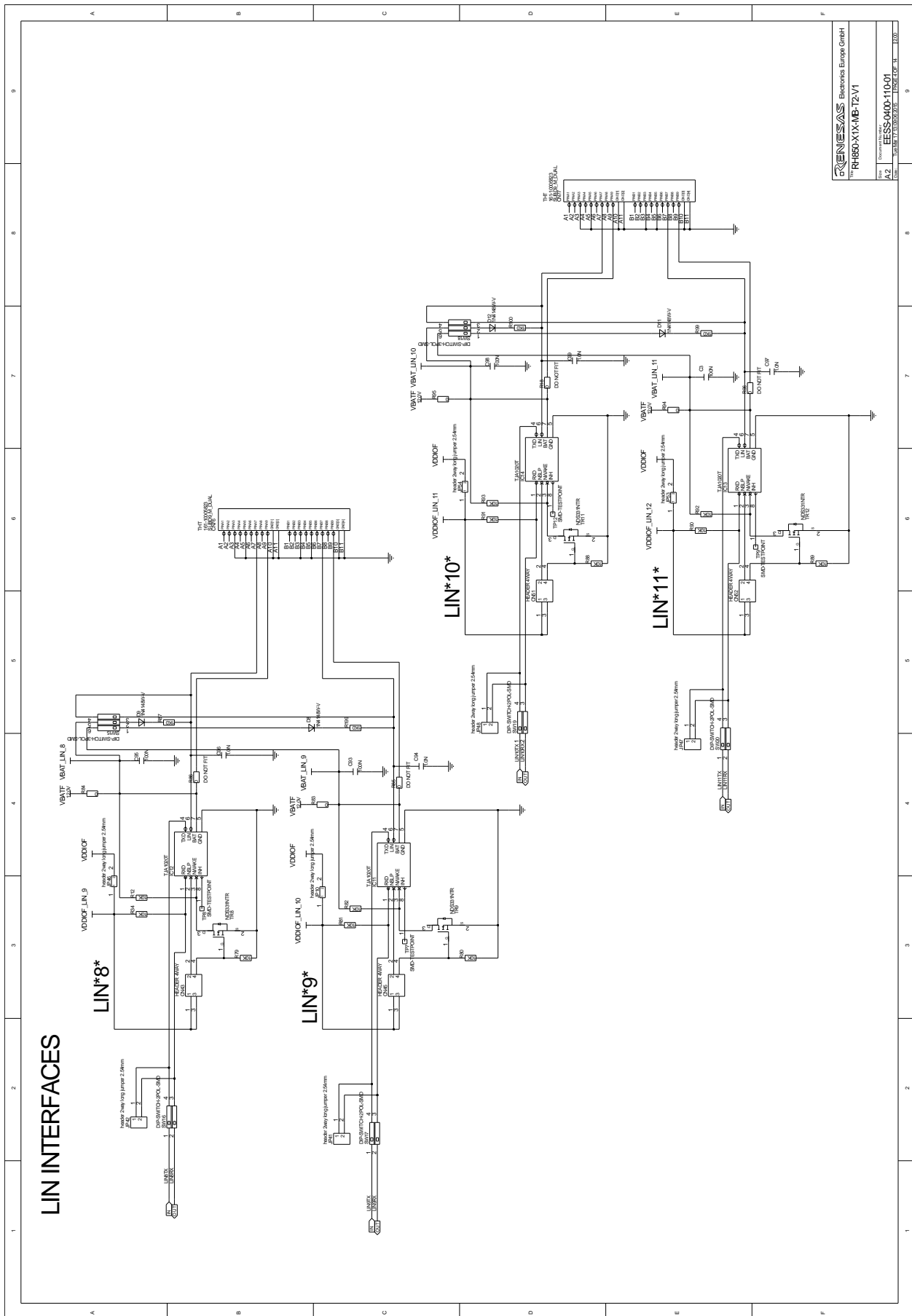
Chapter 8 Appendix D: Schematic

8.1 Version 1

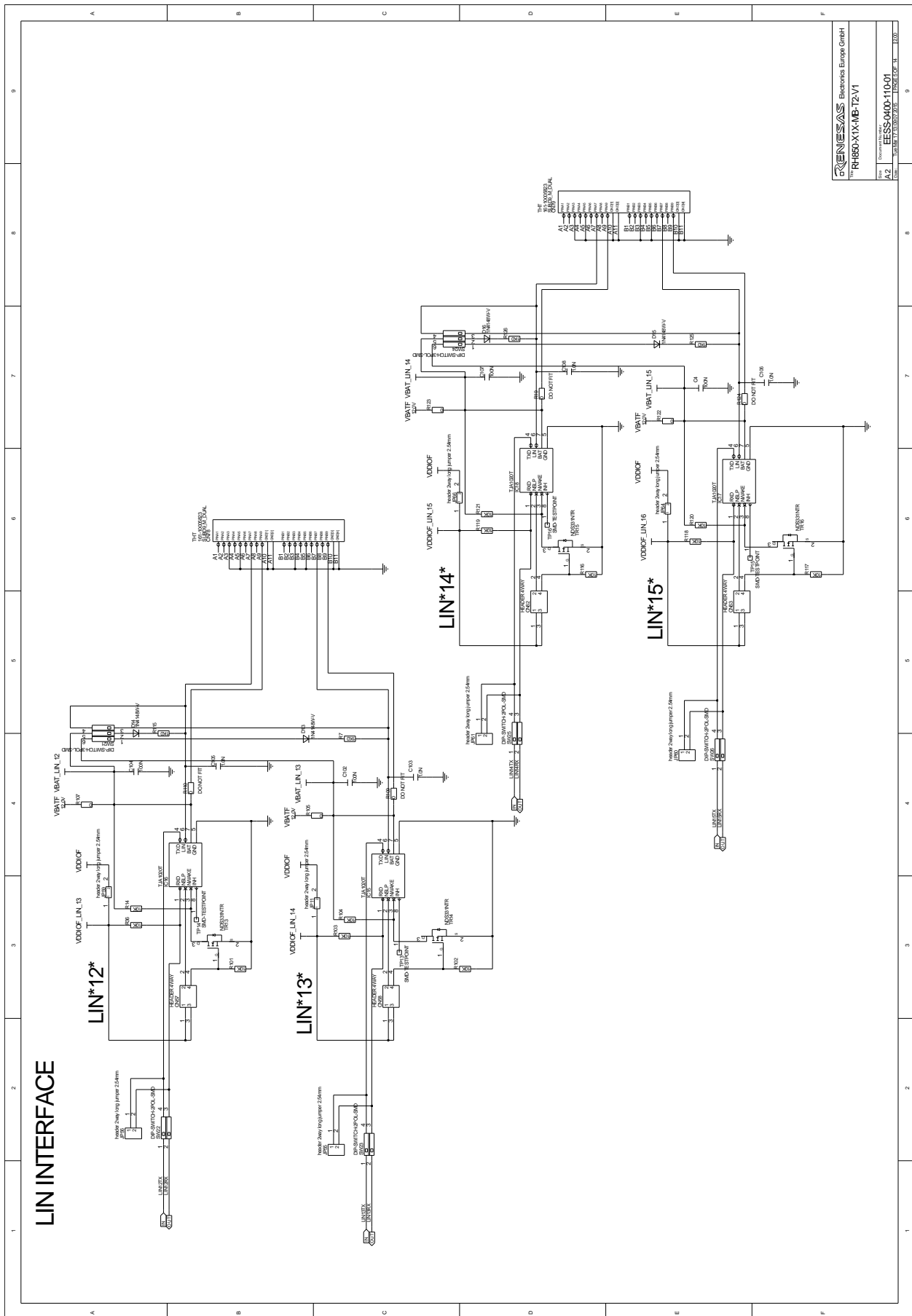




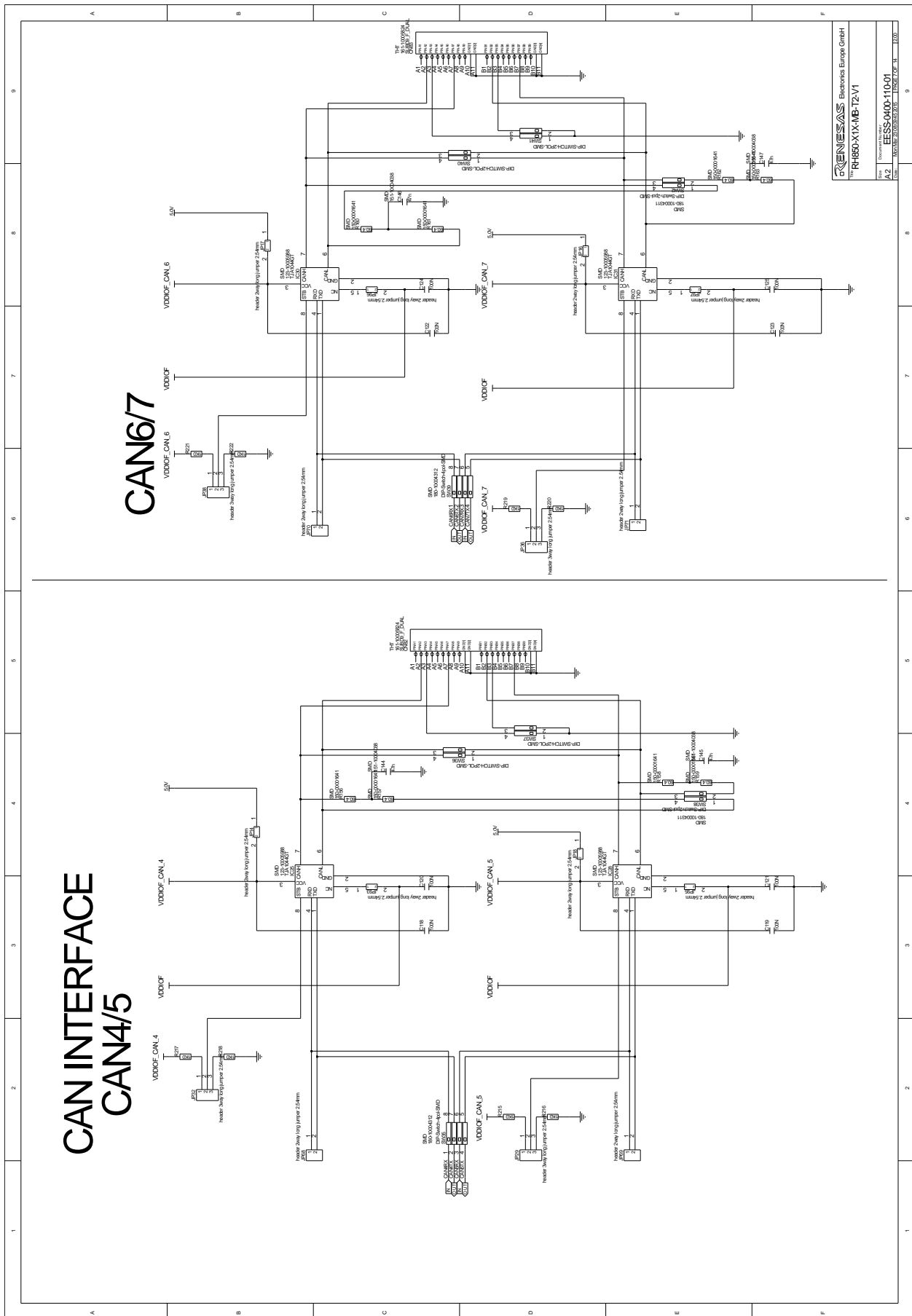




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Drawing No. EESS-000-110-01 Rev. A.2 Date 12/03/07	Issue of 1 Total of 10



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Project	TR2020P-11
Doc. No.	110



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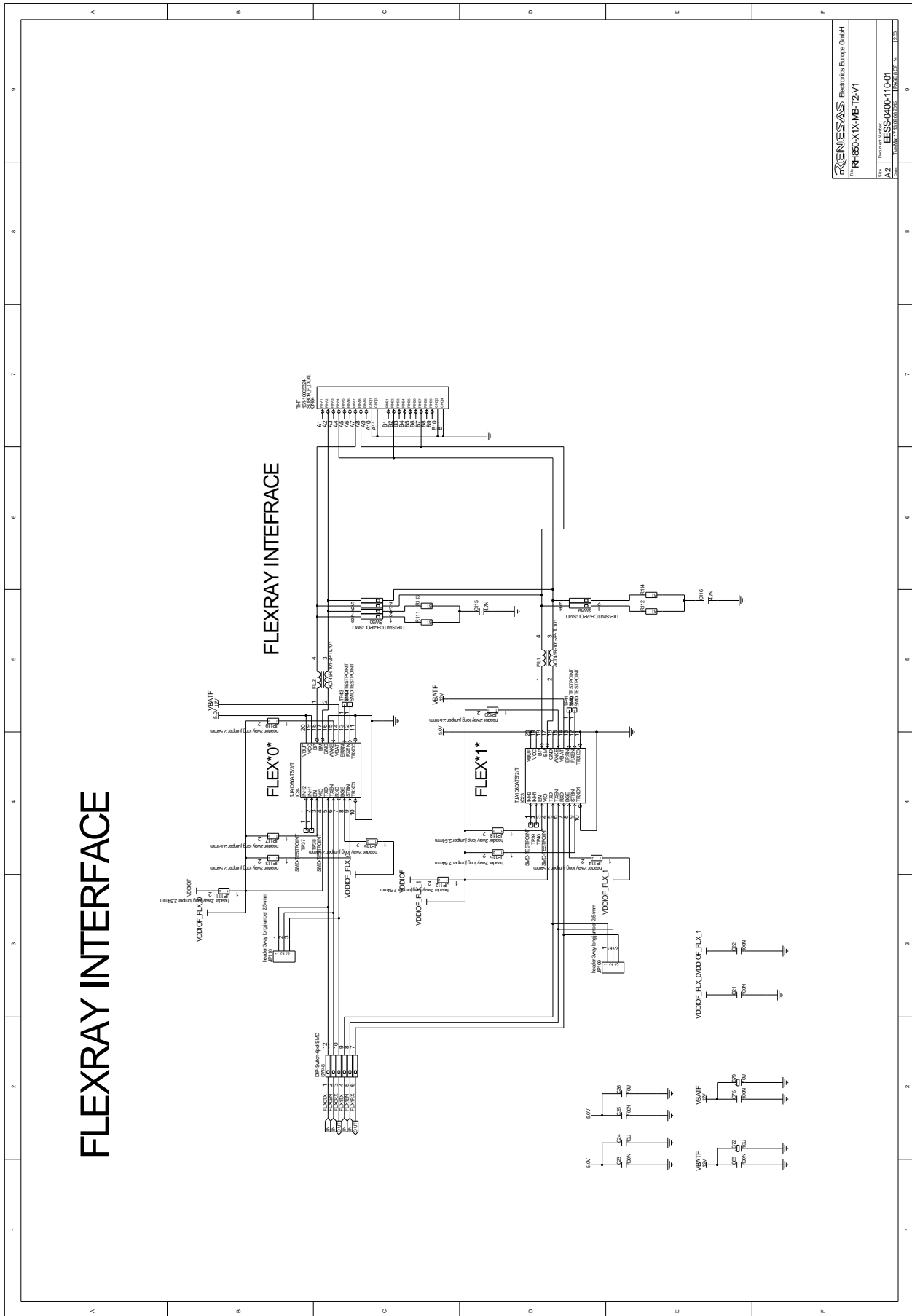
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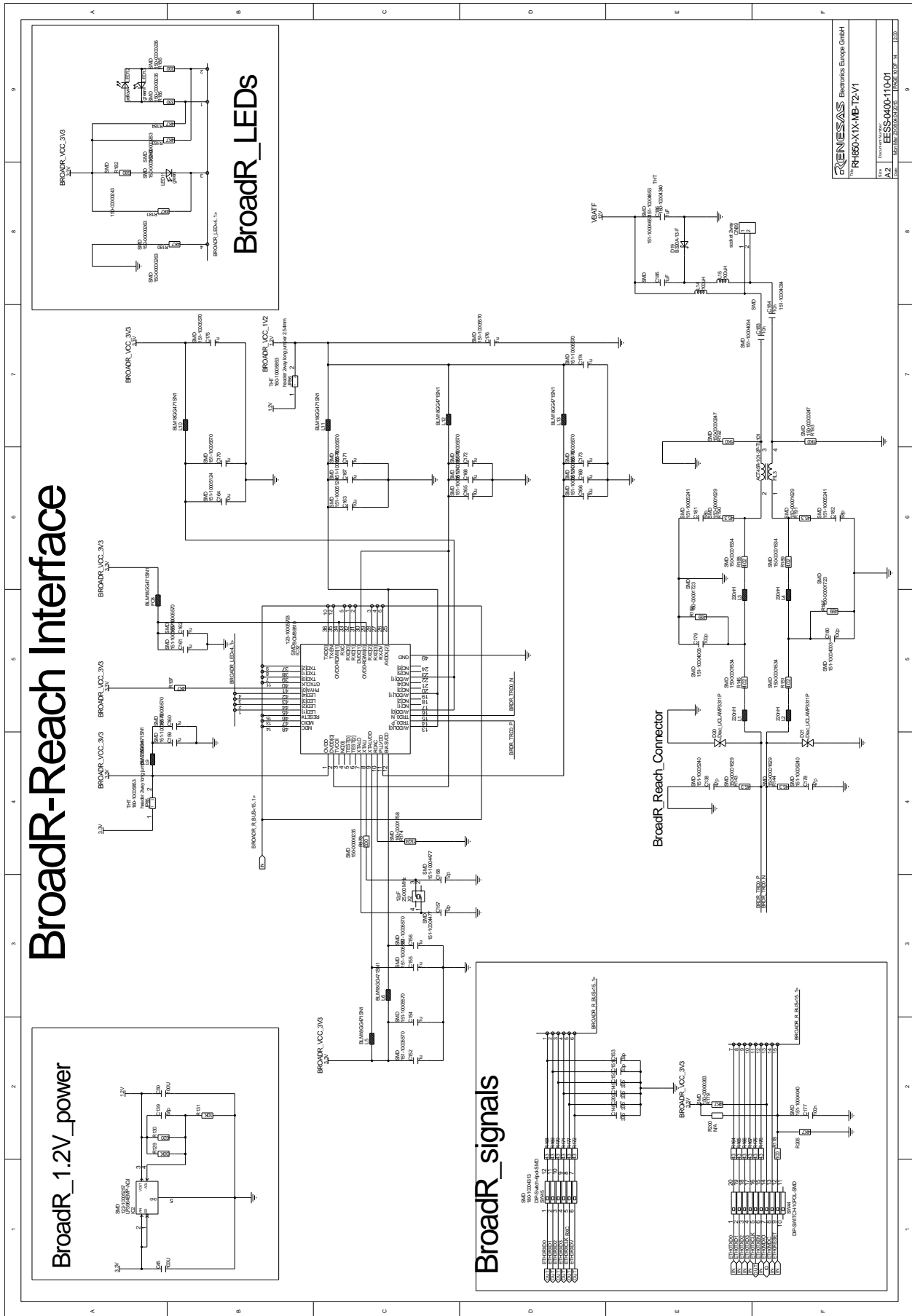
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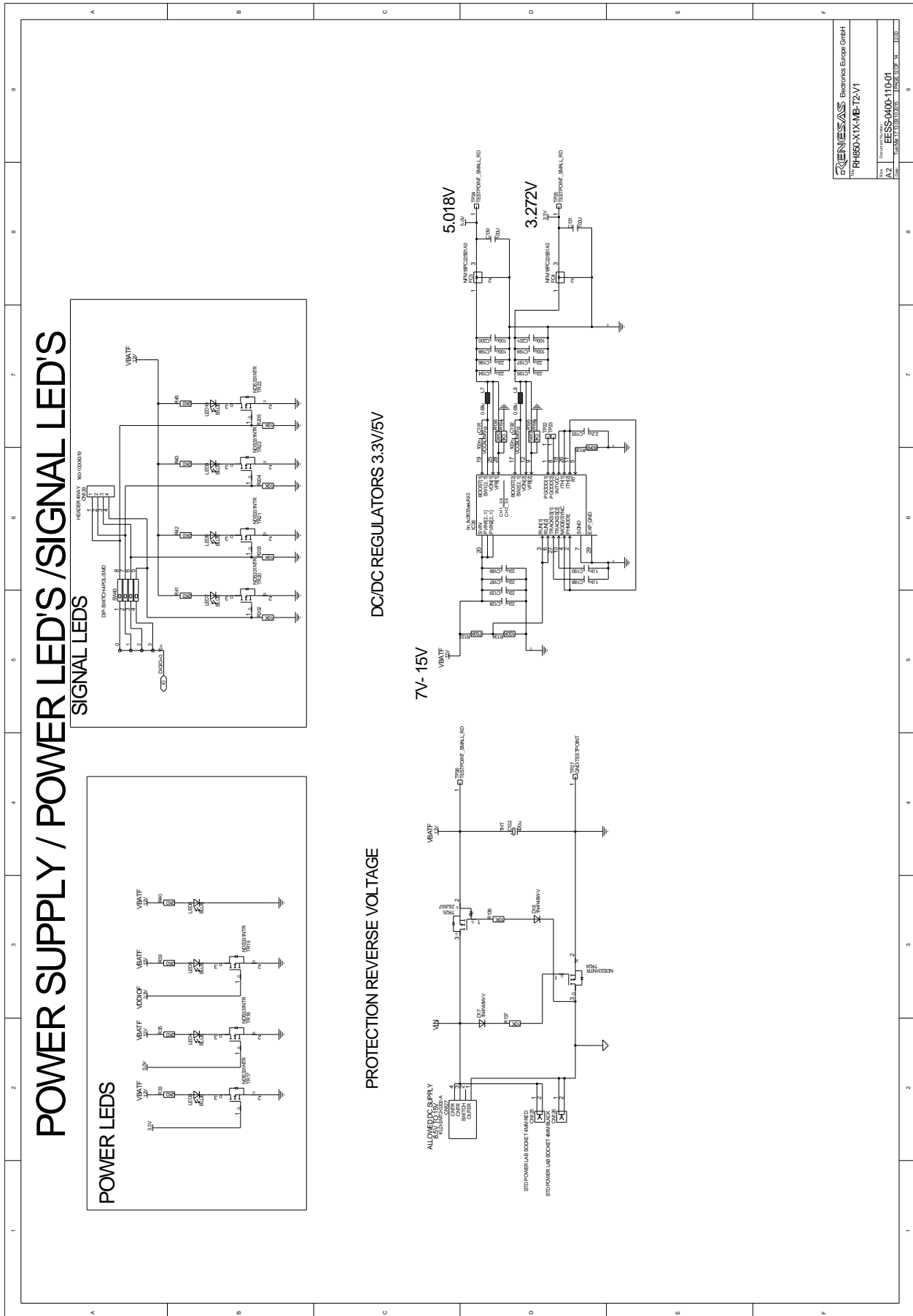
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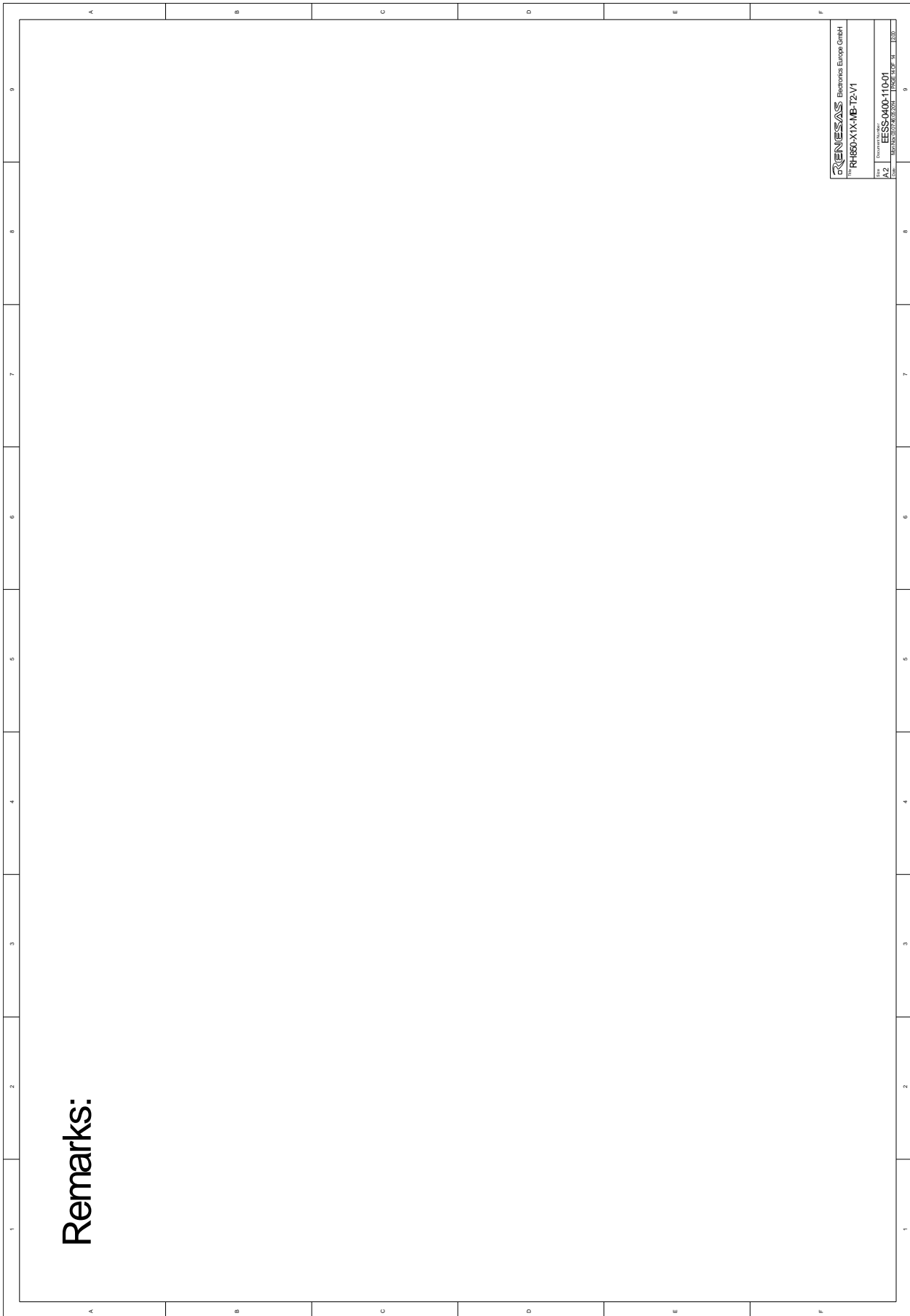


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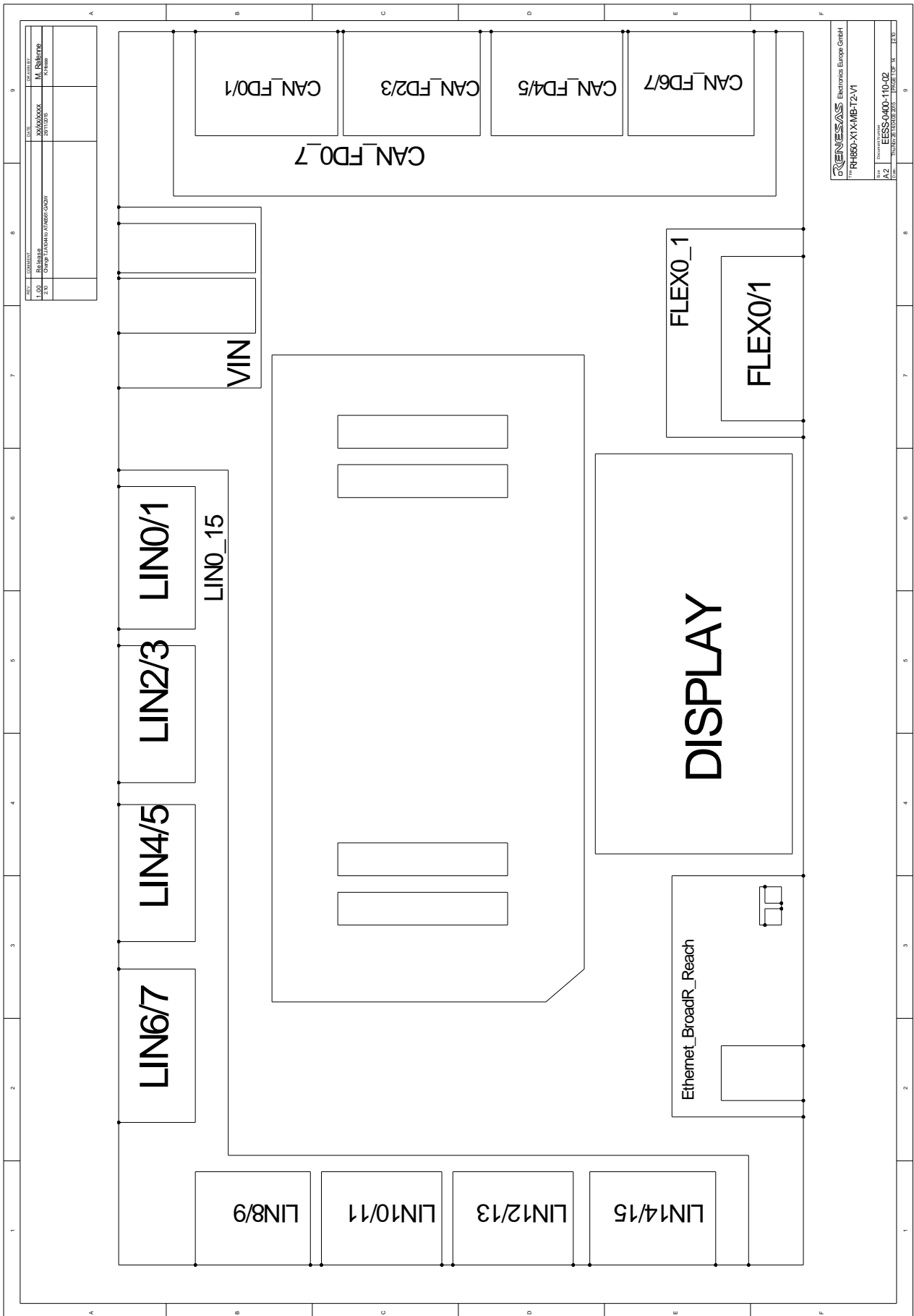


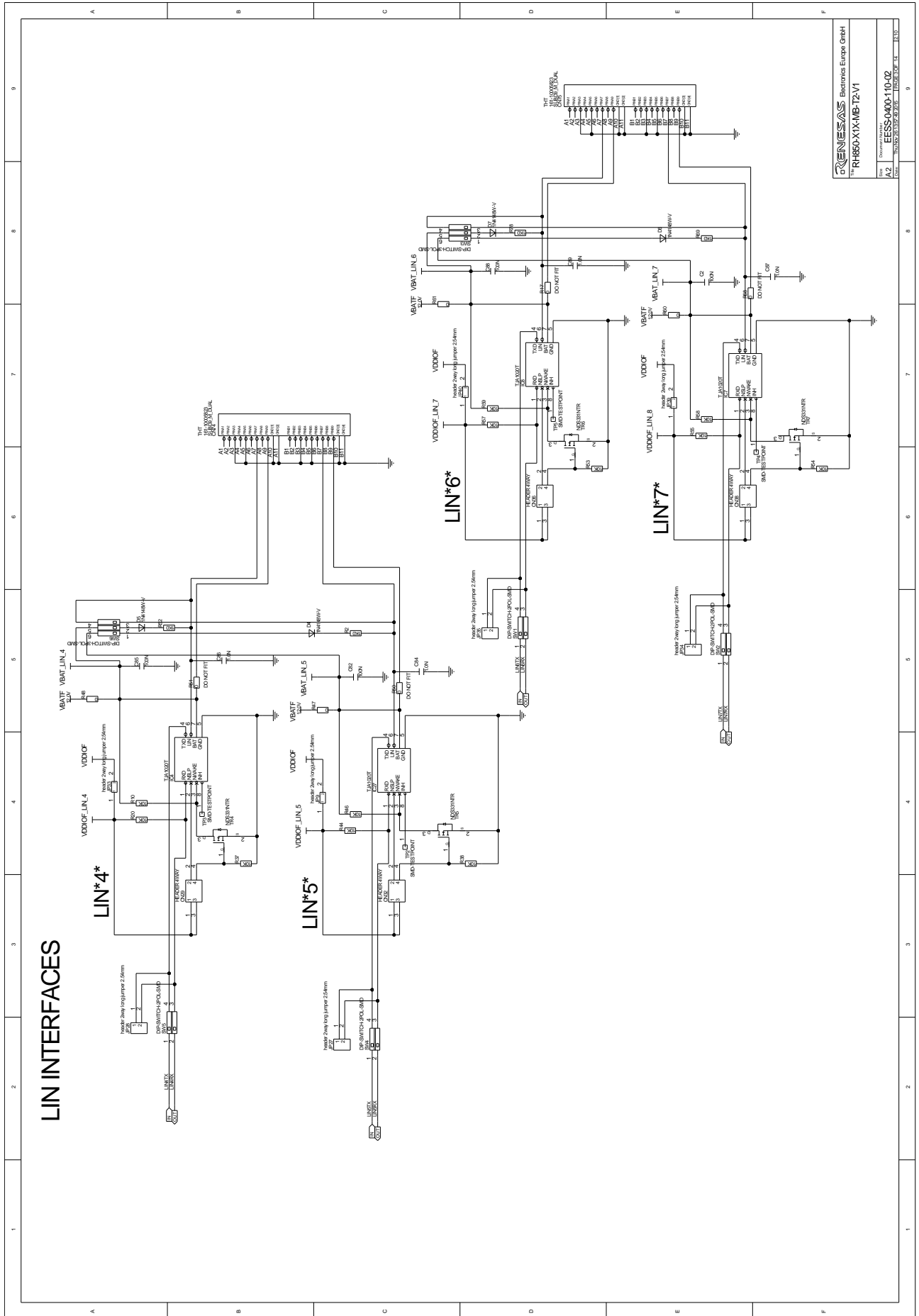
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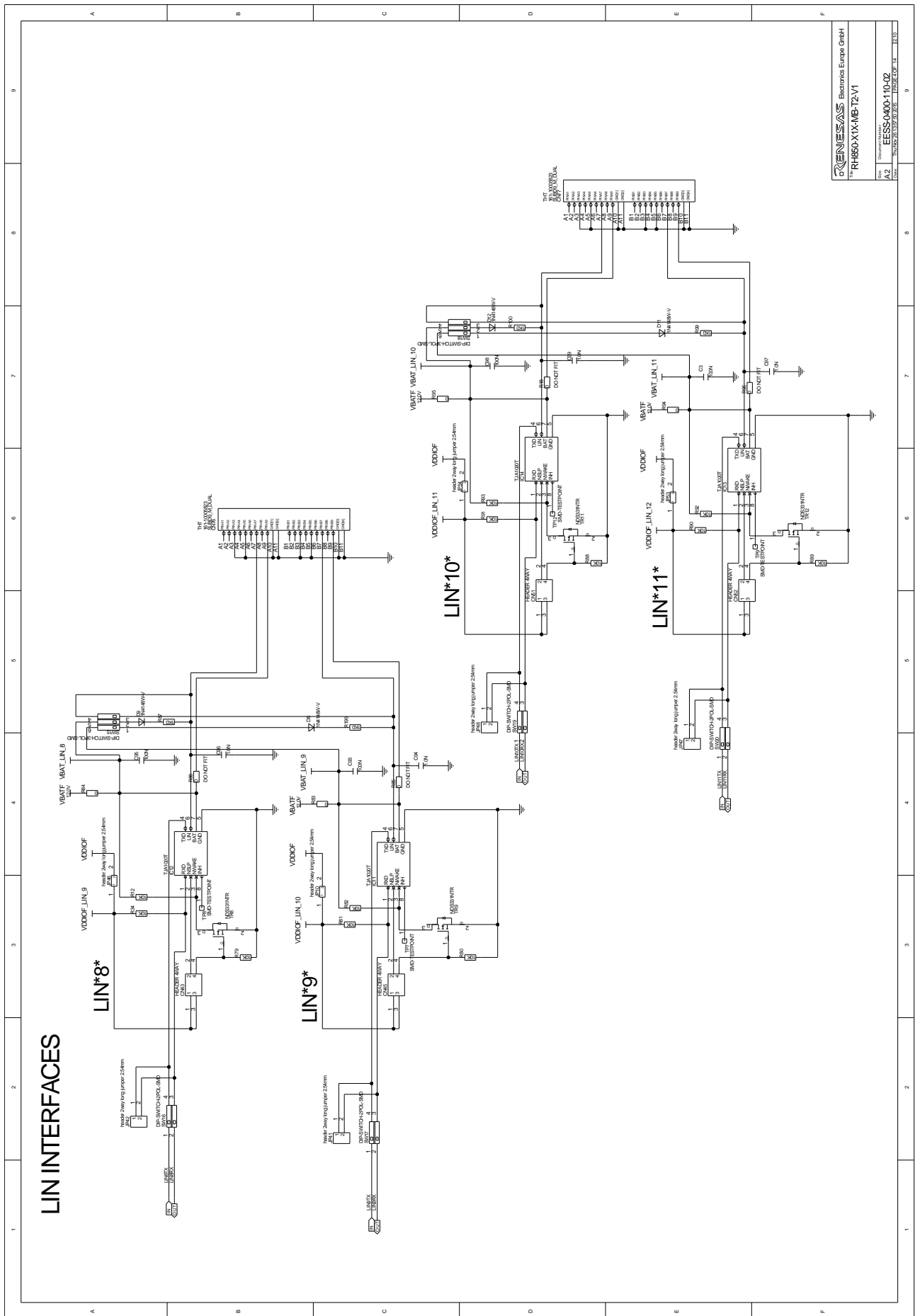


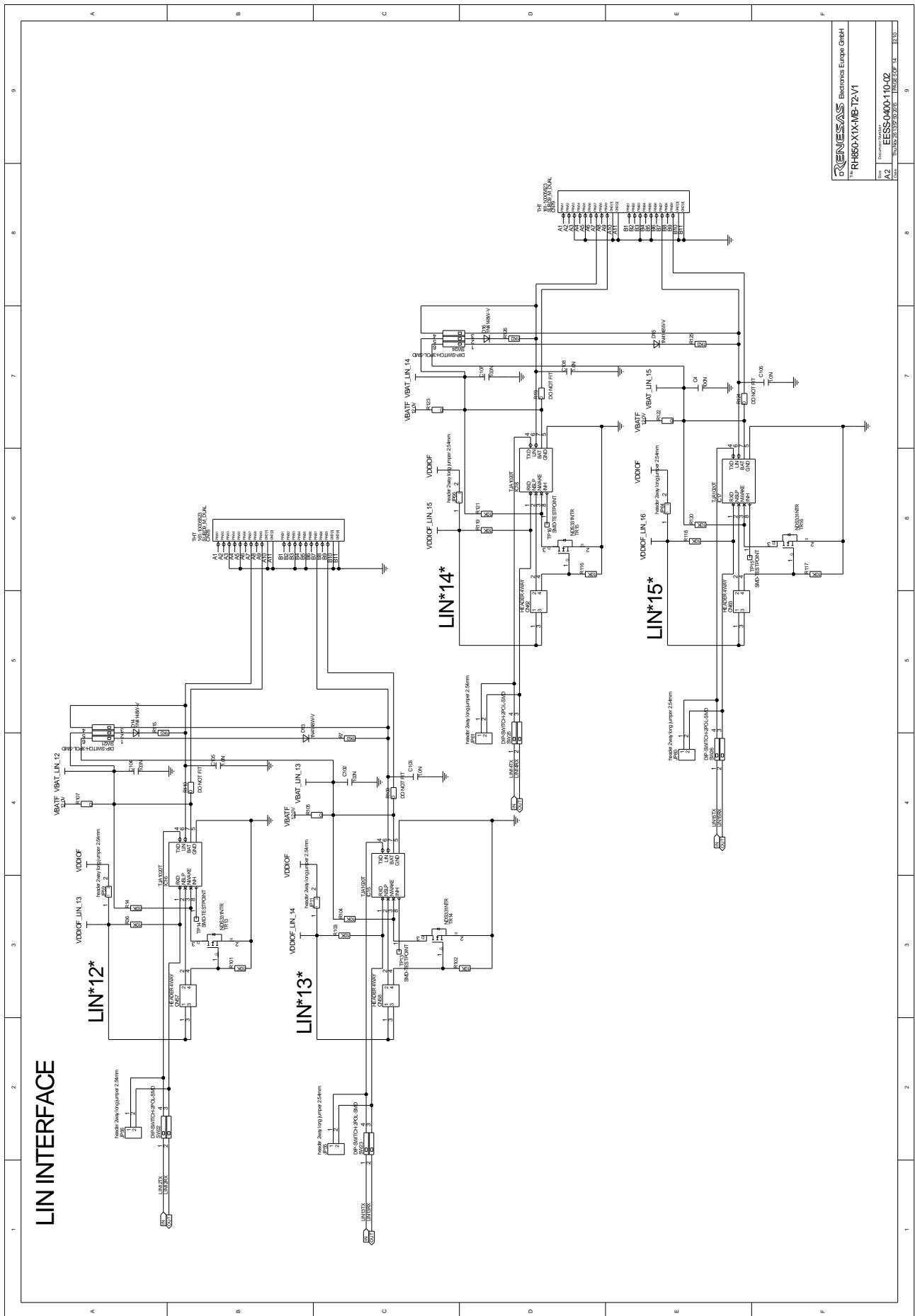
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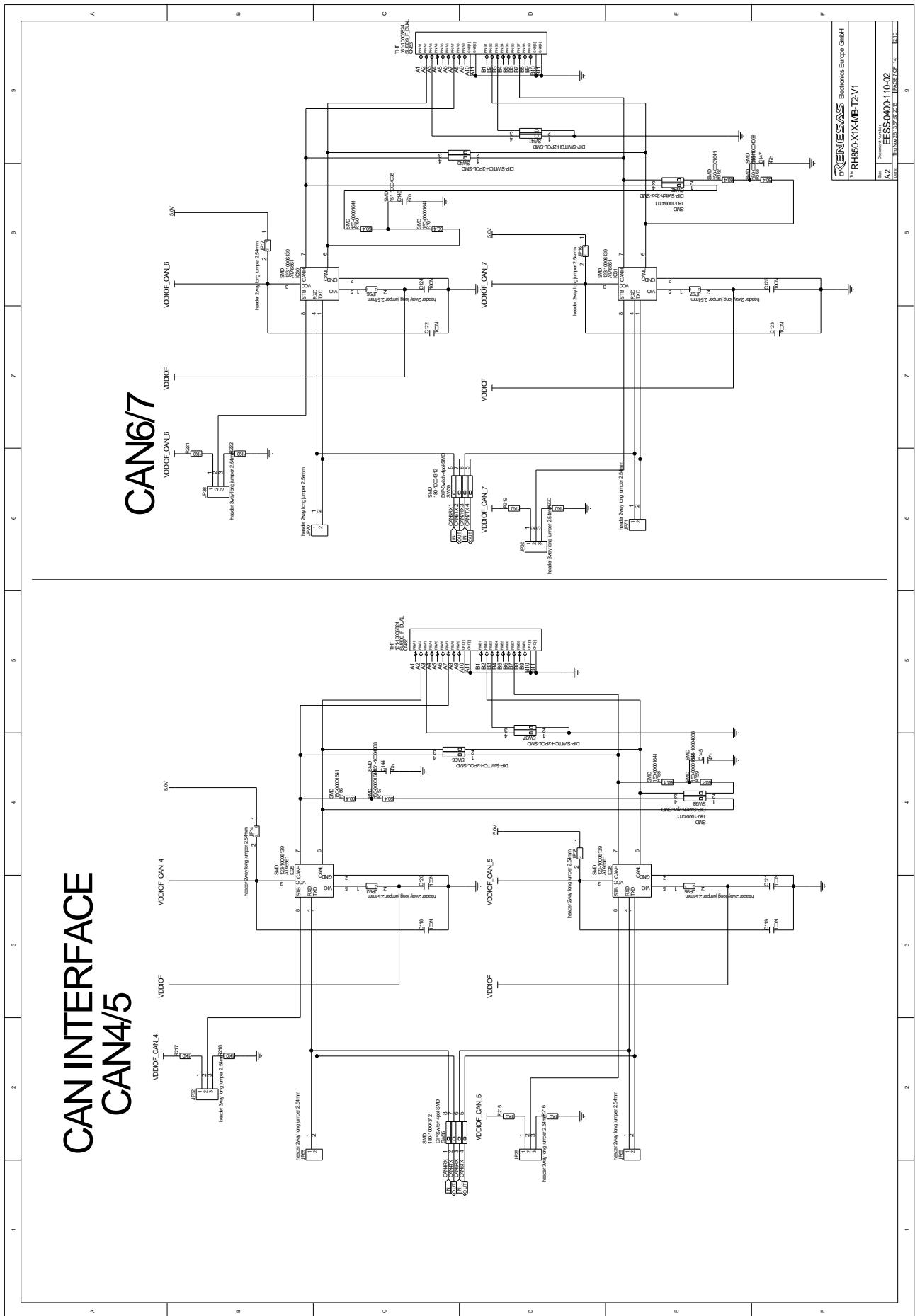


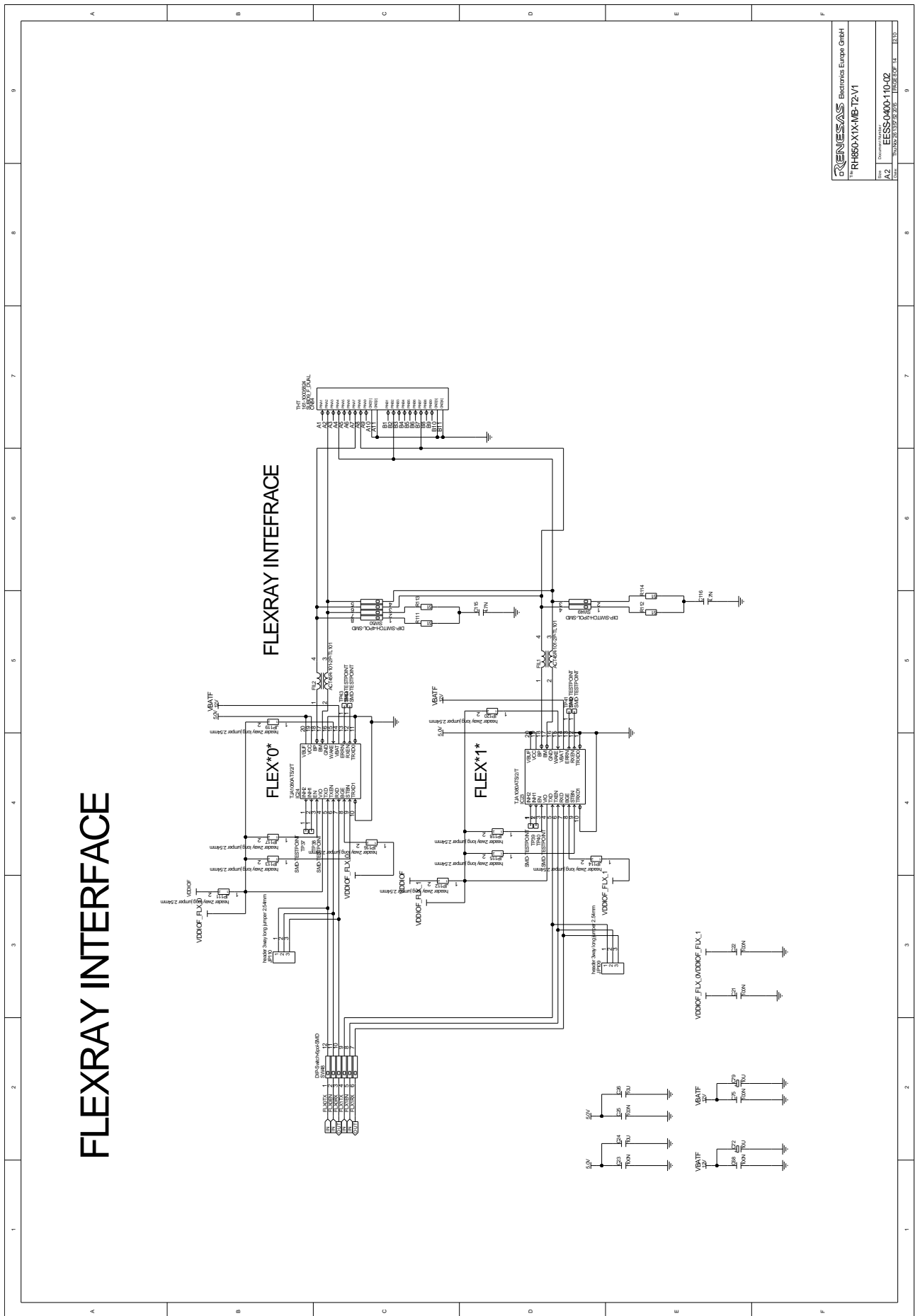
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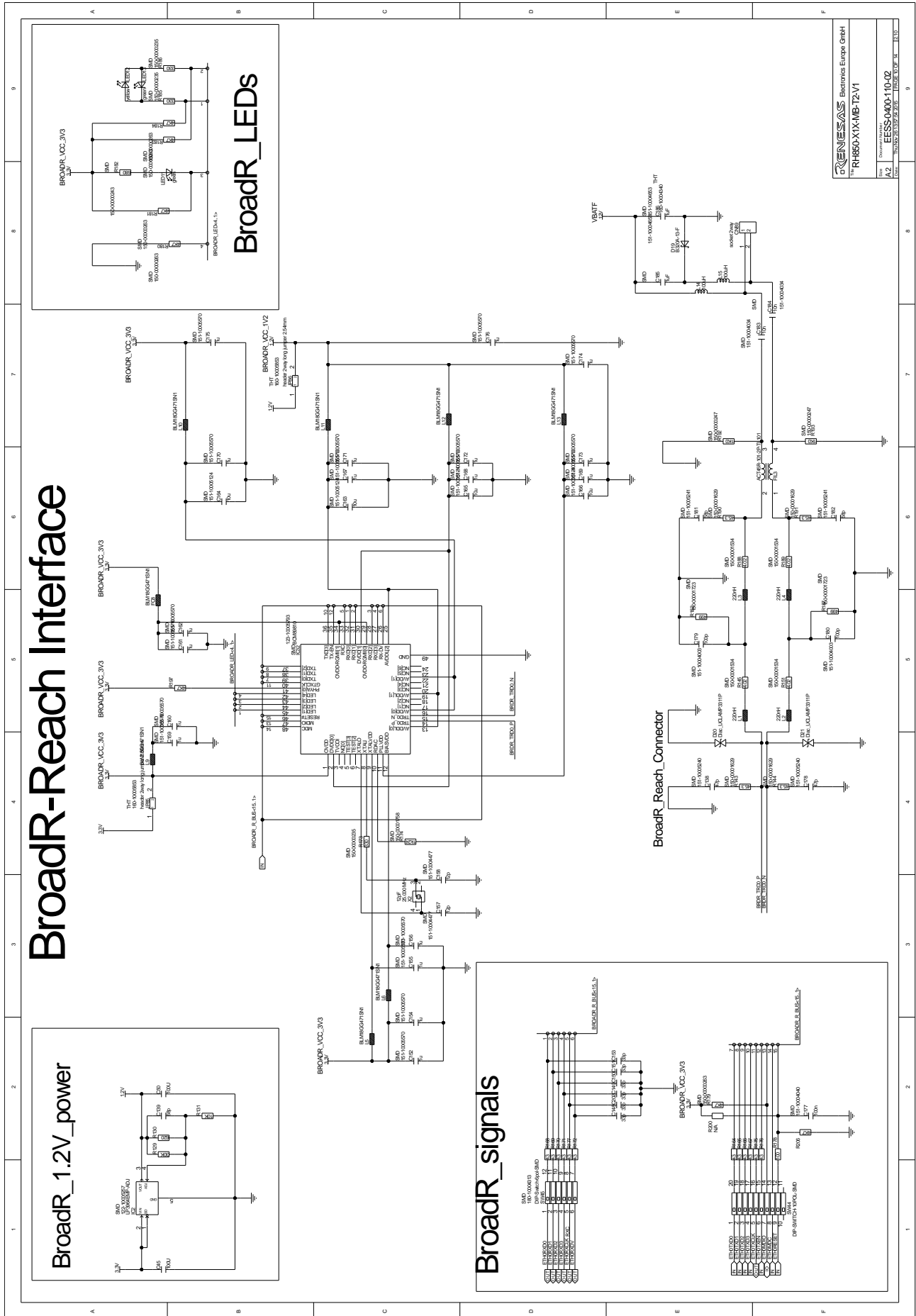


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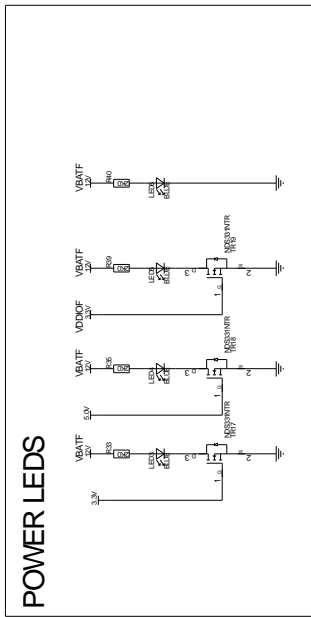
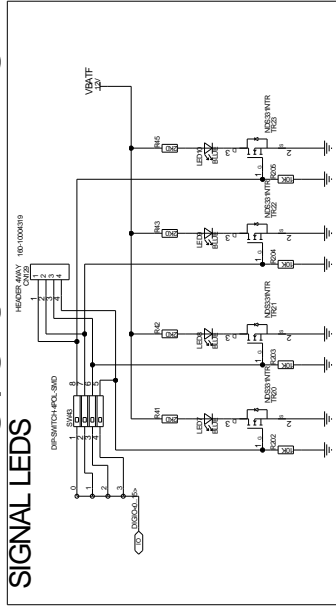




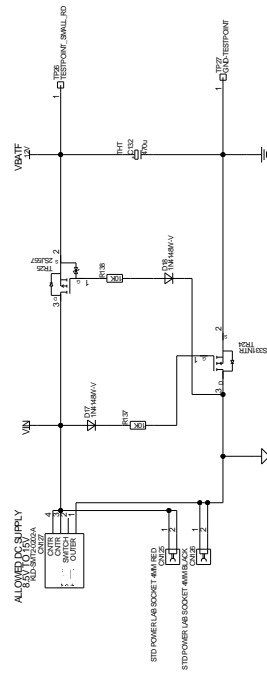
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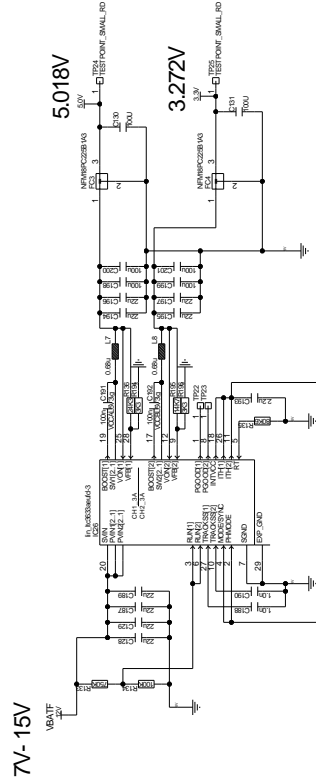
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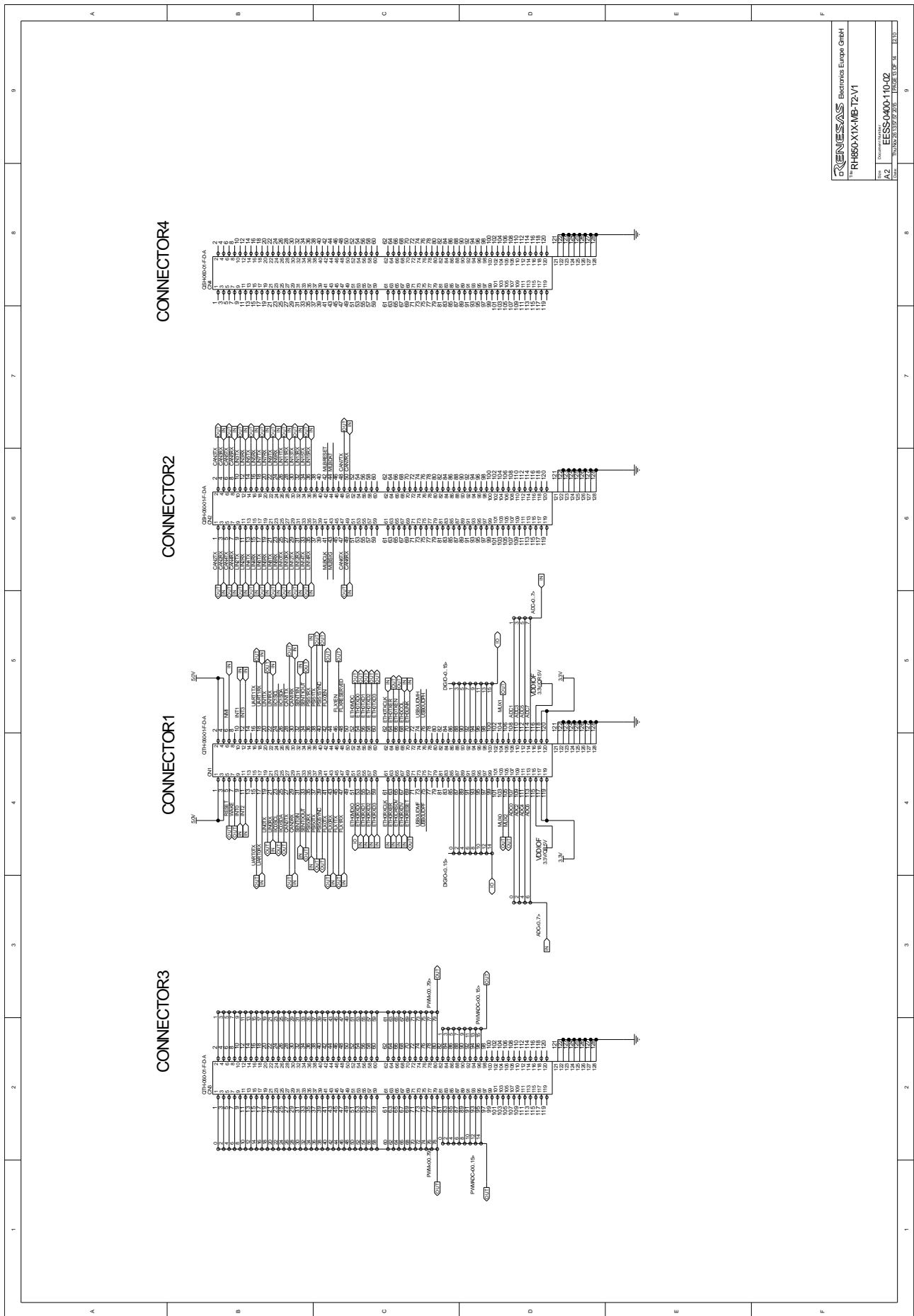
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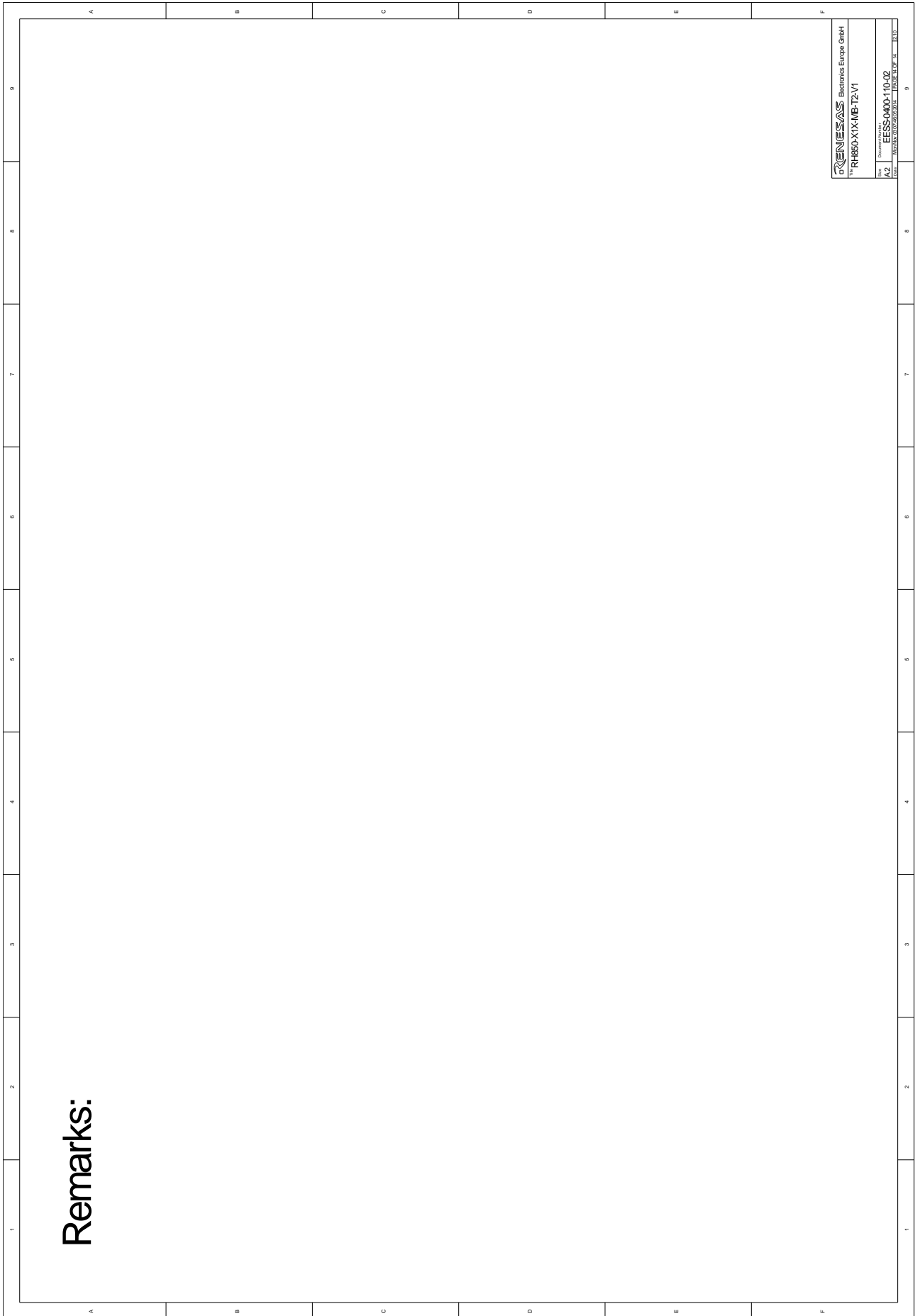
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