24-BIT, 192-kHz SAMPLING, ADVANCED SEGMENT, AUDIO STEREO DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **24-Bit Resolution**
- **Analog Performance:**
  - **Dynamic Range: 132 dB (9 V RMS, Mono)**
    129 dB (4.5 V RMS, Stereo)
    127 dB (2 V RMS, Stereo)
  - **THD+N: 0.0004%**
- **Differential Current Output: 7.8 mA p-p**
- **8× Oversampling Digital Filter:**
  - **Stop-Band Attenuation: –130 dB**
  - **Pass-Band Ripple: ±0.00001 dB**
- **Sampling Frequency: 10 kHz to 200 kHz**
- **System Clock: 128, 192, 256, 384, 512, or 768 f_S With Autodetect**
- **Accepts 16- and 24-Bit Audio Data**
- **PCM Data Formats: Standard, I^2S, and Left-Justified**
- **Optional Interface Available to External Digital Filter or DSP**
- **Digital De-Emphasis**
- **Digital Filter Rolloff: Sharp or Slow**
- **Soft Mute**
- **Zero Flag**
- **Dual-Supply Operation:**
  - **5-V Analog, 3.3-V Digital**
- **5-V Tolerant Digital Inputs**
- **Small 28-Lead SSOP Package**

APPLICATIONS

- **A/V Receivers**
- **DVD Players**
- **Musical Instruments**
- **HDTV Receivers**
- **Car Audio Systems**
- **Digital Multitrack Recorders**
- **Other Applications Requiring 24-Bit Audio**

DESCRIPTION

The PCM1794 is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters and support circuitry in a small 28-lead SSOP package. The data converters use TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1794 provides balanced current outputs, allowing the user to optimize analog performance externally. Sampling rates up to 200 kHz are supported.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PCM1794DB	28-lead SSOP	28DB	–25°C to 85°C	PCM1794	PCM1794DB	Tube
					PCM1794DBR	Tape and reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		PCM1794
Supply voltage	$V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$	–0.3 V to 6.5 V
	V_{DD}	–0.3 V to 4 V
Supply voltage differences: $V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$		±0.1 V
Ground voltage differences: AGND1, AGND2, AGND3L, AGND3R, DGND		±0.1 V
Digital input voltage	LRCK, DATA, BCK, SCK, FMT1, FMT0, MONO, CHSL, DEM, MUTE, $\overline{RST}$,	–0.3 V to 6.5 V
	ZERO	–0.3 V to (V_{DD} + 0.3 V) < 4 V
Analog input voltage		–0.3 V to (V_{CC} + 0.3 V) < 6.5 V
Input current (any pins except supplies)		±10 mA
Ambient temperature under bias		–40°C to 125°C
Storage temperature		–55°C to 150°C
Junction temperature		150°C
Lead temperature (soldering)		260°C, 5 s
Package temperature (IR reflow, peak)		250°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM1794DB MIN	TYP	MAX	UNIT
RESOLUTION				24		Bits
DATA FORMAT						
	Audio data interface format		Standard, I^2S, left justified			
	Audio data bit length		16-, 24-bit selectable			
	Audio data format		MSB first, 2s complement			
f_S	Sampling frequency		10		200	kHz
	System clock frequency		128, 192, 256, 384, 512, 768 f_S			
DIGITAL INPUT/OUTPUT						
	Logic family		TTL compatible			
V_{IH}	Input logic level		2			VDC
V_{IL}					0.8	
I_{IH}	Input logic current	$V_{IN} = V_{DD}$			10	µA
I_{IL}		V_{IN} = 0 V			–10	
V_{OH}	Output logic level	I_{OH} = –2 mA	2.4			VDC
V_{OL}		I_{OL} = 2 mA			0.4	

ELECTRICAL CHARACTERISTICS (Continued)

all specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data, unless otherwise noted

PARAMETER	TEST CONDITIONS	PCM1794DB			UNIT
		MIN	TYP	MAX	
DYNAMIC PERFORMANCE (2-V RMS OUTPUT) (1)(2)					
THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%	0.0008%	
	f_S = 96 kHz		0.0008%		
	f_S = 192 kHz		0.0015%		
Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	123	127		dB
	EIAJ, A-weighted, f_S = 96 kHz		127		
	EIAJ, A-weighted, f_S = 192 kHz		127		
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	123	127		dB
	EIAJ, A-weighted, f_S = 96 kHz		127		
	EIAJ, A-weighted, f_S = 192 kHz		127		
Channel separation	f_S = 44.1 kHz	120	123		dB
	f_S = 96 kHz		122		
	f_S = 192 kHz		120		
Level linearity error	V_{OUT} = –120 dB		±1		dB
DYNAMIC PERFORMANCE (4.5-V RMS Output) (1)(3)					
THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%		
	f_S = 96 kHz		0.0008%		
	f_S = 192 kHz		0.0015%		
Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz		129		dB
	EIAJ, A-weighted, f_S = 96 kHz		129		
	EIAJ, A-weighted, f_S = 192 kHz		129		
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz		129		dB
	EIAJ, A-weighted, f_S = 96 kHz		129		
	EIAJ, A-weighted, f_S = 192 kHz		129		
Channel separation	f_S = 44.1 kHz		124		dB
	f_S = 96 kHz		123		
	f_S = 192 kHz		121		
DYNAMIC PERFORMANCE (MONO MODE) (1)(3)					
THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%		
	f_S = 96 kHz		0.0008%		
	f_S = 192 kHz		0.0015%		
Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz		132		dB
	EIAJ, A-weighted, f_S = 96 kHz		132		
	EIAJ, A-weighted, f_S = 192 kHz		132		
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz		132		dB
	EIAJ, A-weighted, f_S = 96 kHz		132		
	EIAJ, A-weighted, f_S = 192 kHz		132		

(1) Filter condition:
THD+N: 20-Hz HPF, 20-kHz apogee LPF
Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Channel separation: 20-Hz HPF, 20-kHz AES17 LPF
Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.
(2) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 24.
(3) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 25.

ELECTRICAL CHARACTERISTICS (Continued)

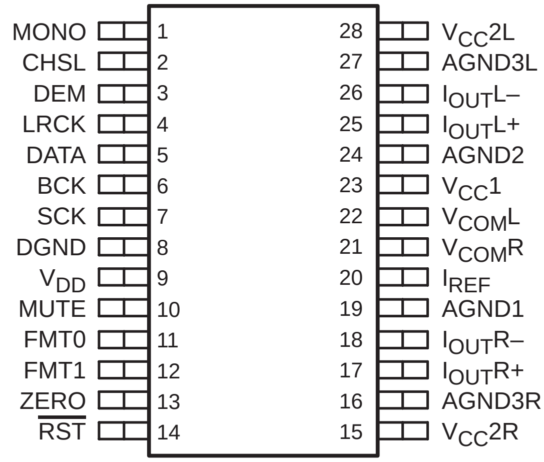
all specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM1794DB MIN	PCM1794DB TYP	PCM1794DB MAX	UNIT
ANALOG OUTPUT						
	Gain error		–6	±2	6	% of FSR
	Gain mismatch, channel-to-channel		–3	±0.5	3	% of FSR
	Bipolar zero error	At BPZ	–2	±0.5	2	% of FSR
	Output current	Full scale (0 dB)		7.8		mA p-p
	Center current	At BPZ		–6.2		mA
DIGITAL FILTER PERFORMANCE						
	De-emphasis error				±0.004	dB
FILTER CHARACTERISTICS-1: SHARP ROLLOFF						
	Pass band	±0.00001 dB			0.454 f_S	
		–3 dB			0.49 f_S	
	Stop band		0.546 f_S			
	Pass-band ripple				±0.00001	dB
	Stop-band attenuation	Stop band = 0.546 f_S	–130			dB
	Delay time			55/f_S		s
FILTER CHARACTERISTICS-2: SLOW ROLLOFF						
	Pass band	±0.04 dB			0.254 f_S	
		–3 dB			0.46 f_S	
	Stop band		0.732 f_S			
	Pass-band ripple				±0.001	dB
	Stop-band attenuation	Stop band = 0.732 f_S	–100			dB
	Delay time			18/f_S		s
POWER SUPPLY REQUIREMENTS						
V_{DD}	Voltage range		3	3.3	3.6	VDC
$V_{CC}1$			4.75	5	5.25	VDC
$V_{CC}2L$						
$V_{CC}2R$						
I_{DD}	Supply current (1)	f_S = 44.1 kHz		12	15	mA
		f_S = 96 kHz		23		
		f_S = 192 kHz		45		
I_{CC}		f_S = 44.1 kHz		33	40	mA
		f_S = 96 kHz		35		
		f_S = 192 kHz		37		
	Power dissipation (1)	f_S = 44.1 kHz		205	250	mW
		f_S = 96 kHz		250		
		f_S = 192 kHz		335		
TEMPERATURE RANGE						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance	28-pin SSOP		100		°C/W

(1) Input is BPZ data.

PIN ASSIGNMENTS

PCM1794
(TOP VIEW)

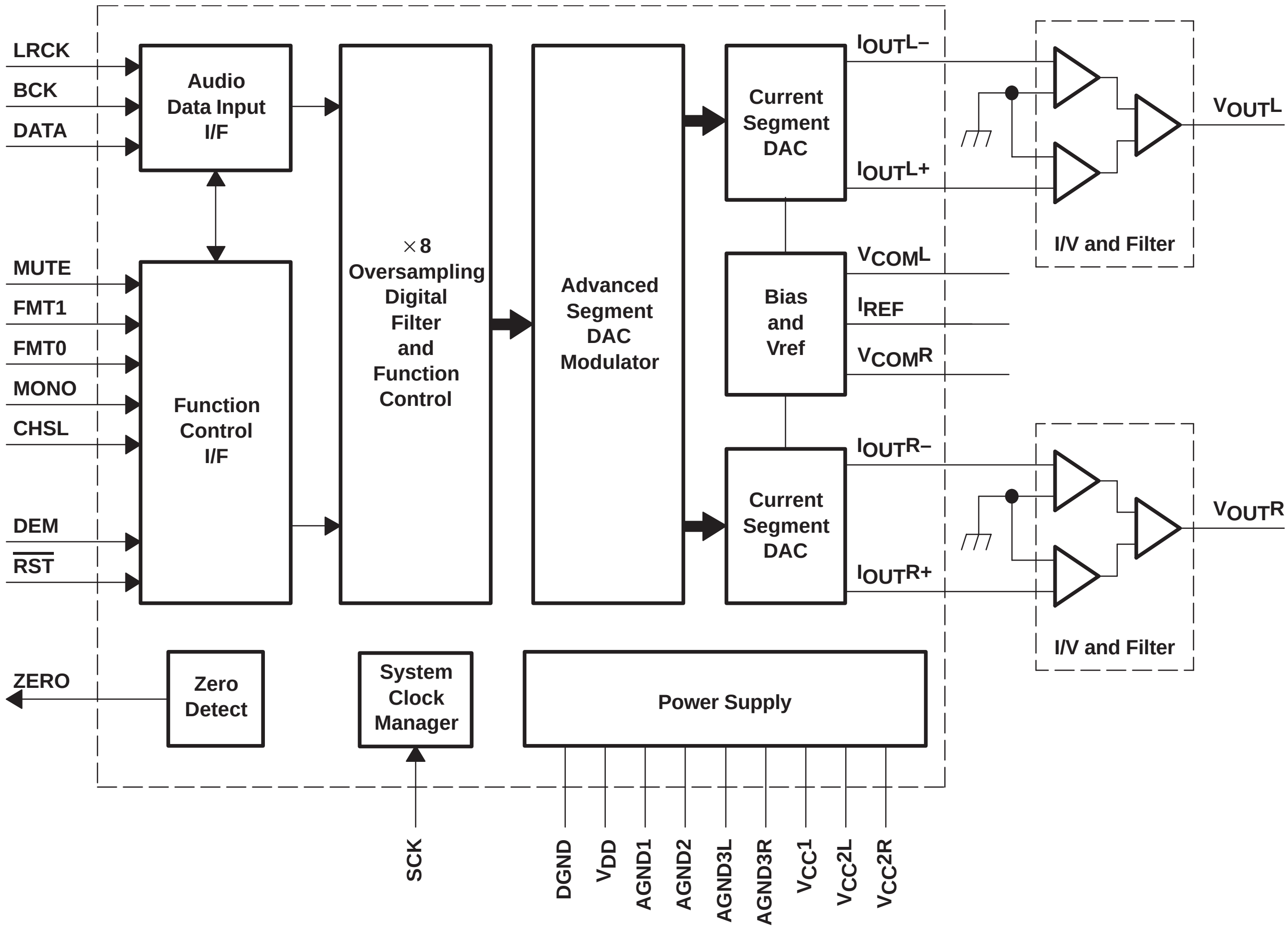


Terminal Functions

TERMINAL NAME	TERMINAL PIN	I/O	DESCRIPTIONS
AGND1	19	–	Analog ground (internal bias)
AGND2	24	–	Analog ground (internal bias)
AGND3L	27	–	Analog ground (L-channel DACFF)
AGND3R	16	–	Analog ground (R-channel DACFF)
BCK	6	I	Bit clock input (1)
CHSL	2	I	L-, R-channel select (1)
DATA	5	I	Serial audio data input (1)
DEM	3	I	De-emphasis enable (1)
DGND	8	–	Digital ground
FMT0	11	I	Audio data format select (1)
FMT1	12	I	Audio data format select (1)
I_{OUT}L+	25	O	L-channel analog current output +
I_{OUT}L–	26	O	L-channel analog current output –
I_{OUT}R+	17	O	R-channel analog current output +
I_{OUT}R–	18	O	R-channel analog current output –
I_{REF}	20	–	Output current reference bias pin
LRCK	4	I	Left and right clock (f_S) input (1)
MONO	1	I	Monaural mode enable (1)
MUTE	10	I	Mute control (1)
$\overline{RST}$	14	I	Reset(1)
SCK	7	I	System clock input(1)
V_{CC}1	23	–	Analog power supply, 5 V
V_{CC}2L	28	–	Analog power supply (L-channel DACFF), 5 V
V_{CC}2R	15	–	Analog power supply (R-cahnnel DACFF), 5 V
V_{COM}L	22	–	L-channel internal bias decoupling pin
V_{COM}R	21	–	R-channel internal bias decoupling pin
V_{DD}	9	–	Digital power supply, 3.3 V
ZERO	13	O	Zero flag

(1) Schmitt-trigger input, 5-V tolerant

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CURVES

DIGITAL FILTER

Digital Filter Response

AMPLITUDE
vs
FREQUENCY

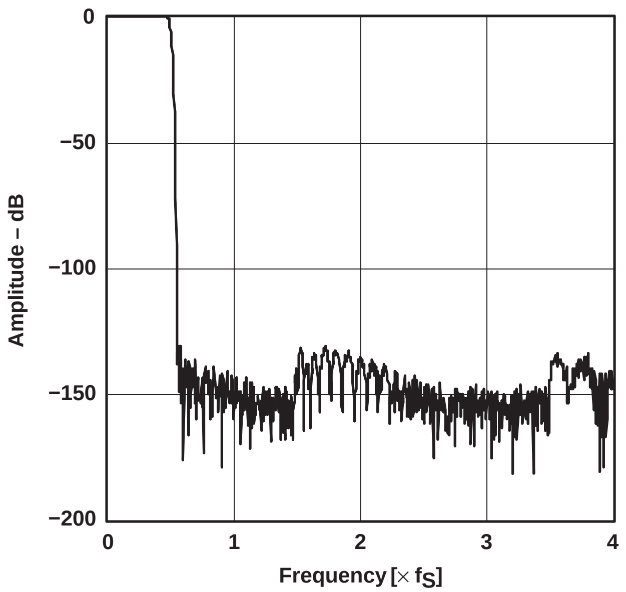


Figure 1. Frequency Response, Sharp Rolloff

AMPLITUDE
vs
FREQUENCY

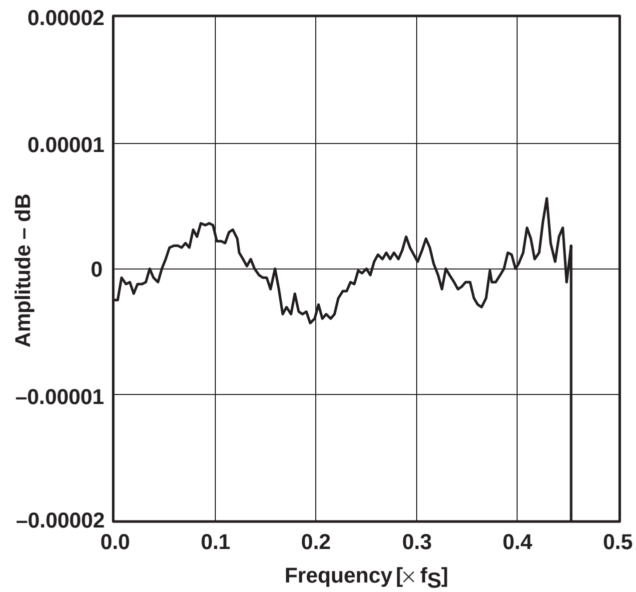


Figure 2. Pass-Band Ripple, Sharp Rolloff

AMPLITUDE
vs
FREQUENCY

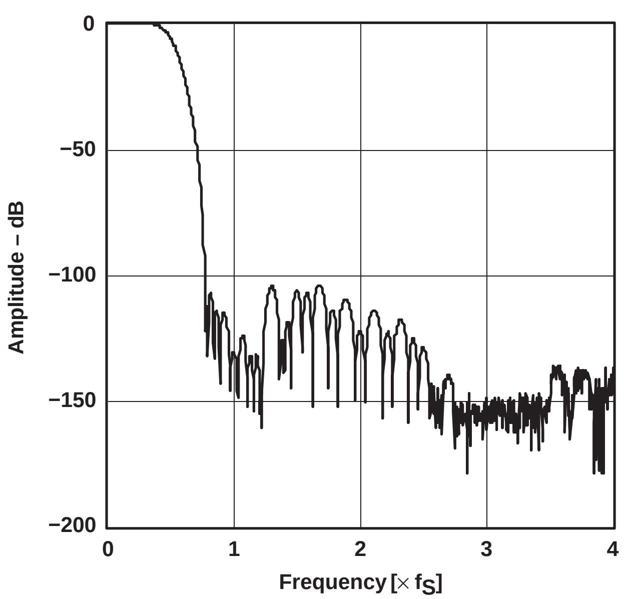


Figure 3. Frequency Response, Slow Rolloff

AMPLITUDE
vs
FREQUENCY

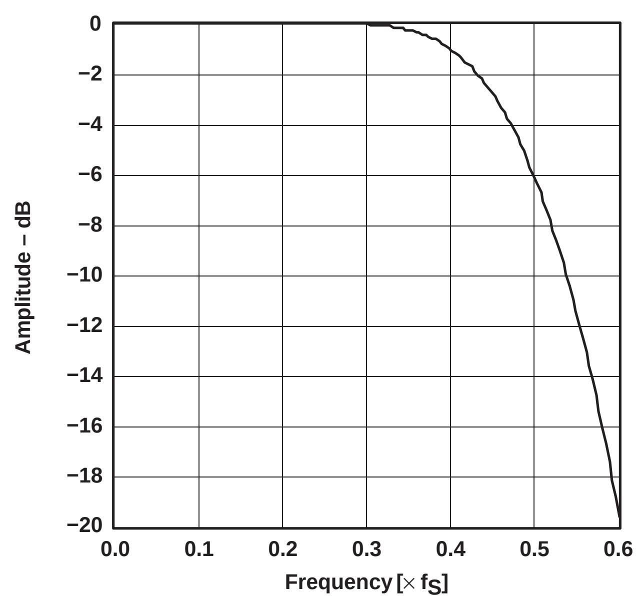


Figure 4. Transition Characteristics, Slow Rolloff

De-Emphasis Filter

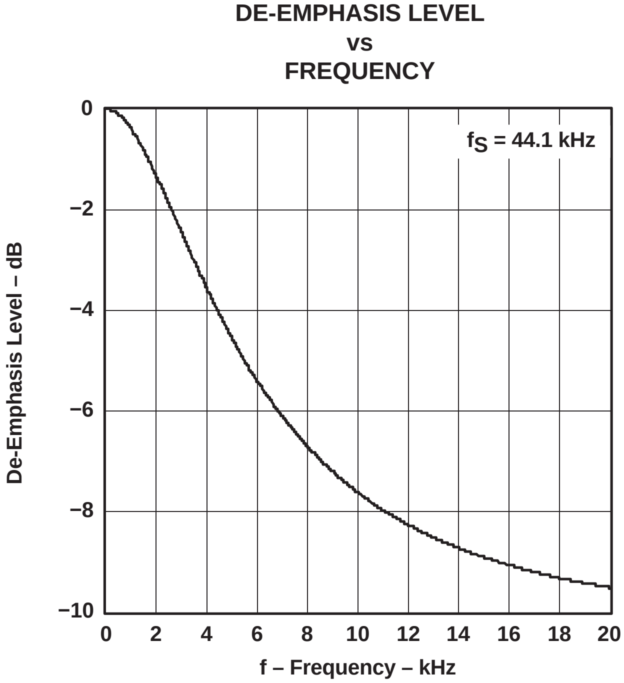


Figure 5

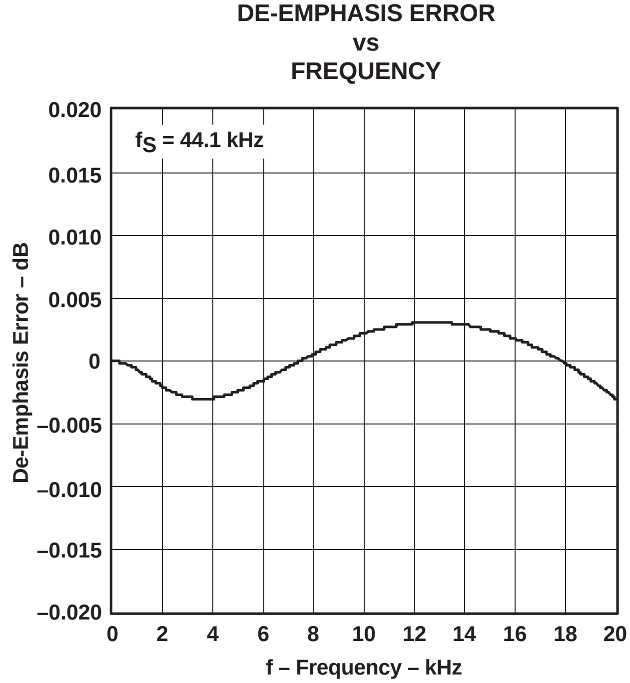


Figure 6

ANALOG DYNAMIC PERFORMANCE

Supply Voltage Characteristics

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE

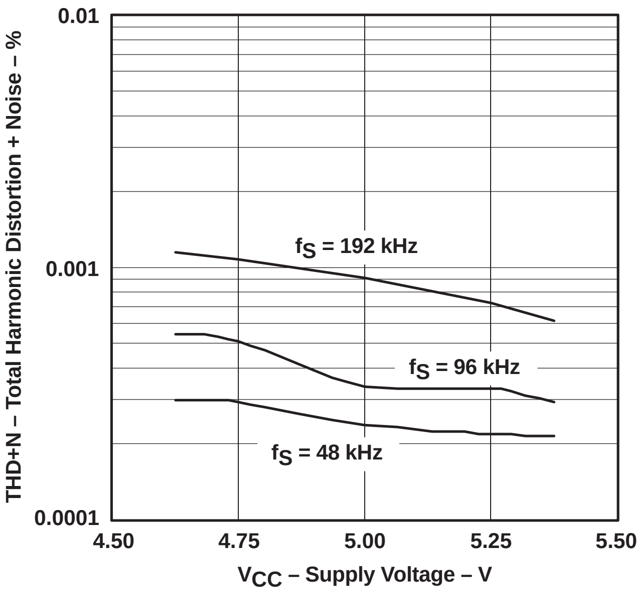


Figure 7

DYNAMIC RANGE vs SUPPLY VOLTAGE

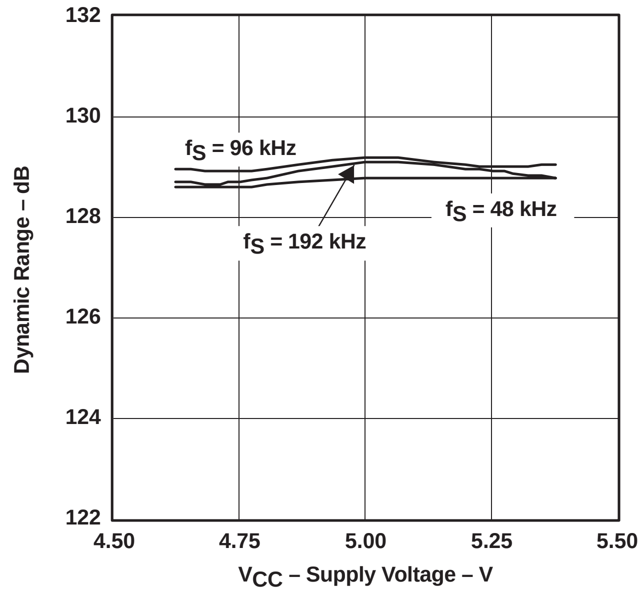


Figure 8

SIGNAL-to-NOISE RATIO vs SUPPLY VOLTAGE

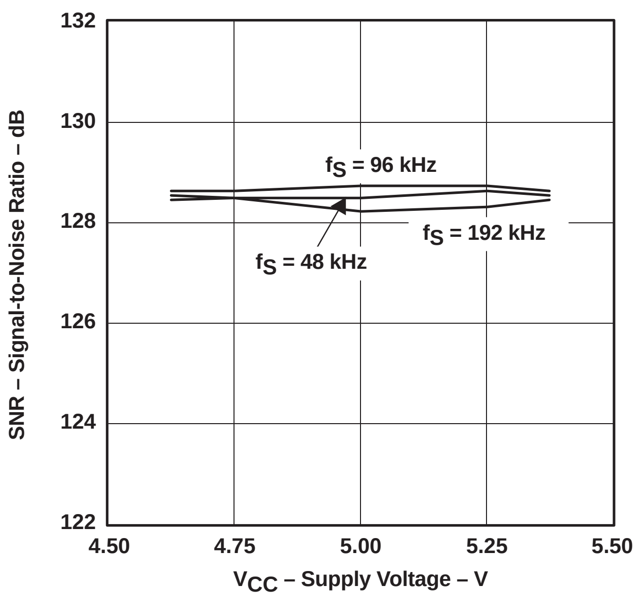


Figure 9

CHANNEL SEPARATION vs SUPPLY VOLTAGE

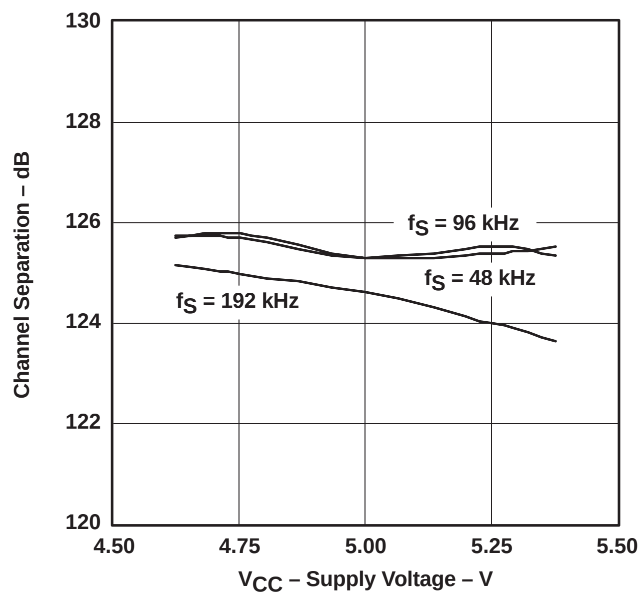


Figure 10

NOTE: T_A = 25°C, V_{DD} = 3.3 V, measurement circuit is Figure 25 (V_{OUT} = 4.5 V rms).

Temperature Characteristics

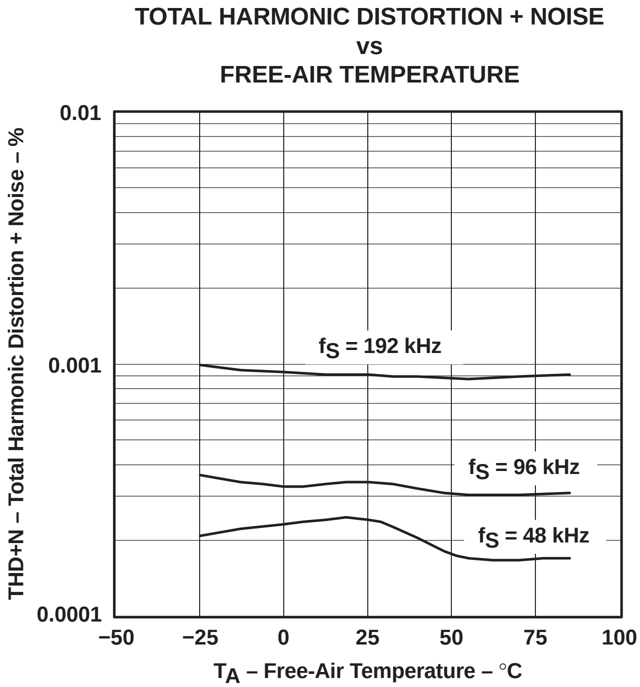


Figure 11

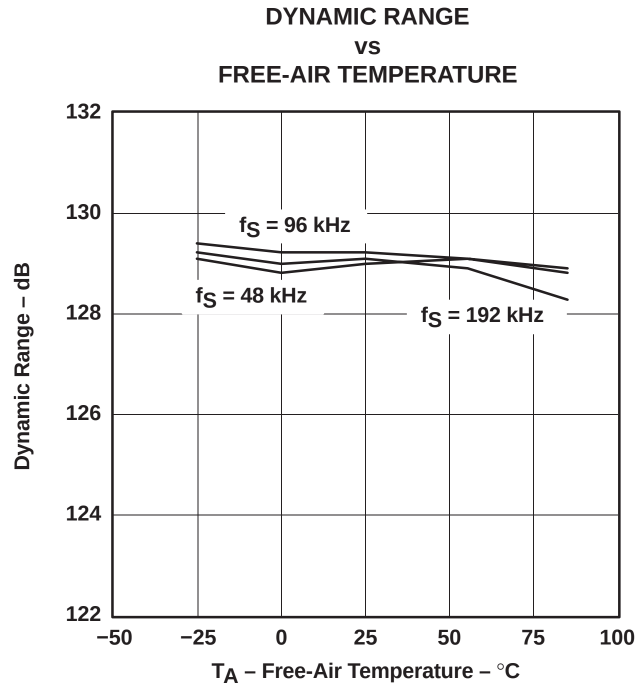


Figure 12

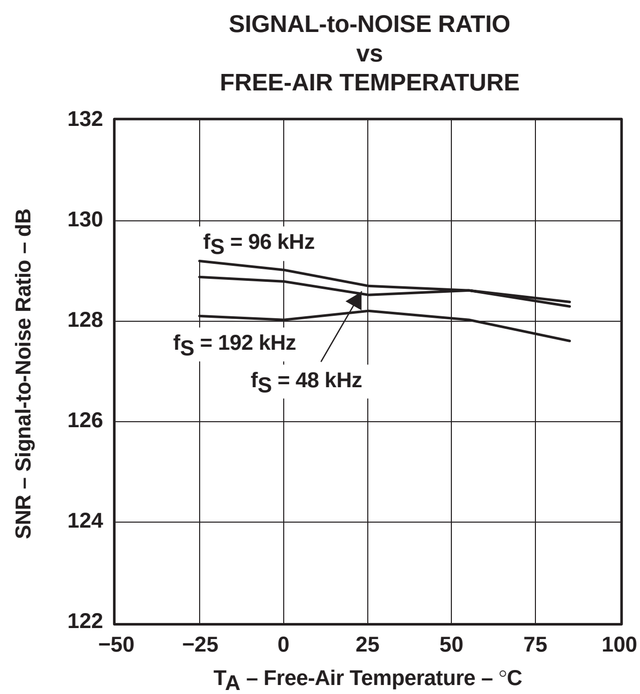


Figure 13

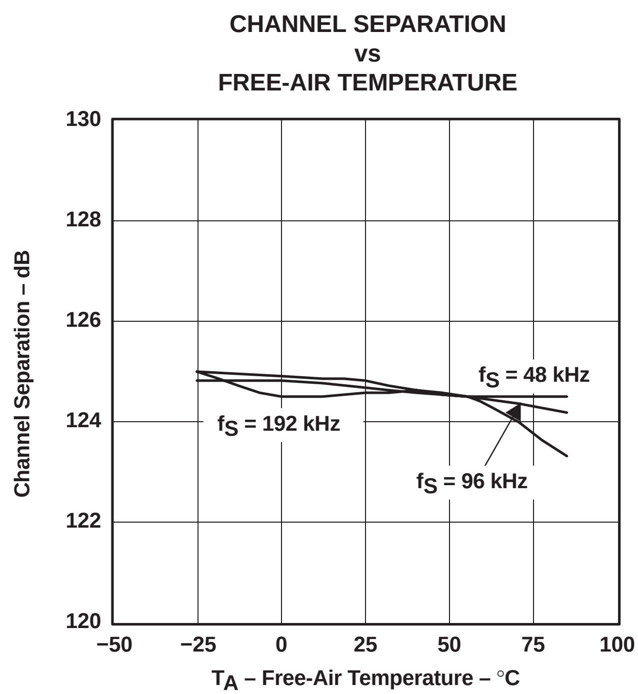
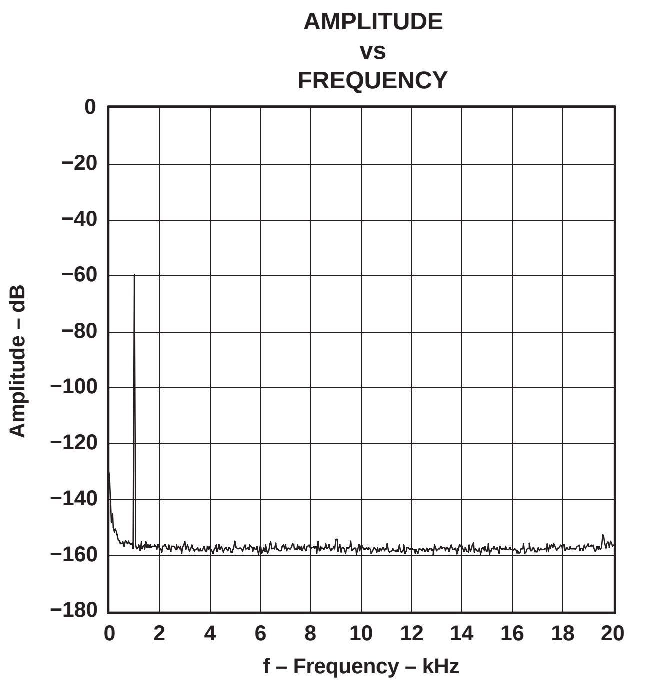


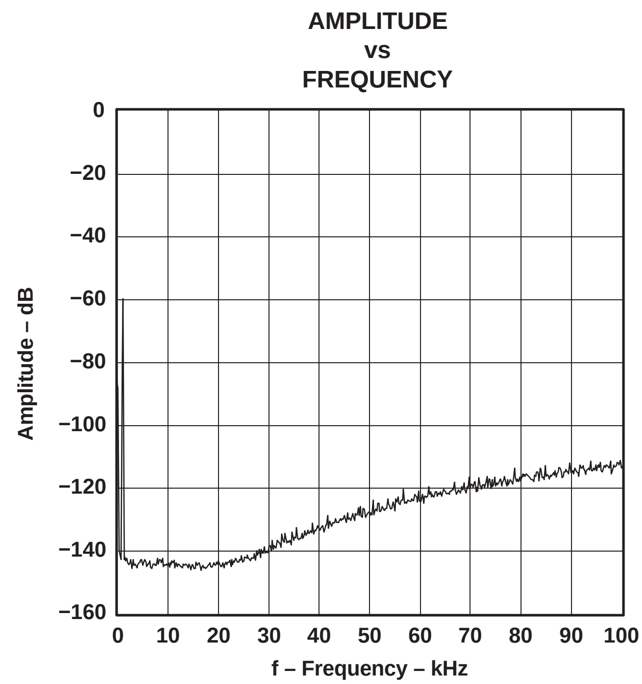
Figure 14

NOTE: V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 25 (V_{OUT} = 4.5 V rms).



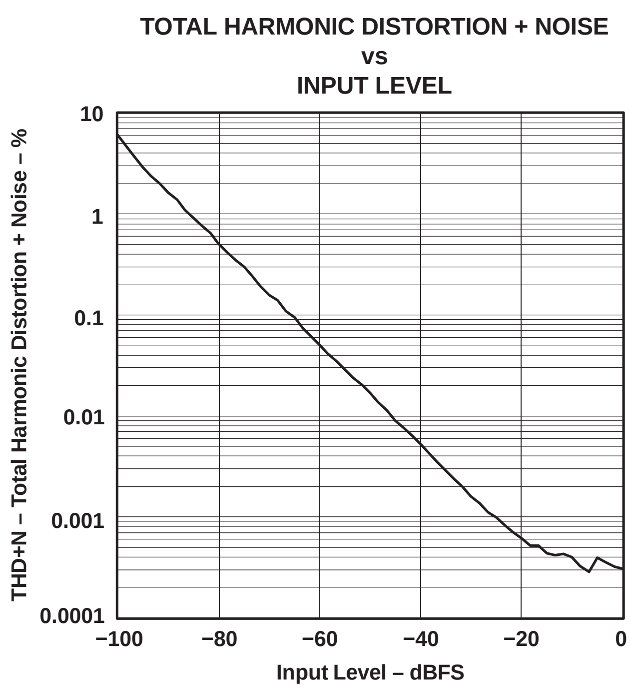
NOTE: f_S = 48 kHz, 32768 point 8 average, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 25.

Figure 15. –60-db Output Spectrum, BW = 20 kHz



NOTE: f_S = 48 kHz, 32768 point 8 average, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 25.

Figure 16. –60-db Output Spectrum, BW = 100 kHz



NOTE: f_S = 48 kHz, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 25.

Figure 17. THD+N vs Input Level

SYSTEM CLOCK AND RESET FUNCTIONS

System Clock Input

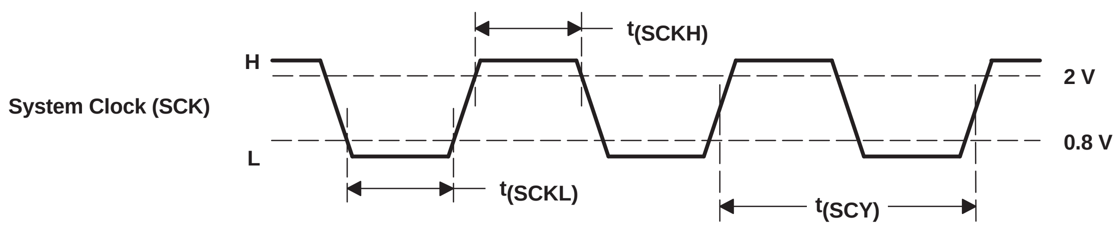
The PCM1794 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 7). The PCM1794 has a system clock detection circuit that automatically senses the frequency at which the system clock is operating. Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 18 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. One of the Texas Instruments PLL1700 family of multiclock generators is an excellent choice for providing the PCM1794 system clock.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCK}) (MHz)					
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1 kHz	5.6488	8.4672	11.2896	16.9344	22.5792	33.8688
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864
96 kHz	12.288	18.432	24.576	36.864	49.152	73.728
192 kHz	24.576	36.864	49.152	73.728	(1)	(1)

(1) This system clock rate is not supported for the given sampling frequency.



PARAMETERS		MIN	MAX	UNITS
$t_{(SCY)}$	System clock pulse cycle time	13		ns
$t_{(SCKH)}$	System clock pulse duration, HIGH	$0.4t_{(SCY)}$		ns
$t_{(SCKL)}$	System clock pulse duration, LOW	$0.4t_{(SCY)}$		ns

Figure 18. System Clock Input Timing

Power-On and External Reset Functions

The PCM1794 includes a power-on reset function. Figure 19 shows the operation of this function. With V_{DD} > 2 V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V.

The PCM1794 also includes an external reset capability using the $\overline{RST}$ input (pin 14). This allows an external controller or master reset circuit to force the PCM1794 to initialize to its default reset state.

Figure 20 shows the external reset operation and timing. The $\overline{RST}$ pin is set to logic 0 for a minimum of 20 ns. The $\overline{RST}$ pin is then set to a logic 1 state, thus starting the initialization sequence, which requires 1024 system clock periods. The external reset is especially useful in applications where there is a delay between the PCM1794 power up and system clock activation.

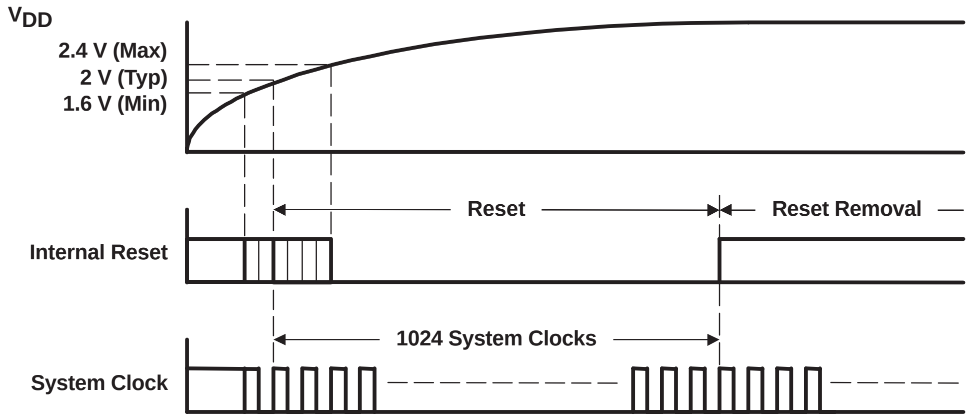
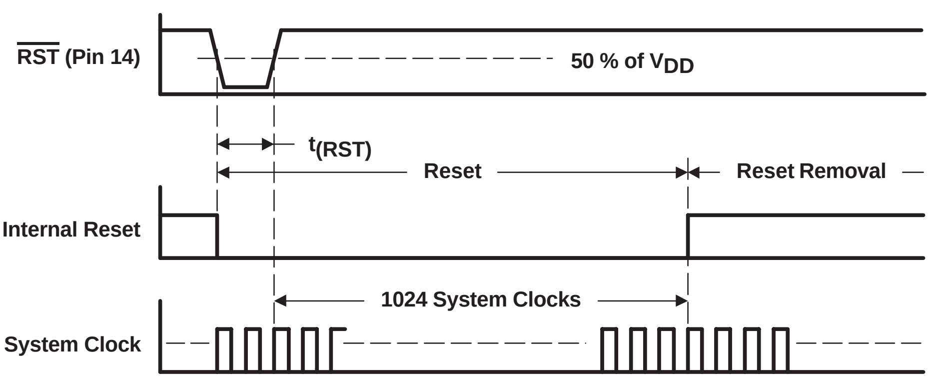


Figure 19. Power-On Reset Timing



PARAMETERS		MIN	MAX	UNITS
$t_{(RST)}$	Reset pulse duration, LOW	20		ns

Figure 20. External Reset Timing

AUDIO DATA INTERFACE

Audio Serial Interface

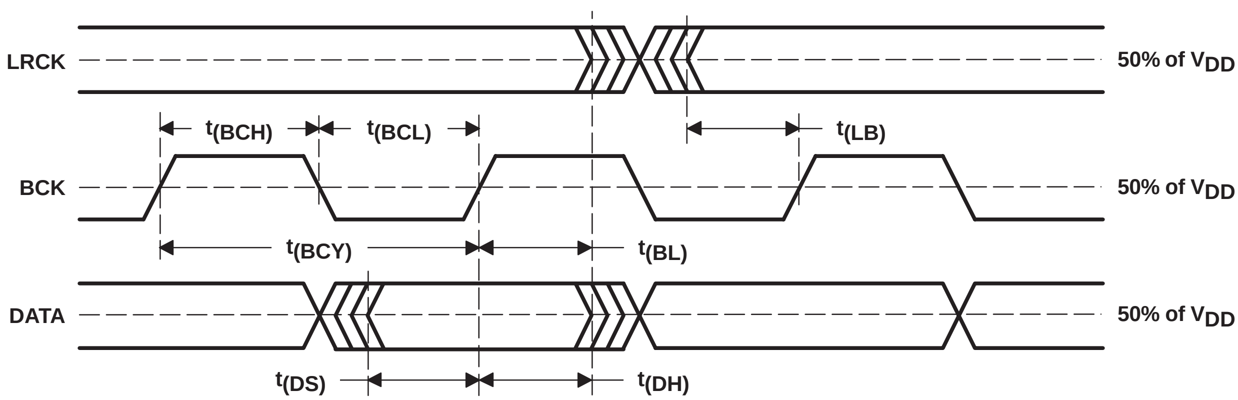
The audio interface port is a 3-wire serial port. It includes LRCK (pin 4), BCK (pin 6), and DATA (pin 5). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1794 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

The PCM1794 requires the synchronization of LRCK and the system clock, but does not need a specific phase relation between LRCK and the system clock.

If the relationship between LRCK and the system clock changes more than ±6 BCK, internal operation is initialized within $1/f_S$ and the analog outputs are forced to the bipolar zero level until resynchronization between LRCK and the system clock is completed.

PCM Audio Data Formats and Timing

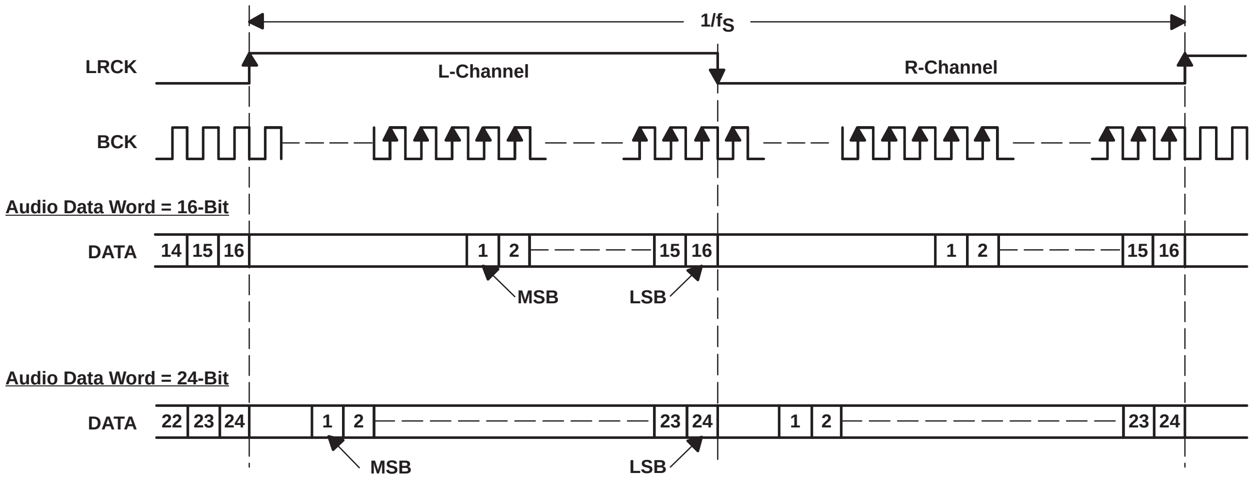
The PCM1794 supports industry-standard audio data formats, including standard right-justified, I^2S, and left-justified. The data formats are shown in Figure 22. Data formats are selected using the format bits, FMT1 (pin 12), and FMT0 (pin 11) as shown in Table 2. All formats require binary twos-complement, MSB-first audio data. Figure 21 shows a detailed timing diagram for the serial audio interface.



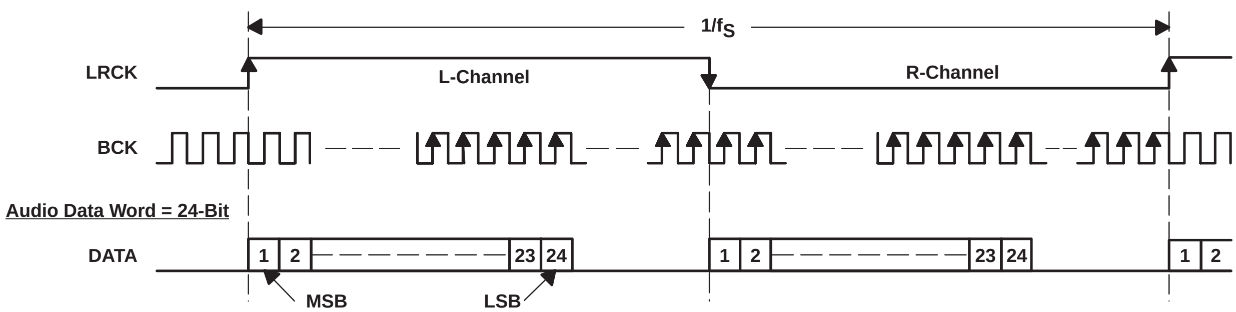
PARAMETERS		MIN	MAX	UNITS
$t_{(BCY)}$	BCK pulse cycle time	70		ns
$t_{(BCL)}$	BCK pulse duration, LOW	30		ns
$t_{(BCH)}$	BCK pulse duration, HIGH	30		ns
$t_{(BL)}$	BCK rising edge to LRCK edge	10		ns
$t_{(LB)}$	LRCK edge to BCK rising edge	10		ns
$t_{(DS)}$	DATA setup time	10		ns
$t_{(DH)}$	DATA hold time	10		ns
—	LRCK clock duty	50% ± 2 bit clocks		

Figure 21. Timing of Audio Interface

(1) Standard Data Format (Right Justified); L-Channel = HIGH, R-Channel = LOW



(2) Left Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(3) I2S Data Format; L-Channel = LOW, R-Channel = HIGH

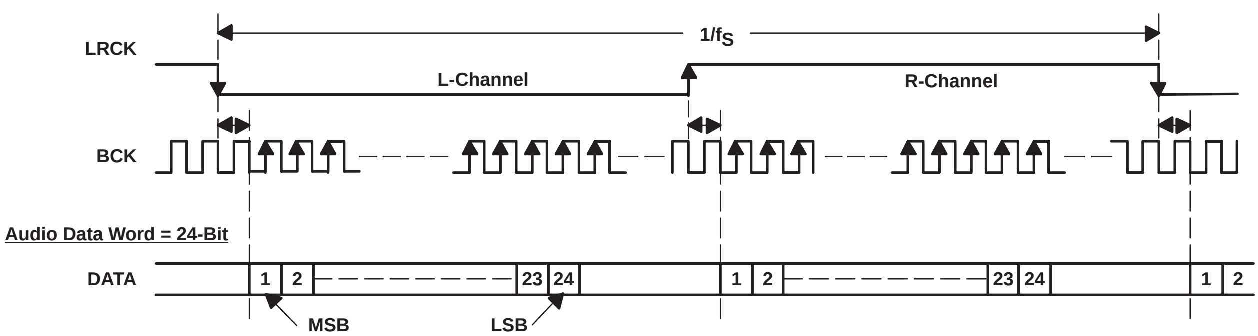


Figure 22. Audio Data Input Formats

FUNCTION DESCRIPTIONS

Audio data format

Audio format is selected using FMT0 (pin 11) and FMT1 (pin 12). The PCM1794 also supports monaural mode and DF bypass mode using MONO (pin 1) and CHSL (pin 2). The PCM1794 can select the DF rolloff characteristics.

Table 2. Audio Data Format Select

MONO	CHSL	FMT1	FMT0	FORMAT	STEREO/MONO	DF ROLLOFF
0	0	0	0	I^2S	Stereo	Sharp
0	0	0	1	Left-justified format	Stereo	Sharp
0	0	1	0	Standard, 16-bit	Stereo	Sharp
0	0	1	1	Standard, 24-bit	Stereo	Sharp
0	1	0	0	I^2S	Stereo	Slow
0	1	0	1	Left-justified format	Stereo	Slow
0	1	1	0	Standard, 16-bit	Stereo	Slow
0	1	1	1	Digital filter bypass	Mono	–
1	0	0	0	I^2S	Mono, L-channel	Sharp
1	0	0	1	Left-justified format	Mono, L-channel	Sharp
1	0	1	0	Standard, 16-bit	Mono, L-channel	Sharp
1	0	1	1	Standard, 24-bit	Mono, L-channel	Sharp
1	1	0	0	I^2S	Mono, R-channel	Sharp
1	1	0	1	Left-justified format	Mono, R-channel	Sharp
1	1	1	0	Standard, 16-bit	Mono, R-channel	Sharp
1	1	1	1	Standard, 24-bit	Mono, R-channel	Sharp

Soft Mute

The PCM1794 supports mute operation. When MUTE (pin 10) is set to HIGH, both analog outputs are transitioned to the bipolar zero level in –0.5-dB steps with a transition speed of $1/f_S$ per step. This system provides pop-free muting of the DAC output.

De-Emphasis

The PCM1794 has a de-emphasis filters for the sampling frequency of 44.1 kHz. The de-emphasis filter is controlled using DEM (pin 3).

Zero Detect

When the PCM1794 detects that the audio input data in the L-channel and the R-channel is continuously zero for 1024 LRCKs in the PCM mode or that the audio input data is continuously zero for 1024 WDCKs in the external filter mode, the PCM1794 sets ZERO (pin 13) to HIGH.

TYPICAL CONNECTION DIAGRAM

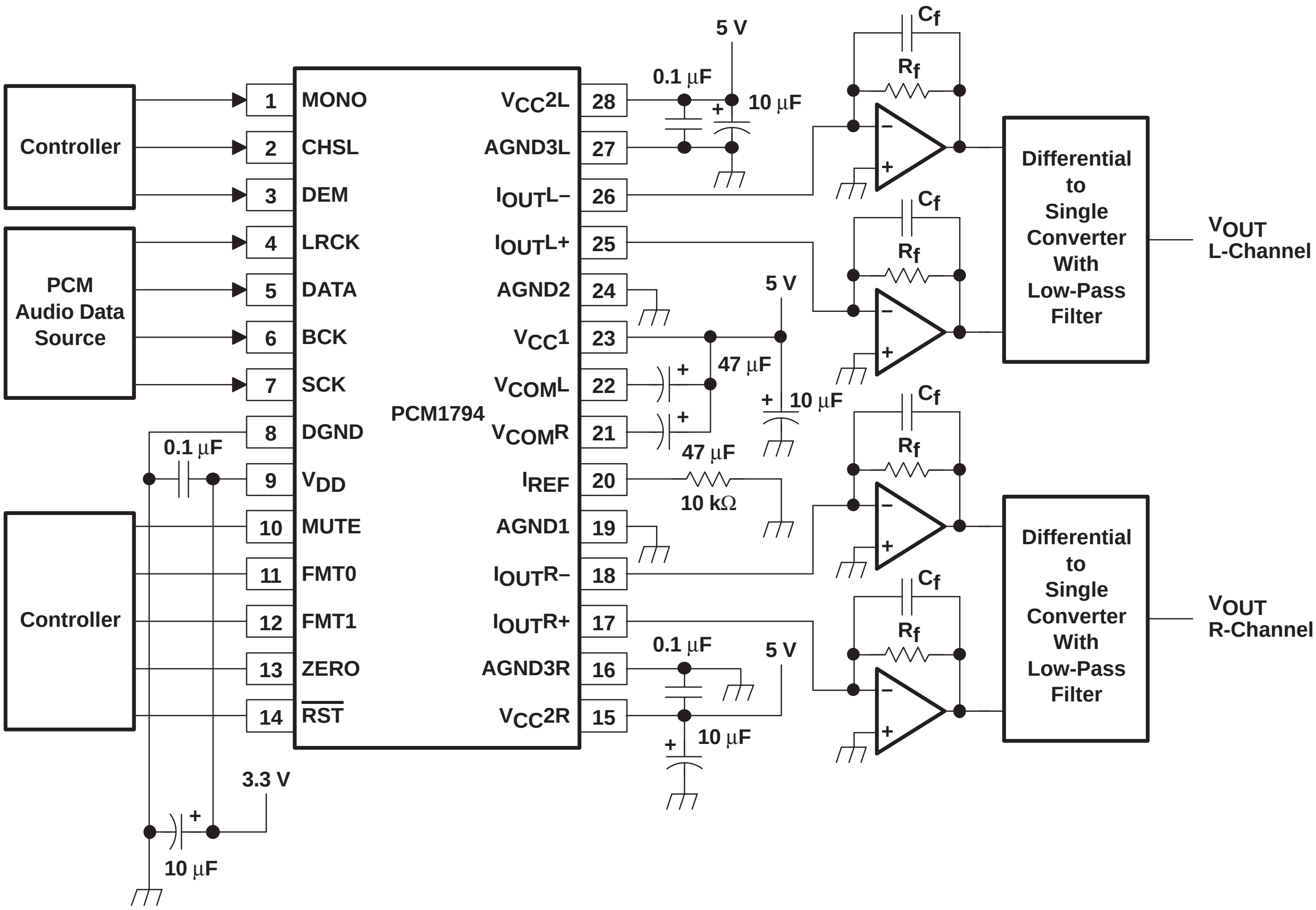


Figure 23. Typical Application Circuit

APPLICATION INFORMATION

APPLICATION CIRCUIT

The design of the application circuit is very important in order to actually realize the high S/N ratio of which the PCM1794 is capable. This is because noise and distortion that are generated in an application circuit are not negligible.

In the circuit of Figure 24, the output level is 2 V RMS, and 127 dB S/N is achieved. The circuit of Figure 25 can realize the highest performance. In this case the output level is set to 4.5 V RMS and 129 dB S/N is achieved (stereo mode). In monaural mode, if the output of the L-channel and R-channel is used as a balanced output, 132 dB S/N is achieved (see Figure 26).

I/V Section

The current of the PCM1794 on each of the output pins (I_{OUT}L+, I_{OUT}L–, I_{OUT}R+, I_{OUT}R–) is 7.8 mA p-p at 0 dB (full scale). The voltage output level of the I/V converter (Vi) is given by following equation:

$$Vi = 7.8\ mA\ p\text{–}p \times R_f$$ (R_f : feedback resistance of I/V converter)

An NE5534 operational amplifier is recommended for the I/V circuit to obtain the specified performance. Dynamic performance such as the gain bandwidth, settling time, and slew rate of the operational amplifier affects the audio dynamic performance of the I/V section.

Differential Section

The PCM1794 voltage outputs are followed by differential amplifier stages, which sum the differential signals for each channel, creating a single-ended I/V op-amp output. In addition, the differential amplifiers provide a low-pass filter function.

The operational amplifier recommended for the differential circuit is the Linear Technology LT1028, because its input noise is low.

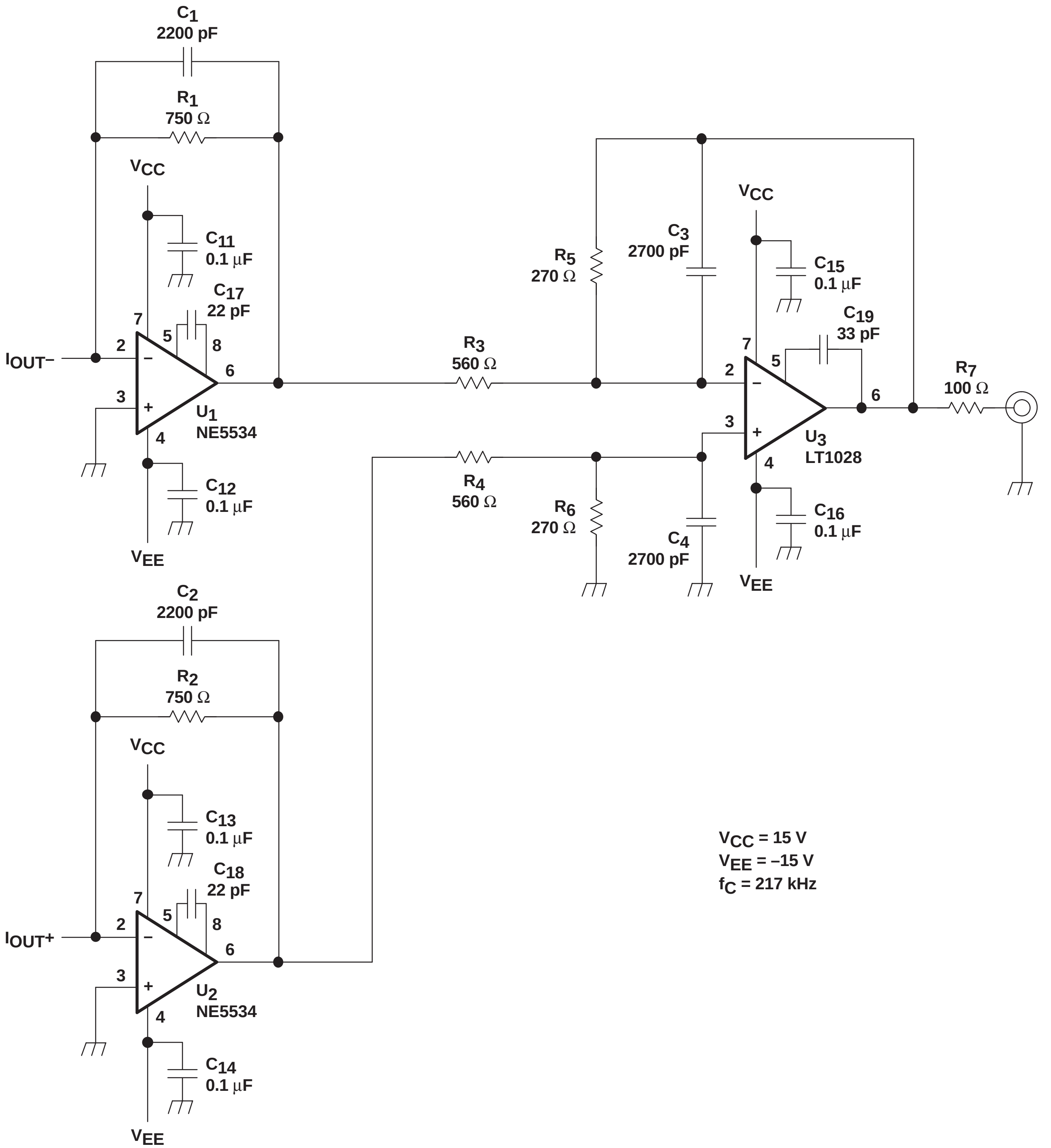


Figure 24. Measurement Circuit, V_{OUT} = 2 V RMS

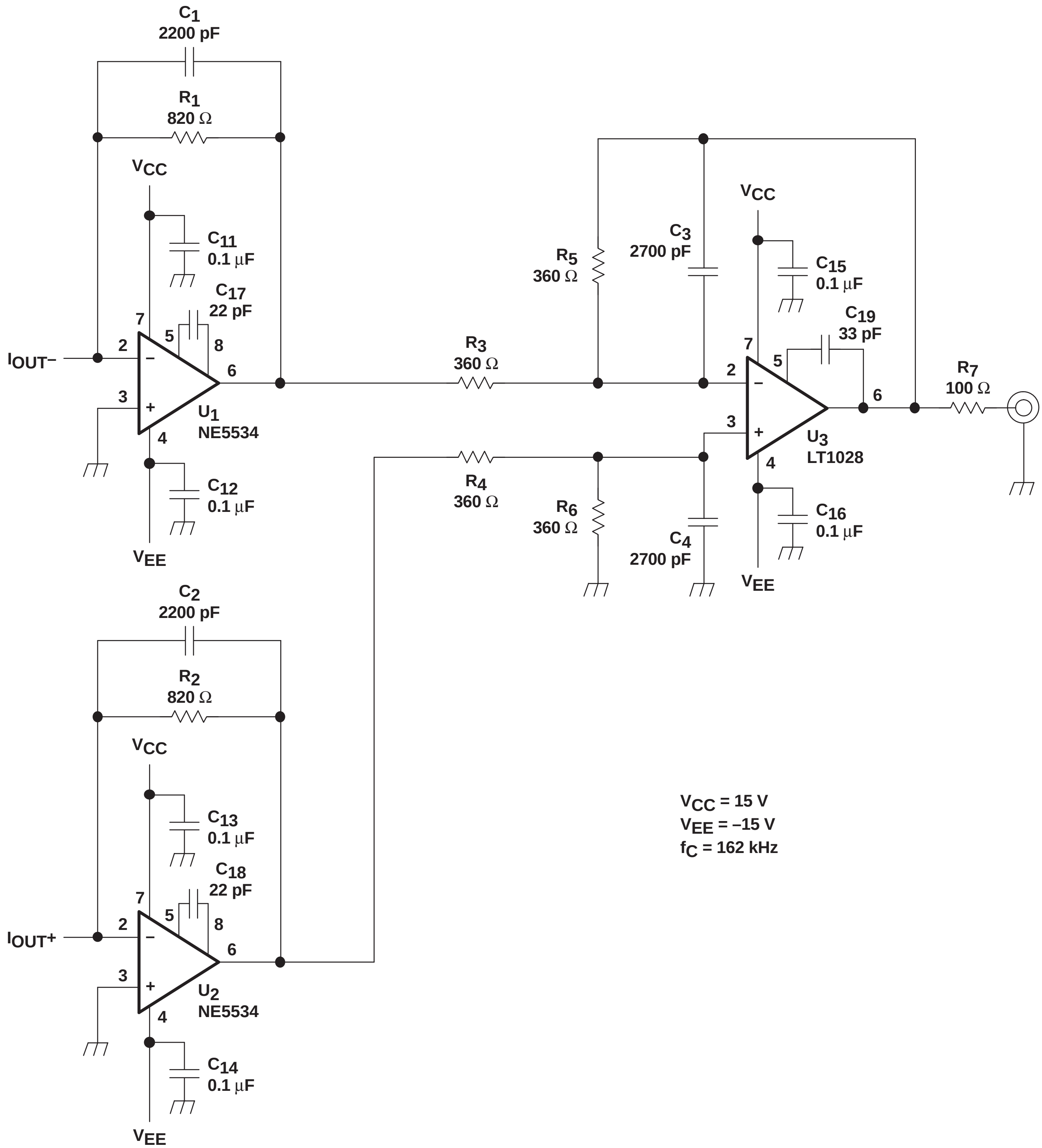


Figure 25. Measurement Circuit, V_{OUT} = 4.5 V RMS

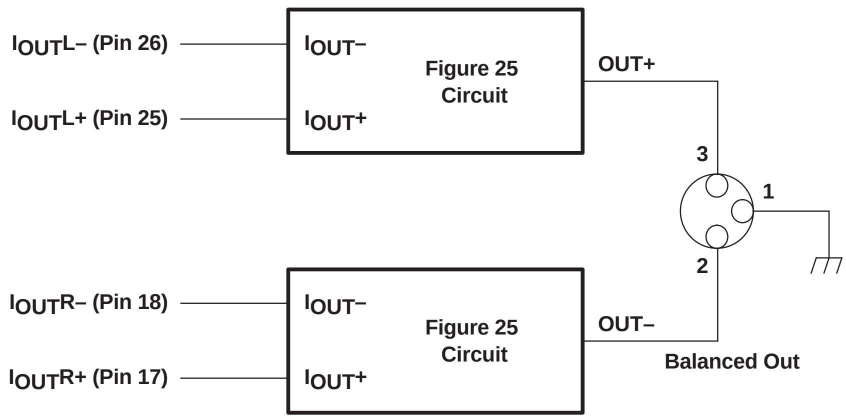


Figure 26. Measurement Circuit for Monaural Mode

APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE

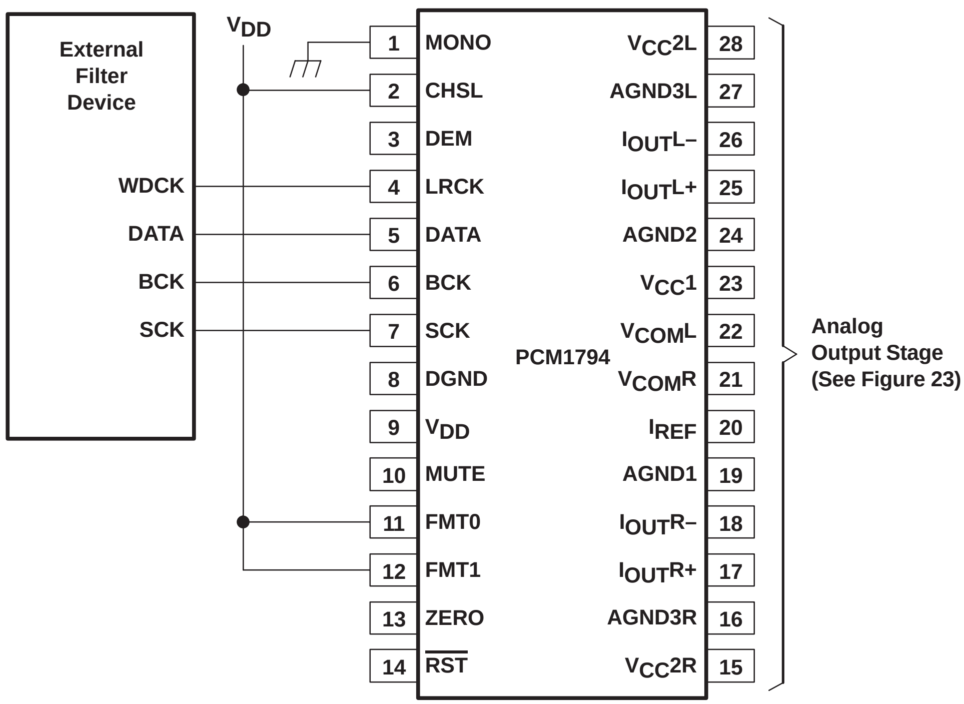


Figure 27. Connection Diagram for External DIgital Filter (Internal DF Bypass Mode) Application

Application for Interfacing With an External Digital Filter

For some applications, it may be desirable to use a programmable digital signal processor as an external digital filter to perform the interpolation function. The following pin settings enable the external digital filter application mode.

- MONO (pin 1) = LOW
- CHSL (Pin 2) = HIGH
- FMT0 (Pin 11) = HIGH
- FMT1 (pin 12) = HIGH

The pins used to provide the serial interface for the external digital filter are shown in the connection diagram of Figure 27. The word clock (WDCK) must be operated at 8× or 4× the desired sampling frequency, f_S.

System Clock (SCK) and Interface Timing

The PCM1794 in an application using an external digital filter requires the synchronization of WDCK and the system clock. The system clock is phase-free with respect to WDCK. Interface timing among WDCK, BCK, and DATA is shown in Figure 29.

Audio Format

The PCM1794 in the external digital filter interface mode supports right-justified audio formats including 24-bit audio data, as shown in Figure 28.

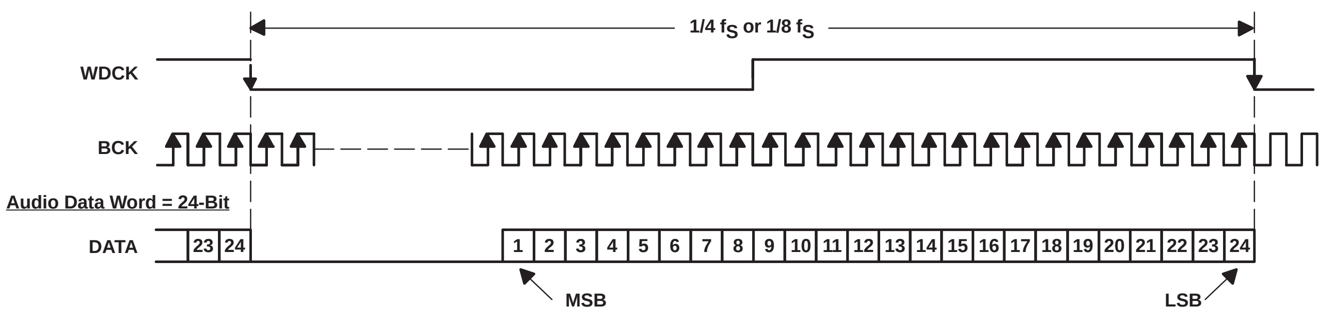
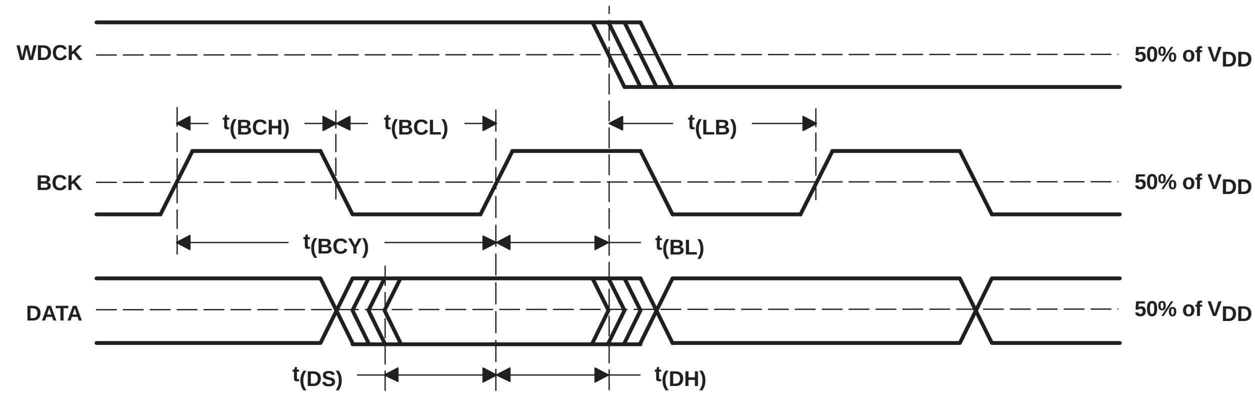


Figure 28. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application



PARAMETER		MIN	MAX	UNITS
$t_{(BCY)}$	BCK pulse cycle time	20		ns
$t_{(BCL)}$	BCK pulse duration, LOW	7		ns
$t_{(BCH)}$	BCK pulse duration, HIGH	7		ns
$t_{(BL)}$	BCK rising edge to WDCK falling edge	5		ns
$t_{(LB)}$	WDCK falling edge to BCK rising edge	5		ns
$t_{(DS)}$	DATA setup time	5		ns
$t_{(DH)}$	DATA hold time	5		ns

Figure 29. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application

THEORY OF OPERATION

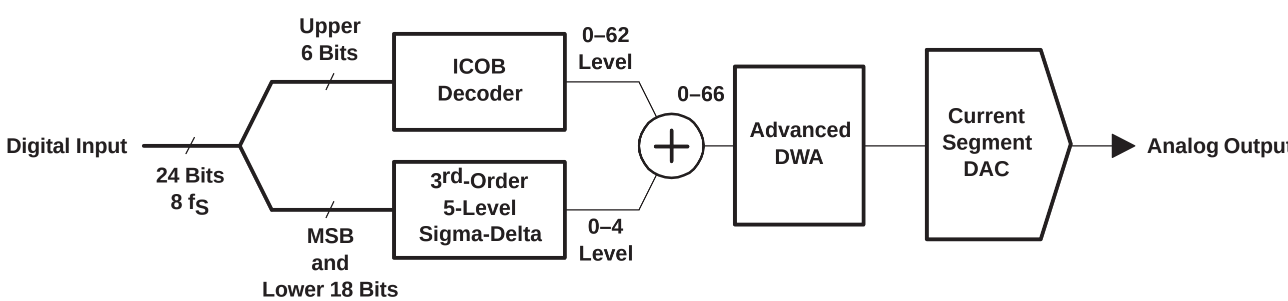


Figure 30. Advanced Segment DAC

The PCM1794 uses TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1794 provides balanced current outputs.

Digital input data via the digital filter is separated into 6 upper bits and 18 lower bits. The 6 upper bits are converted to inverted complementary offset binary (ICOB) code. The lower 18 bits, associated with the MSB, are processed by a five-level third-order delta-sigma modulator operated at 64 f_S by default. The 1 level of the modulator is equivalent to the 1 LSB of the ICOB code converter. The data groups processed in the ICOB converter and third-order delta-sigma modulator are summed together to create an up-to-66-level digital code, and then processed by data-weighted averaging (DWA) to reduce the noise produced by element mismatch. The data of up to 66 levels from the DWA is converted to an analog output in the differential-current segment section.

This architecture has overcome the various drawbacks of conventional multibit processing and also achieves excellent dynamic performance.

Analog output

The following table and Figure 31 show the relationship between the digital input code and analog output.

	800000 (–FS)	000000 (BPZ)	7FFFFF (+FS)
$I_{OUT}N$ [mA]	–2.3	–6.2	–10.1
$I_{OUT}P$ [mA]	–10.1	–6.2	–2.3
$V_{OUT}N$ [V]	–1.725	–4.65	–7.575
$V_{OUT}P$ [V]	–7.575	–4.65	–1.725
V_{OUT} [V]	–2.821	0	2.821

NOTE: $V_{OUT}N$ is the output of U1, $V_{OUT}P$ is the output of U2, and V_{OUT} is the output of U3 in the measurement circuit of Figure 24.

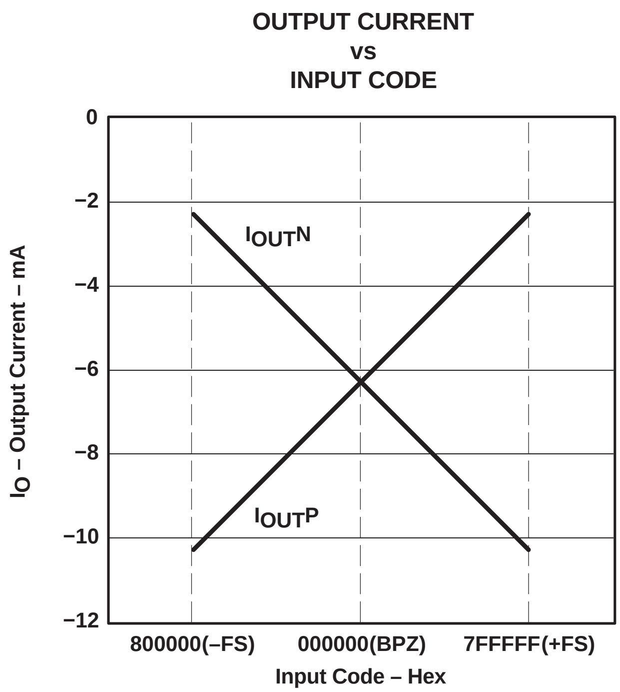


Figure 31. The Relationship Between Digital Input and Analog Output

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1794DB	NRND	SSOP	DB	28	47	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1794	
PCM1794DBG4	NRND	SSOP	DB	28	47	TBD	Call TI	Call TI	-25 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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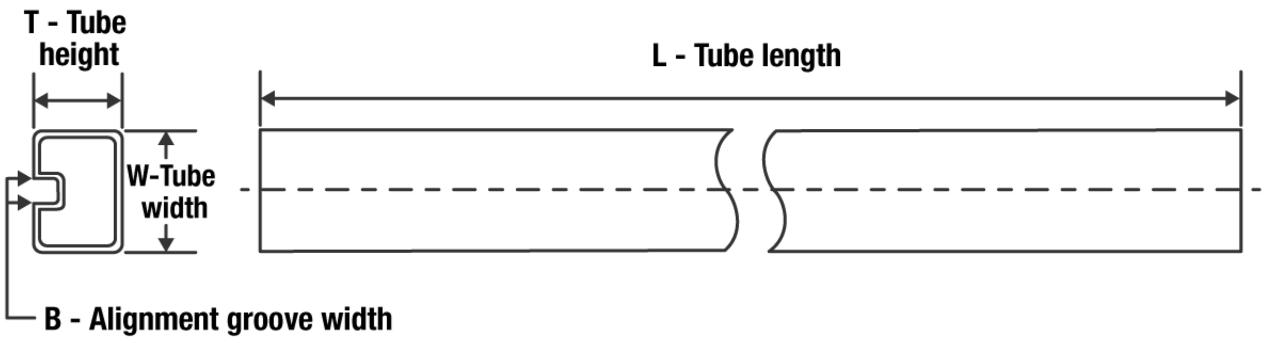
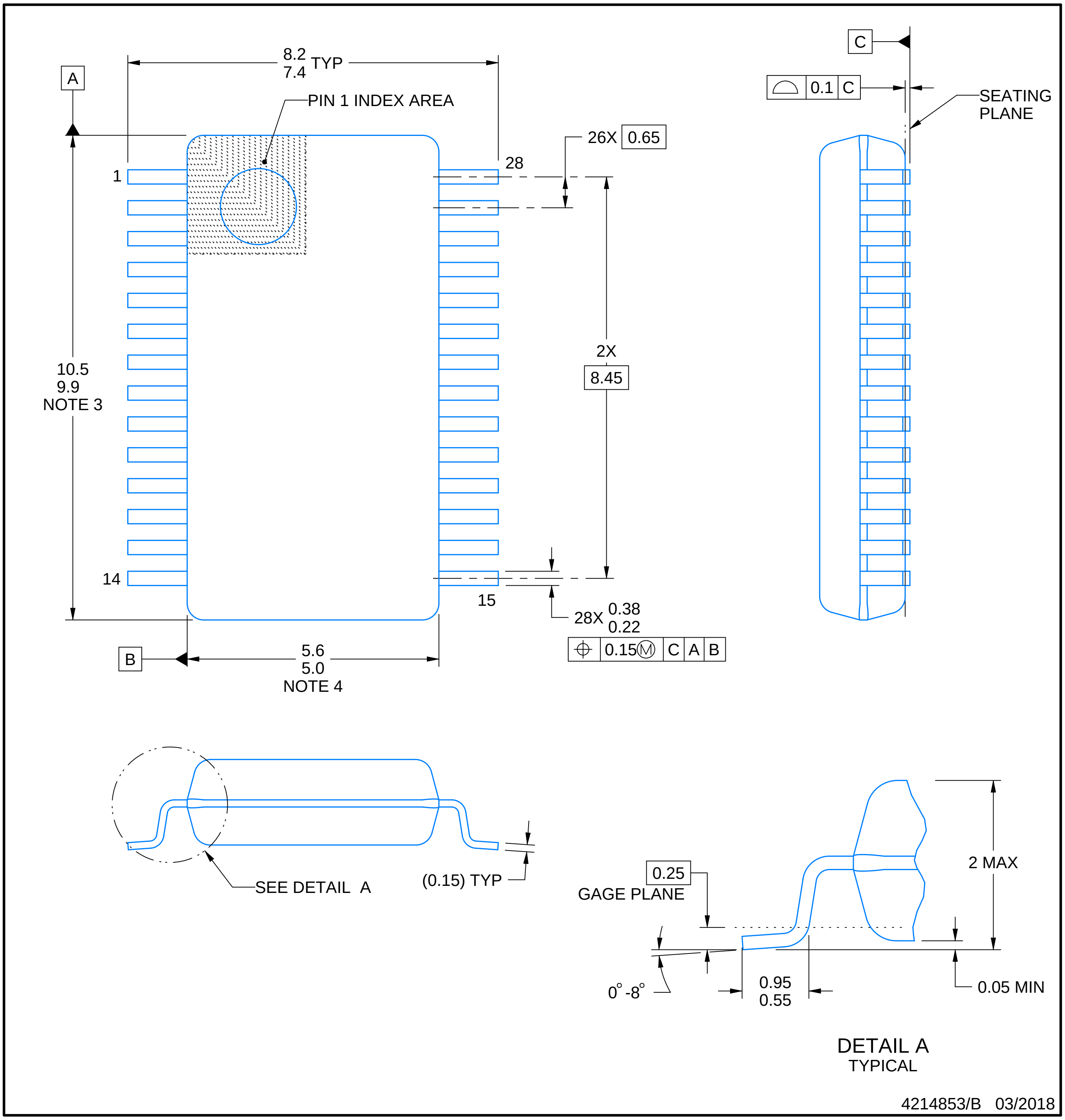
TUBE



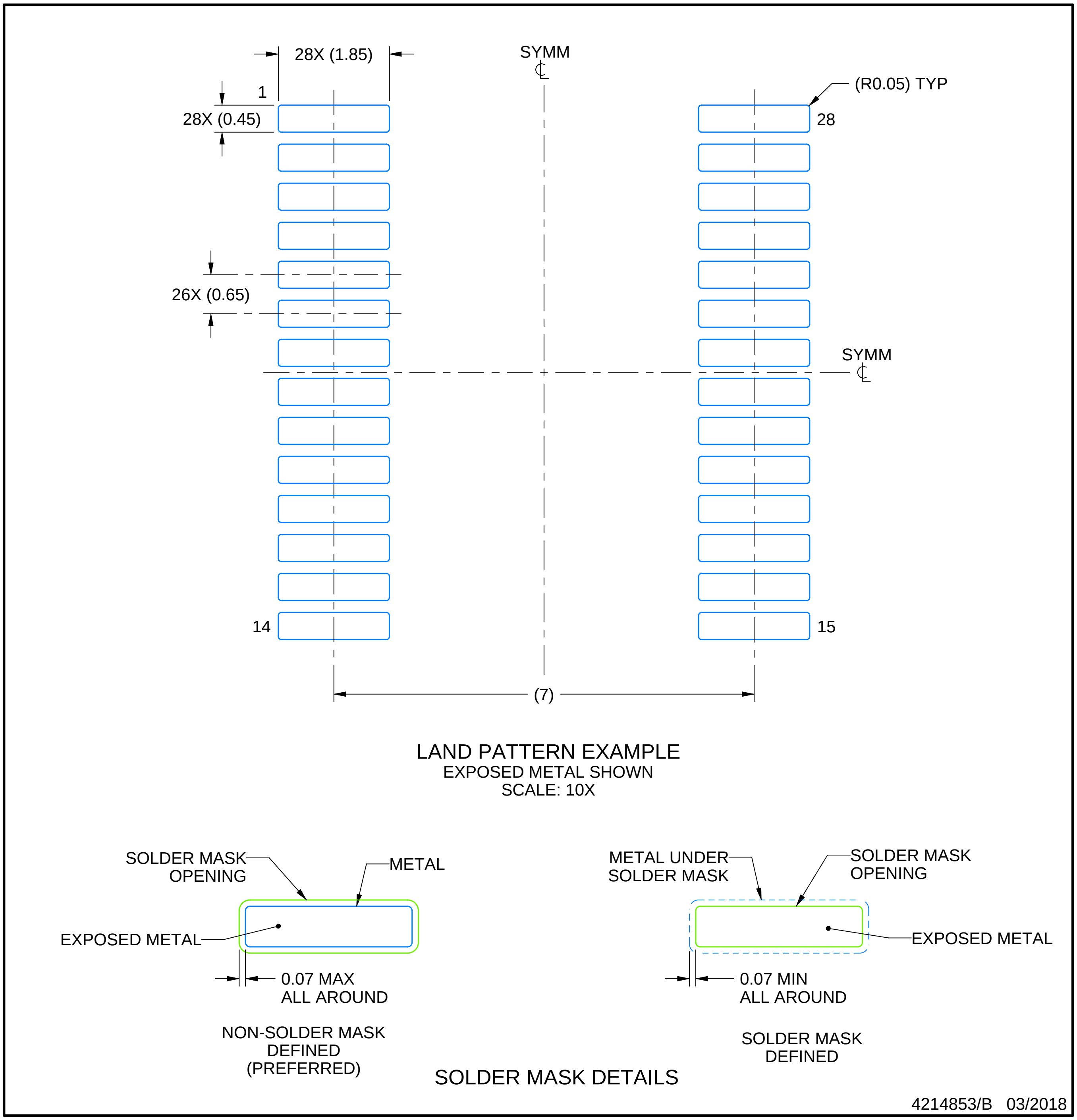
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM1794DB	DB	SSOP	28	47	500	10.6	500	9.6
PCM1794DBG4	DB	SSOP	28	47	500	10.6	500	9.6



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

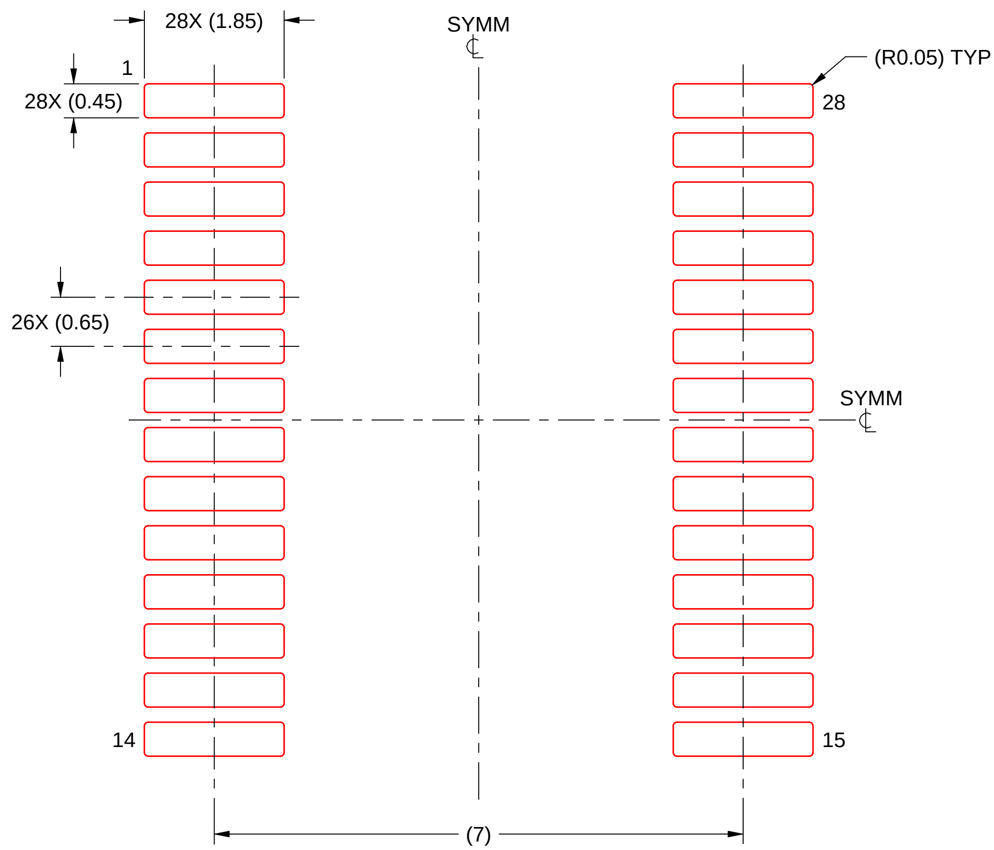


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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