

MAX19793

1500MHz to 6000MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

General Description

The MAX19793 dual general-purpose analog voltage variable attenuator (VVA) is designed to interface with 50Ω systems operating in the 1500MHz to 6000MHz frequency range. The device includes a patented control circuit that provides 23.3dB of attenuation range (per attenuator) with a typical linear control slope of 8.4dB/V.

Both attenuators share a common analog control and can be cascaded together to yield 46.6dB of total attenuation range with a typical combined linear control slope of 16.8dB/V (5V operation).

Alternatively, the on-chip 4-wire SPI-controlled 10-bit DAC can be used to control both attenuators. In addition, a step-up/down feature allows user-programmable attenuator stepping through command pulses without reprogramming the SPI interface.

The MAX19793 is a monolithic device designed using one of Maxim's proprietary SiGe BiCMOS processes. The part operates from a single +5V supply or alternatively from a single +3.3V supply. It is available in a compact 36-pin TQFN package (6mm x 6mm x 0.8mm) with an exposed pad. Electrical performance is guaranteed over the -40°C to +100°C extended temperature range.

Applications

Broadband System Applications, Including
Wireless Infrastructure Digital and
Spread-Spectrum Communication Systems
WCDMA/LTE, TD-SCDMA/TD-LTE, WiMAX®,
cdma2000®, GSM/EDGE, and
MMDS Base Stations
VSAT/Satellite Modems
Microwave Point-to-Point Systems
Lineup Gain Trim
Temperature-Compensation Circuits
Automatic Level Control (ALC)
Transmitter Gain Control
Receiver Gain Control
General Test Equipment

Features

- ◆ **Wideband Coverage**
 - ◇ 1500MHz to 6000MHz RF Frequency Range
- ◆ **High Linearity**
 - ◇ Greater Than +37dBm IIP3 Over the Full Attenuation Range
 - ◇ +23.7dBm Input P_{1dB}
- ◆ **Integrates Two Analog Attenuators in One Monolithic Device**
- ◆ **Two Convenient Control Options**
 - ◇ Single Analog Voltage
 - ◇ On-Chip SPI-Controlled 10-Bit DAC
- ◆ **Step-Up/Down Pulse Command Inputs**
- ◆ **Flexible Attenuation Control Ranges**
 - ◇ 23.3dB (Per Attenuator)
 - ◇ 46.6dB (Both Attenuators Cascaded)
- ◆ **Linear dB/V Analog Control Response Curve Simplifies Automatic Leveling Control and Gain-Trim Algorithms**
- ◆ **Excellent Attenuation Flatness Over Wide Frequency Ranges and Attenuation Settings**
- ◆ **On-Chip Comparator (for Successive Approximation Measurement of Attenuator Control Voltage)**
- ◆ **Low 13mA Supply Current**
- ◆ **Single 5V or 3.3V Supply Voltage**
- ◆ **Pin-Compatible with the MAX19791 and MAX19792**
- ◆ **Pin-Compatible with the MAX19794 with Addition of Two Shunt Capacitors**
- ◆ **PCB-Compatible with the MAX19790**
- ◆ **Lead(Pb)-Free Package**

Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX19793.related.

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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|--|-----------------|
| V _{CC} | -0.3V to +5.5V | RF Input Power at IN_A, IN_B, OUT_A, OUT_B | +20dBm |
| REF_IN..... | -0.3V to Minimum (V _{CC} + 0.3V, 3.6V) | Continuous Power Dissipation (Note 1) | 2.8W |
| REF_SEL, DAC_LOGIC, MODE, DWN, UP, DIN, CLK, \overline{CS} | -0.3V to Minimum (V _{CC} + 0.3V, 3.6V) | Operating Case Temperature Range (Note 2).... | -40°C to +100°C |
| COMP_OUT, DOUT..... | -0.3V to +3.6V | Maximum Junction Temperature..... | +150°C |
| IN_A, OUT_A, IN_B, OUT_B | -0.3V to V _{CC} + 0.3V | Storage Temperature Range..... | -65°C to +150°C |
| CTRL (except for test mode)..... | -0.3V to V _{CC} + 0.3V | Lead Temperature (soldering, 10s) | +300°C |
| Maximum CTRL Pin Load Current (CTRL configured as an output)..... | 0.3mA | Soldering Temperature (reflow) | +260°C |

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS

TQFN

| | | | |
|---|---------|--|---------|
| Junction-to-Ambient Thermal Resistance (θ_{JA}) (Notes 3, 4)..... | +36°C/W | Junction-to-Case Thermal Resistance (θ_{JC}) (Notes 1, 4)..... | +10°C/W |
|---|---------|--|---------|

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

3.3V DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.15V to 3.45V, V_{CTRL} = 1V, V_{DAC_LOGIC} = 0V, R_{DBK_EN} (D9, REG3) = logic 0, no RF signals applied, all input and output ports terminated with 50Ω through DC blocks, T_C = -40°C to +100°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, V_{CTRL} = 1V, V_{DAC_LOGIC} = 0V, R_{DBK_EN} (D9, REG3) = logic 0, T_C = +25°C, unless otherwise noted.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|-------------------|---|------|-----|------|-------|
| Supply Voltage | V _{CC} | | 3.15 | 3.3 | 3.45 | V |
| Supply Current | I _{CC} | | | 9.5 | 14 | mA |
| Control Voltage Range | V _{CTRL} | | 1 | | 2.5 | V |
| CTRL Input Resistance | R _{CTRL} | | | 1.0 | | MΩ |
| Input Current Logic-High | I _{IH} | | -1 | | +1 | μA |
| Input Current Logic-Low | I _{IL} | | -1 | | +1 | μA |
| REF_IN Voltage | | | | 1.4 | | V |
| REF_IN Input Resistance | | | | 1.0 | | MΩ |
| DAC Number of Bits | | Monotonic | | | 10 | Bits |
| Input Voltage Logic-High | V _{IH} | | 2 | | | V |
| Input Voltage Logic-Low | V _{IL} | | | | 0.8 | V |
| COMP_OUT Logic-High | | R _{DBK_EN} (D9, REG3) = logic 1, R _{LOAD} = 47kΩ | | 3.3 | | V |
| COMP_OUT Logic-Low | | R _{DBK_EN} (D9, REG3) = logic 1, R _{LOAD} = 47kΩ | | 0 | | V |

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5V DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 4.75V$ to $5.25V$, $V_{CTRL} = 1V$, $V_{DAC_LOGIC} = 0V$, $RDBK_EN$ (D9, REG3) = logic 0, no RF signals applied, all input and output ports terminated with 50Ω through DC blocks, $T_C = -40^\circ C$ to $+100^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = 5V$, $V_{CTRL} = 1V$, $V_{DAC_LOGIC} = 0V$, $RDBK_EN$ (D9, REG3) = logic 0, $T_C = +25^\circ C$, unless otherwise noted.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|------------|--|------|-----|------|------------|
| Supply Voltage | V_{CC} | | 4.75 | 5.0 | 5.25 | V |
| Supply Current | I_{CC} | | | 13 | 20 | mA |
| CTRL Voltage Range | V_{CTRL} | | 1 | | 4 | V |
| CTRL Input Resistance | R_{CTRL} | | | 124 | | k Ω |
| Input Current Logic-High | I_{IH} | | -1 | | +1 | μA |
| Input Current Logic-Low | I_{IL} | | -1 | | +1 | μA |
| REF_IN Voltage Range | | | | 1.4 | | V |
| REF_IN Input Resistance | | | | 1.0 | | M Ω |
| DAC Number of Bits | | Monotonic | | 10 | | Bits |
| Input Voltage Logic-High | V_{IH} | | 2 | | | V |
| Input Voltage Logic-Low | V_{IL} | | | | 0.8 | V |
| COMP_OUT Logic-High | | $RDBK_EN$ (D9, REG3) = logic 1, $R_{LOAD} = 47k\Omega$ | | 3.3 | | V |
| COMP_OUT Logic-Low | | $RDBK_EN$ (D9, REG3) = logic 1, $R_{LOAD} = 47k\Omega$ | | 0 | | V |

RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|----------|----------------------|------|-----|------|-------|
| RF Frequency Range | f_{RF} | (Note 6) | 1500 | | 6000 | MHz |
| RF Port Input Power | P_{RF} | Continuous operation | | | 15 | dBm |

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3.3V AC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, one attenuator, $V_{CC} = 3.15V$ to $3.45V$, RF ports are driven from 50Ω sources and loaded into 50Ω , input $P_{RF} = 0dBm$, $f_{RF} = 3500MHz$, $V_{CTRL} = 1V$ to $2.5V$, $V_{DAC_LOGIC} = 0V$, $RDBK_EN$ (D9, REG3) = logic 0, $T_C = -40^\circ C$ to $+100^\circ C$. Typical values are for $T_C = +25^\circ C$, $V_{CC} = 3.3V$, input $P_{RF} = 0dBm$, $f_{RF} = 3500MHz$, $V_{CTRL} = 1V$, $V_{DAC_LOGIC} = 0V$, $RDBK_EN$ (D9, REG3) = logic 0, unless otherwise noted.) (Notes 5, 7)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|---|-----|-----------|-----|-------|
| Insertion Loss | IL | One attenuator | | 4.0 | | dB |
| | | Two attenuators | | 7.9 | | |
| Loss Variation Over Temperature | | $T_C = -40^\circ C$ to $+100^\circ C$ | | 0.45 | | dB |
| Input P_{1dB} | IP_{1dB} | | | 18 | | dBm |
| Minimum Input Second-Order Intercept Point Over Full Attenuation Range (Note 8) | IIP2 | One attenuator, $f_{RF1} + f_{RF2}$ term, $f_{RF1} - f_{RF2} = 1MHz$, $V_{CTRL} = 1V$ to $2.5V$, $P_{RF} = 0dBm$ /tone applied to attenuator input | | 54 | | dBm |
| | | Two attenuators, $f_{RF1} + f_{RF2}$ term, $f_{RF1} - f_{RF2} = 1MHz$, $V_{CTRL} = 1V$ to $2.5V$, $P_{RF} = 0dBm$ /tone applied to attenuator input | | 52.3 | | |
| Minimum Input Third-Order Intercept Point Over Full Attenuation Range (Note 8) | IIP3 | One attenuator, $V_{CTRL} = 1V$ to $2.5V$, $f_{RF1} - f_{RF2} = 1MHz$, $P_{RF} = 0dBm$ /tone applied to attenuator input | | 33.8 | | dBm |
| | | Two attenuators, $V_{CTRL} = 1V$ to $2.0V$, $f_{RF1} - f_{RF2} = 1MHz$, $P_{RF} = 0dBm$ /tone applied to attenuator input | | 33.6 | | |
| Second Harmonic | | | | 60.8 | | dBc |
| Third Harmonic | | | | 88.6 | | dBc |
| Attenuation Control Range | | One attenuator, $V_{CTRL} = 1V$ to $2.5V$ | | 23.1 | | dB |
| | | Two attenuators, $V_{CTRL} = 1V$ to $2.5V$ | | 46.2 | | |
| Average Attenuation-Control Slope | | $V_{CTRL} = 1.4V$ to $2.3V$ | | 23.9 | | dB/V |
| Maximum Attenuation-Control Slope | | $V_{CTRL} = 1V$ to $2.5V$ | | 39 | | dB/V |
| S21 Attenuation Deviation from a Straight Line | | $V_{CTRL} = 1.4V$ to $2.1V$ | | ± 0.4 | | dB |

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5V AC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, one attenuator, $V_{CC} = 4.75V$ to $5.25V$, RF ports are driven from 50Ω sources and loaded into 50Ω , input $P_{RF} = 0dBm$, $f_{RF} = 3500MHz$, $V_{CTRL} = 1V$ to $4V$, $V_{DAC_LOGIC} = 0V$, $RDBK_EN$ (D9, REG3) = logic 0, $T_C = -40^\circ C$ to $+100^\circ C$. Typical values are for $T_C = +25^\circ C$, $V_{CC} = 5V$, input $P_{RF} = 0dBm$, $f_{RF} = 3500MHz$, $V_{CTRL} = 1V$, $V_{DAC_LOGIC} = 0V$, $RDBK_EN$ (D9, REG3) = logic 0, unless otherwise noted.) (Notes 5, 7)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|---|-----|-------|-----|-------|
| Insertion Loss | IL | One attenuator | | 3.9 | | dB |
| | | Two attenuators | | 7.6 | | |
| Loss Variation Over Temperature | | $T_C = -40^\circ C$ to $+100^\circ C$ | | 0.45 | | dB |
| Input P_{1dB} | IP_{1dB} | | | 23.7 | | dBm |
| Minimum Input Second-Order Intercept Point Over Full Attenuation Range (Note 8) | IIP2 | One attenuator, $f_{RF1} + f_{RF2}$ term, $f_{RF1} - f_{RF2} = 1MHz$, $V_{CTRL} = 1V$ to $4V$, $P_{RF} = 0dBm$ /tone applied to attenuator input | | 65 | | dBm |
| | | Two attenuators, $f_{RF1} + f_{RF2}$ term, $f_{RF1} - f_{RF2} = 1MHz$, $V_{CTRL} = 1V$ to $3.5V$, $P_{RF} = 0dBm$ /tone applied to attenuator input | | 63 | | |
| Minimum Input Third-Order Intercept Point Over Full Attenuation Range (Note 8) | IIP3 | One attenuator, V_{CTRL} from $1V$ to $4V$, $f_{RF1} - f_{RF2} = 1MHz$, $P_{RF} = 0dBm$ /tone applied to attenuator input | | 38 | | dBm |
| | | Two attenuators, V_{CTRL} from $1V$ to $2.8V$, $f_{RF1} - f_{RF2} = 1MHz$, $P_{RF} = 0dBm$ /tone applied to attenuator input | | 37 | | |
| Second Harmonic | | | | 72.2 | | dBc |
| Third Harmonic | | | | 104.7 | | dBc |
| Attenuation Control Range | | One attenuator, $V_{CTRL} = 1V$ to $4V$ | | 23.3 | | dB |
| | | Two attenuators, $V_{CTRL} = 1V$ to $4V$ | | 46.6 | | |
| Average Attenuation-Control Slope | | $V_{CTRL} = 1.4V$ to $3.1V$ | | 8.4 | | dB/V |
| Maximum Attenuation-Control Slope | | $V_{CTRL} = 1V$ to $3.5V$ | | 30 | | dB/V |
| Attenuation Flatness Over 125MHz Band | | $V_{CTRL} = 1V$ to $4V$ | | 0.25 | | dB |

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5V AC ELECTRICAL CHARACTERISTICS (continued)

(Typical Application Circuit, one attenuator, $V_{CC} = 4.75V$ to $5.25V$, RF ports are driven from 50Ω sources and loaded into 50Ω , input $P_{RF} = 0dBm$, $f_{RF} = 3500MHz$, $V_{CTRL} = 1V$ to $4V$, $V_{DAC_LOGIC} = 0V$, $RDBK_EN$ (D9, REG3) = logic 0, $T_C = -40^\circ C$ to $+100^\circ C$. Typical values are for $T_C = +25^\circ C$, $V_{CC} = 5V$, input $P_{RF} = 0dBm$, $f_{RF} = 3500MHz$, $V_{CTRL} = 1V$, $V_{DAC_LOGIC} = 0V$, $RDBK_EN$ (D9, REG3) = logic 0, unless otherwise noted.) (Notes 5, 7)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------|--|-----|-----------|-----|---------|
| CTRL Switching Time (Note 9) | | 13dB to 0dB range | | 350 | | ns |
| | | 0dB to 13dB range | | 730 | | |
| \overline{CS} Switching Time (Note 10) | | 14dB to 0dB range | | 675 | | ns |
| | | 0dB to 14dB range | | 2300 | | |
| MODE Switching Time (Note 11) | | 15dB to 0dB range (MODE 1 to 0) | | 700 | | ns |
| | | 0dB to 15dB range (MODE 0 to 1) | | 2650 | | |
| Input Return Loss | | | | 19 | | dB |
| Output Return Loss | | | | 17 | | dB |
| Group Delay | | Input/output 50Ω lines deembedded | | 200 | | ps |
| Group Delay Flatness Over 125MHz Band | | Peak to peak | | 20 | | ps |
| Group Delay Change | | $V_{CTRL} = 1V$ to $4V$ | | -120 | | ps |
| Insertion Phase Change vs. Attenuation Control | | $V_{CTRL} = 1V$ to $4V$ | | 28 | | Degrees |
| S21 Attenuation Deviation from a Straight Line | | $V_{CTRL} = 1.4V$ to $3.1V$ | | ± 0.4 | | dB |
| SERIAL PERIPHERAL INTERFACE (SPI) | | | | | | |
| Maximum Clock Speed | | | | 20 | | MHz |
| Data-to-Clock Setup Time | t_{CS} | (Note 12) | | 2 | | ns |
| Data-to-Clock Hold Time | t_{CH} | (Note 12) | | 2.5 | | ns |
| \overline{CS} -to-CLK Setup Time | t_{EWS} | (Note 12) | | 3 | | ns |
| \overline{CS} Positive Pulse Width | t_{EW} | (Note 12) | | 7 | | ns |
| Clock Pulse Width | t_{CW} | (Note 12) | | 5 | | ns |

Note 5: Production tested at $T_C = +100^\circ C$. All other temperatures are guaranteed by design and characterization.

Note 6: Recommended functional range. Not production tested. Operation outside this range is possible, but with degraded performance of some parameters.

Note 7: All limits include external component losses, connectors and PCB traces. Output measurements taken at the RF port of the *Typical Application Circuit*.

Note 8: $f_{RF1} = 3501MHz$, $f_{RF2} = 3500MHz$, $PRF = 0dBm/$ tone applied to attenuator input.

Note 9: Switching time measured from 50% of the CTRL signal to when the RF output settles to $\pm 1dB$ ($R3 = 0\Omega$).

Note 10: Switching time measured from when \overline{CS} is asserted to when the RF output settles to $\pm 1dB$.

Note 11: Switching time measured from when MODE is asserted to when the RF output settles to $\pm 1dB$.

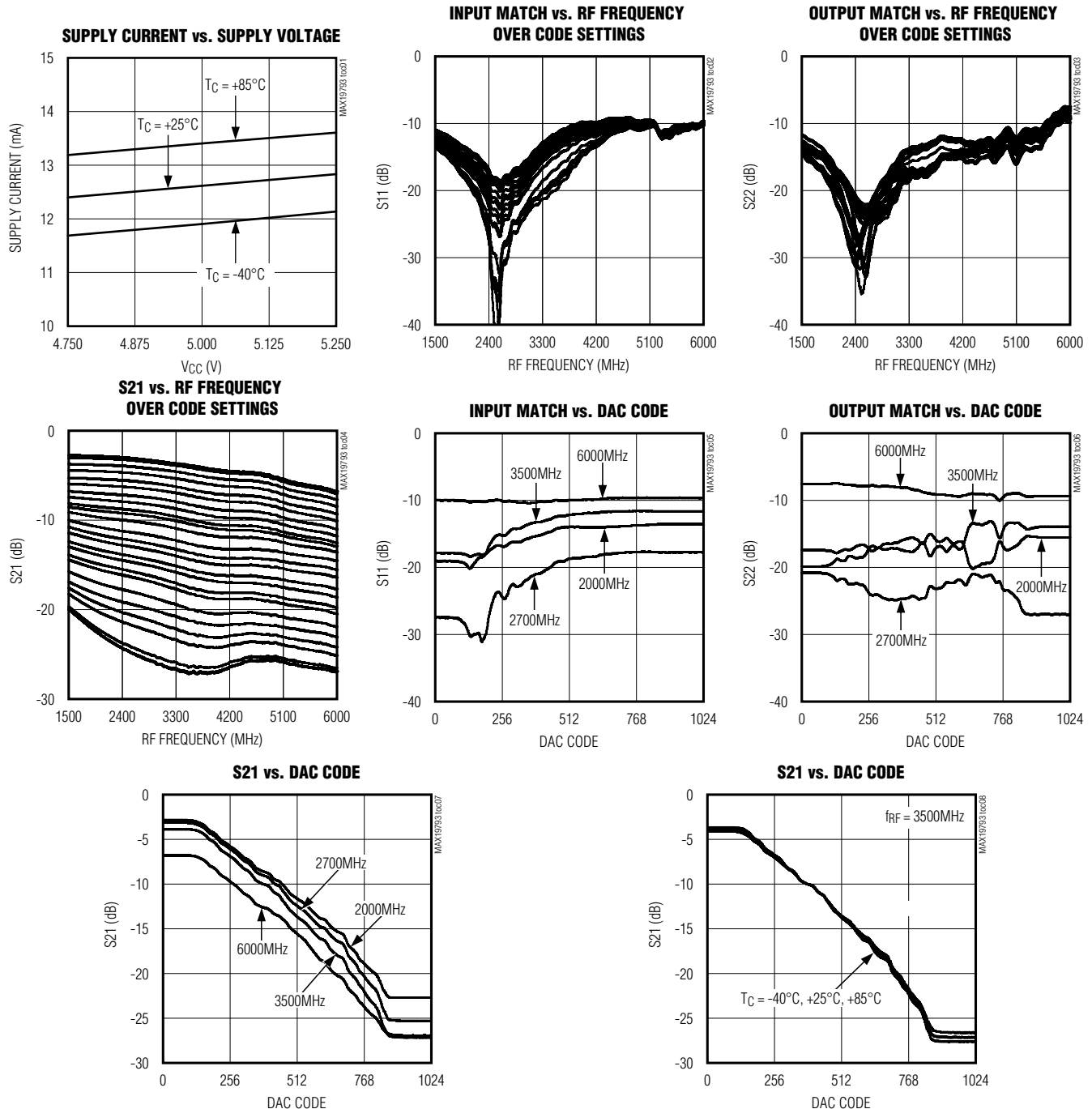
Note 12: Typical minimum time for proper SPI operation.

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Typical Operating Characteristics

(Typical Application Circuit, $V_{CC} = 5V$, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω , $V_{DAC_LOGIC} = 0V$, $RDBK_EN = \text{Logic } 0$, $V_{CTRL} = 1V$, $P_{IN} = 0\text{dBm}$, $f_{RF} = 3500\text{MHz}$, $T_C = +25^\circ\text{C}$, unless otherwise noted.)

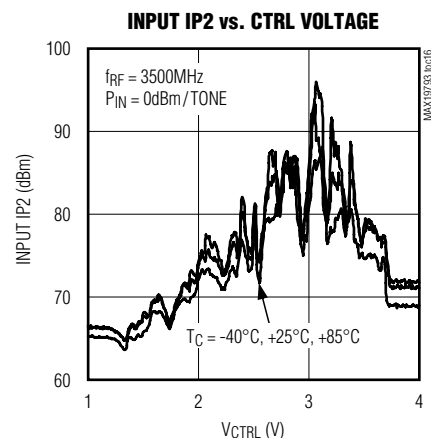
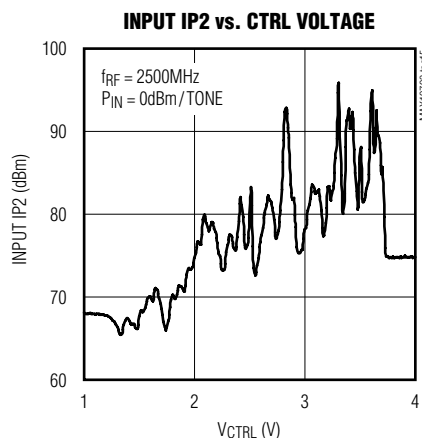
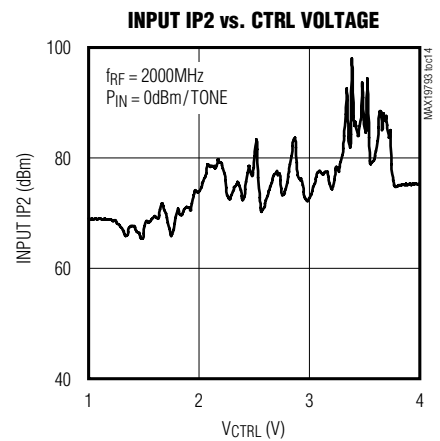
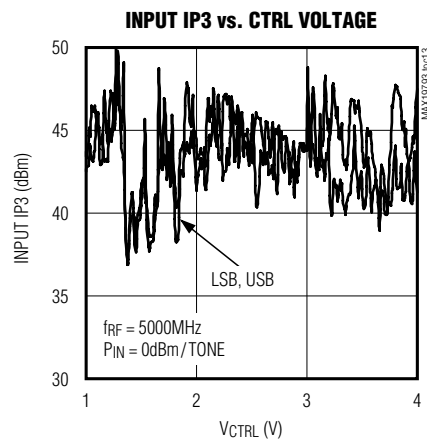
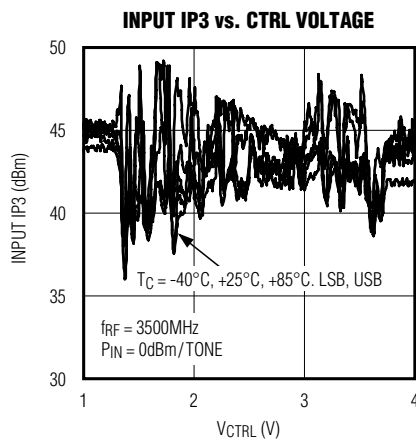
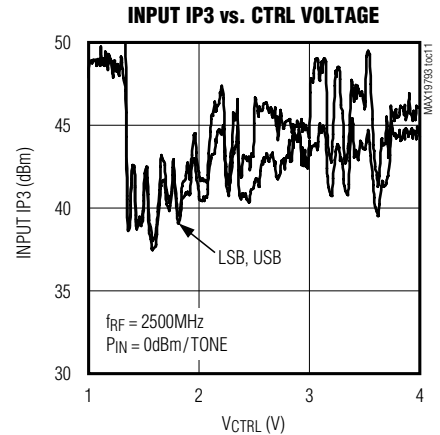
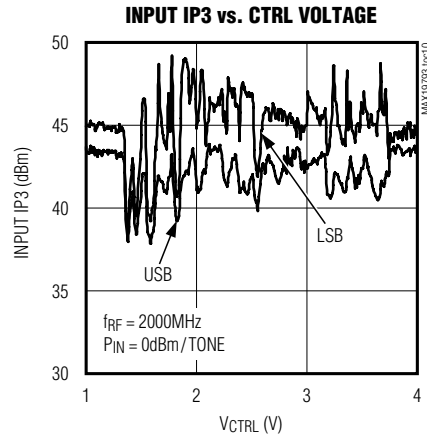
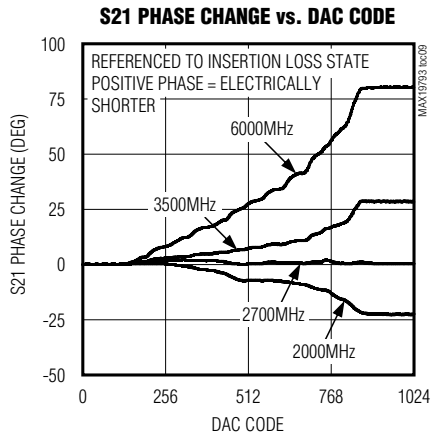


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Typical Operating Characteristics (continued)

(Typical Application Circuit, $V_{CC} = 5V$, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, $V_{DAC_LOGIC} = 0V$, $RDBK_EN = \text{Logic } 0$, $V_{CTRL} = 1V$, $P_{IN} = 0\text{dBm}$, $f_{RF} = 3500\text{MHz}$, $T_C = +25^\circ\text{C}$, unless otherwise noted.)

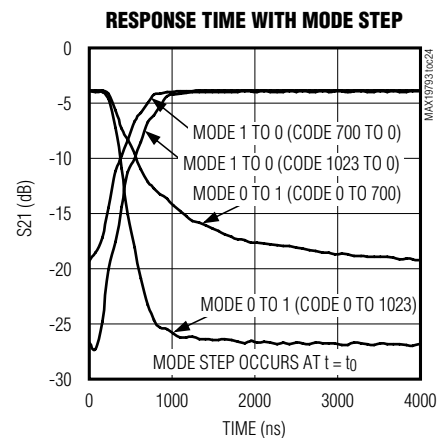
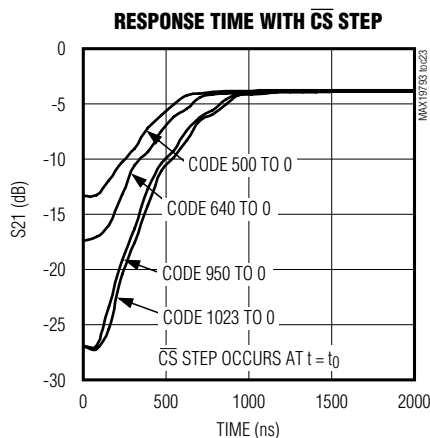
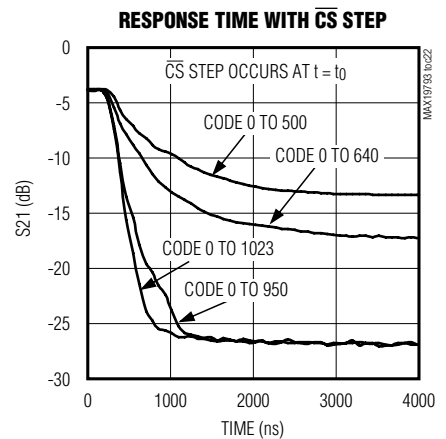
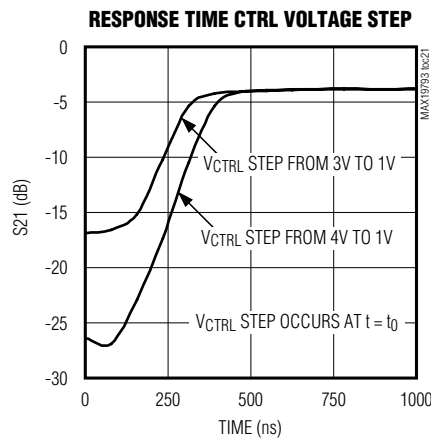
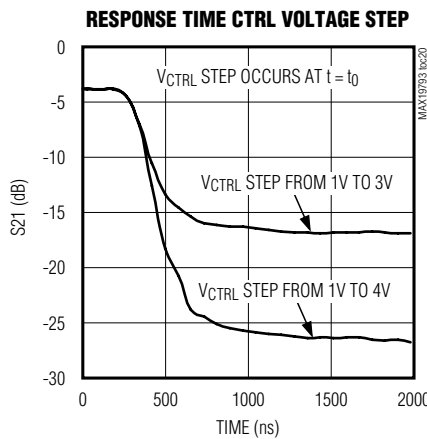
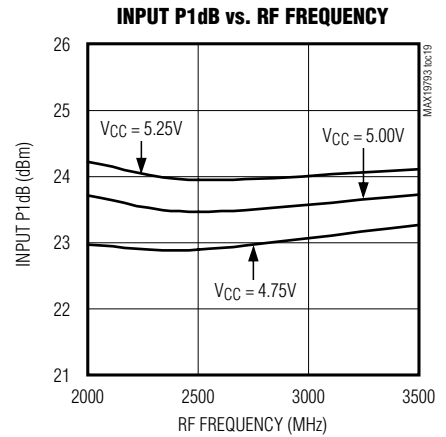
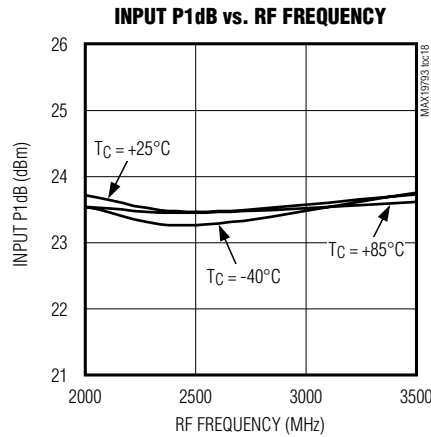
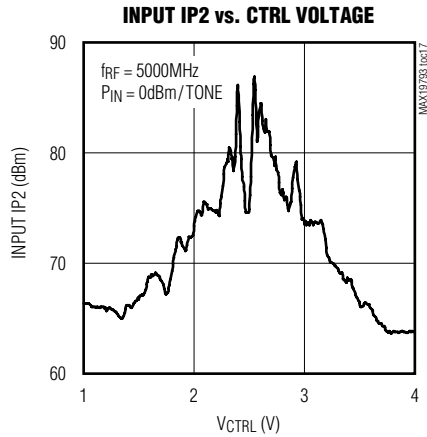


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Typical Operating Characteristics (continued)

(Typical Application Circuit, $V_{CC} = 5V$, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, $V_{DAC_LOGIC} = 0V$, $RDBK_EN = \text{Logic } 0$, $V_{CTRL} = 1V$, $P_{IN} = 0\text{dBm}$, $f_{RF} = 3500\text{MHz}$, $T_C = +25^\circ\text{C}$, unless otherwise noted.)

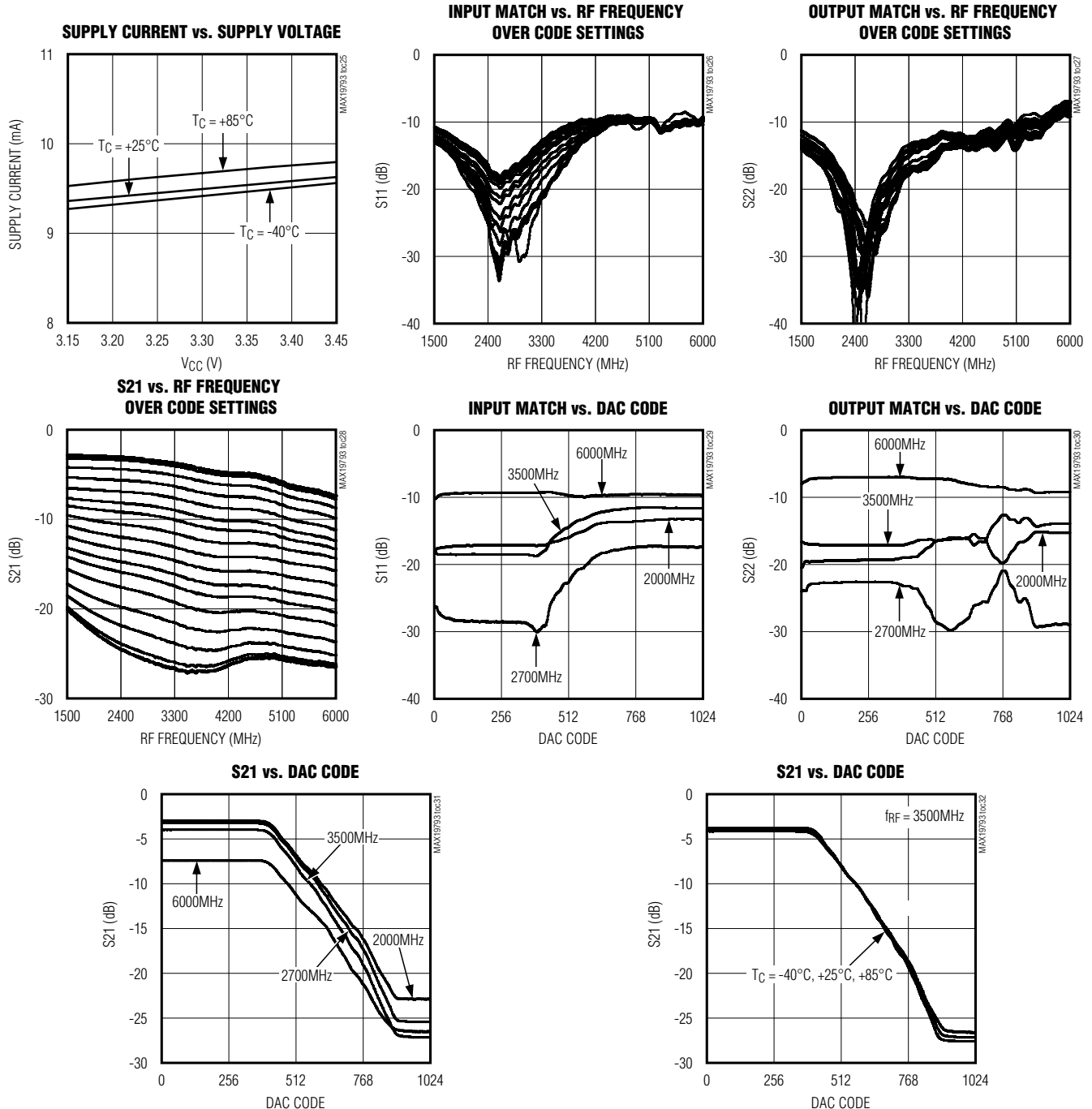


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1500MHz to 6000MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Typical Operating Characteristics

(Typical Application Circuit, $V_{CC} = 3.3V$, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, $V_{DAC_LOGIC} = 0V$, $RDBK_EN = Logic\ 0$, $V_{CTRL} = 1V$, $P_{IN} = 0dBm$, $f_{RF} = 3500MHz$, $T_C = +25^\circ C$, unless otherwise noted.)

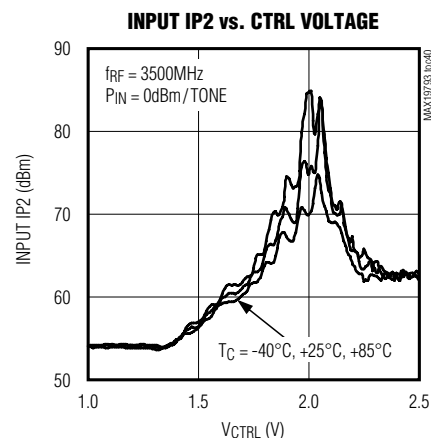
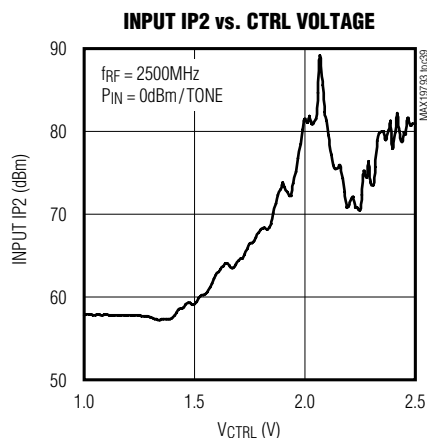
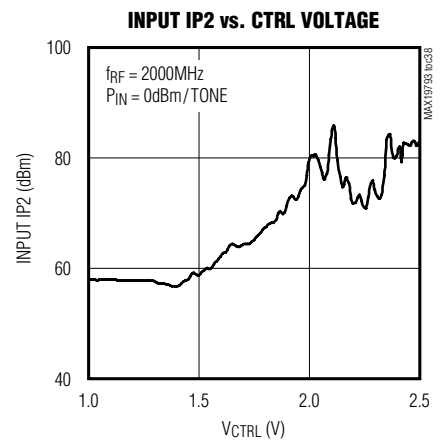
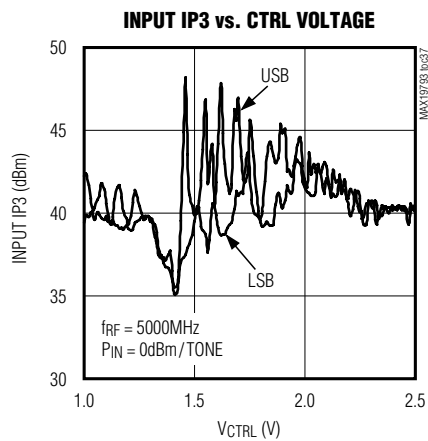
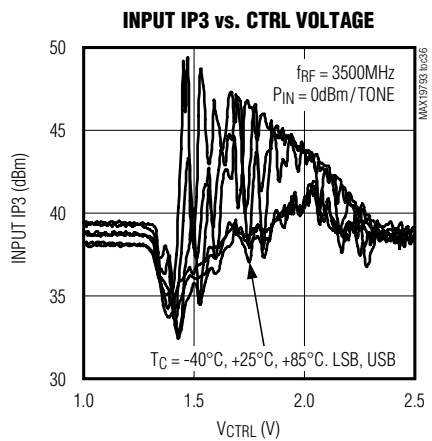
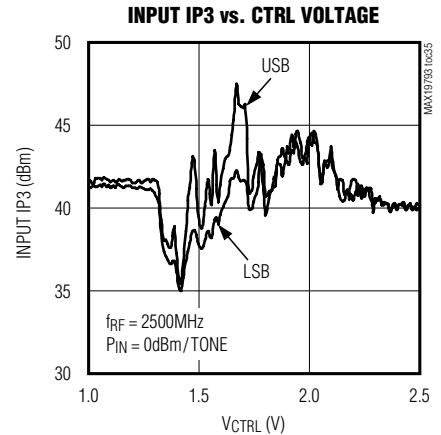
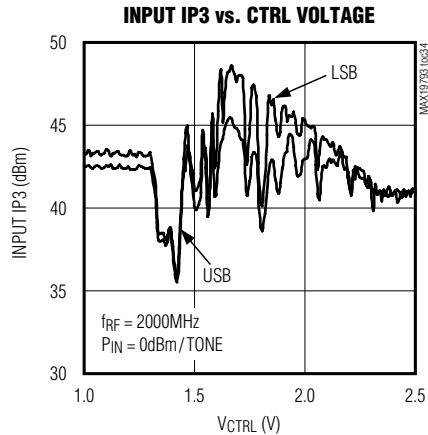
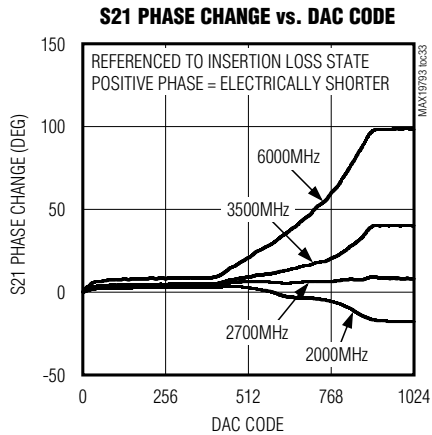


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1500MHz to 6000MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Typical Operating Characteristics (continued)

(Typical Application Circuit, $V_{CC} = 3.3V$, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω , $V_{DAC_LOGIC} = 0V$, $RDBK_EN = \text{logic } 0$, $V_{CTRL} = 1V$, $P_{IN} = 0\text{dBm}$, $f_{RF} = 3500\text{MHz}$, $T_C = +25^\circ\text{C}$, unless otherwise noted.)

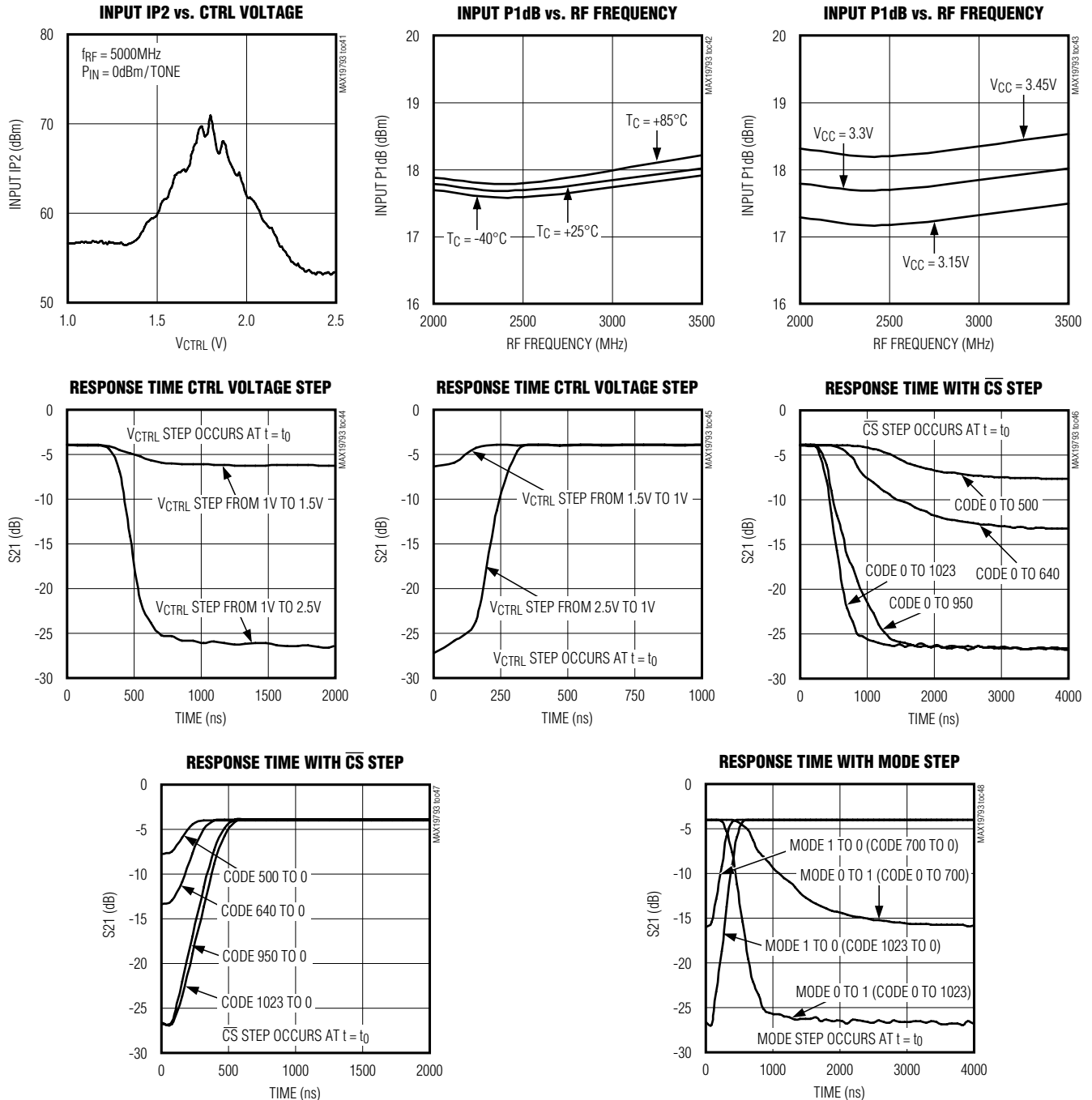


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1500MHz to 6000MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Typical Operating Characteristics (continued)

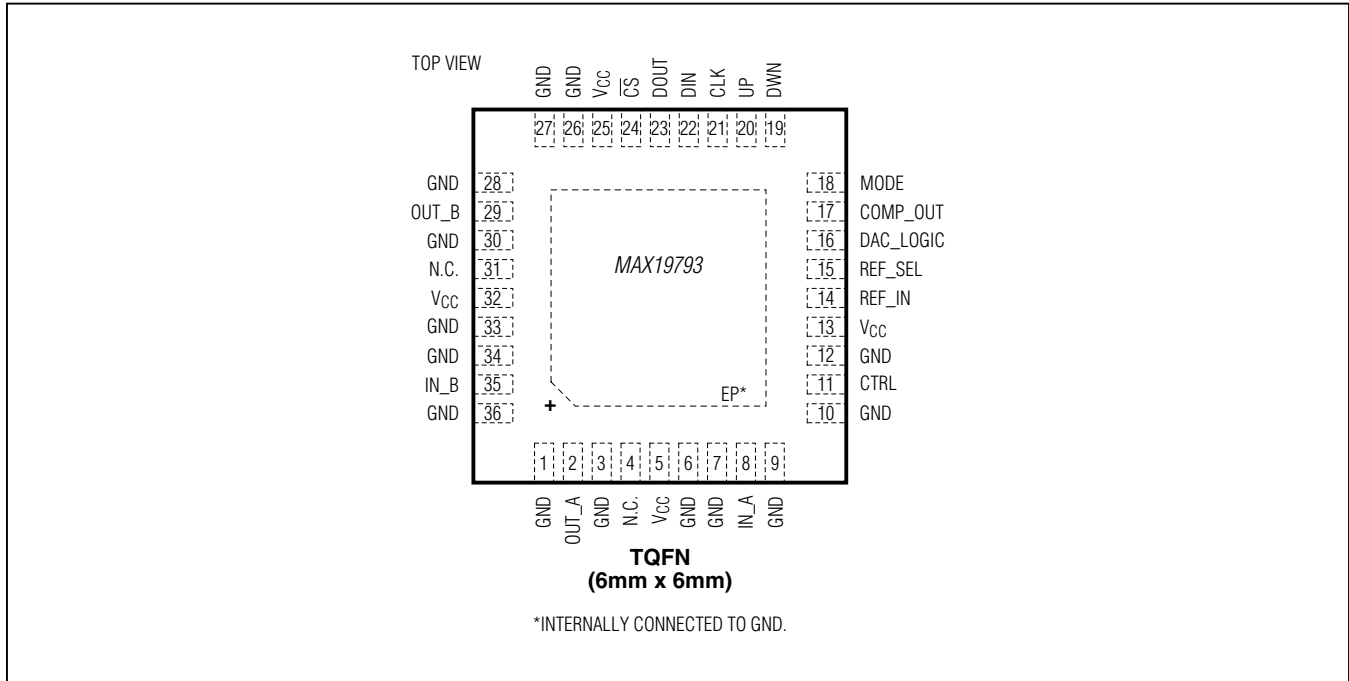
(Typical Application Circuit, $V_{CC} = 3.3V$, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω , $V_{DAC_LOGIC} = 0V$, $RDBK_EN = \text{logic } 0$, $V_{CTRL} = 1V$, $P_{IN} = 0\text{dBm}$, $f_{RF} = 3500\text{MHz}$, $T_C = +25^\circ\text{C}$, unless otherwise noted.)



MAX19793

1500MHz to 6000MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Pin Configuration



Pin Description

| PIN | NAME | DESCRIPTION |
|---|-----------------|--|
| 1, 3, 6, 7, 9, 10, 12, 26, 27, 28, 30, 33, 34, 36 | GND | Ground. Connect to the board's ground plane using low-inductance layout techniques. |
| 2 | OUT_A | Attenuator A RF Output. Internally matched to 50Ω over the operating frequency band. This pin, if used, requires a DC block. If this attenuator is not used, the pin can be left unconnected. |
| 4, 31 | N.C. | No Internal Connection. This pin can be left open or ground. Note: If a common layout is desired to support the MAX19794, connect a 0402 capacitor to ground on each of these pins. |
| 5 | V _{CC} | Attenuator A Power Supply. Bypass to GND with a capacitor and resistor, as shown in the <i>Typical Application Circuit</i> . |
| 8 | IN_A | Attenuator A RF Input. Internally matched to 50Ω over the operating frequency band. This pin, if used, requires a DC block. If this attenuator is not used, the pin can be left unconnected. |
| 11 | CTRL | Attenuator Control Voltage Input. Except in test mode, where no voltage can be applied to this pin. V _{CC} must be present unless using a current-limiting resistor as noted in the <i>Applications Information</i> section. |

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1500MHz to 6000MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Pin Description (continued)

| PIN | NAME | DESCRIPTION |
|-------|------------------------|--|
| 13 | V _{CC} | Analog Supply Voltage. Bypass to GND with a capacitor as close as possible to the device. See the <i>Typical Application Circuit</i> . |
| 14 | REF_IN | DAC Reference Voltage Input (Optional) |
| 15 | REF_SEL | DAC Reference Voltage Selection Logic Input. Logic = 0 to enable on-chip DAC reference. Logic = 1 to use off-chip DAC reference (pin 14). |
| 16 | DAC_LOGIC | DAC Logic Control Input (Table 1) |
| 17 | COMP_OUT | Comparator Logic Output. Use a 4.7pF capacitor to reduce any potential rise-time glitching when the comparator changes state. |
| 18 | MODE | Attenuator Control Mode Logic Input. Logic = 1 to enable attenuator step control. Logic = 0 to enable attenuator SPI control. |
| 19 | DWN | Down Pulse Input. Logic pulse = 0 for each step-down. |
| 20 | UP | Up Pulse Input. Logic pulse = 0 for each step-up. |
| 19/20 | DWN/UP | DWN/UP Pulse. Logic = 0 to both pins to reset the attenuator to a minimum attenuation state. |
| 21 | CLK | SPI Clock Input |
| 22 | DIN | SPI Data Input |
| 23 | DOUT | SPI Data Output |
| 24 | $\overline{\text{CS}}$ | SPI Chip-Select Input |
| 25 | V _{CC} | Digital Supply Voltage. Bypass to GND with a capacitor as close as possible to the device. See the <i>Typical Application Circuit</i> . |
| 29 | OUT_B | Attenuator B RF Output. Internally matched to 50 Ω over the operating frequency band. This pin, if used, requires a DC block. If this attenuator is not used, the pin can be left unconnected. |
| 32 | V _{CC} | Attenuator B Power Supply. Bypass to GND with a capacitor and resistor, as shown in the <i>Typical Application Circuit</i> . |
| 35 | IN_B | Attenuator B RF Input. Internally matched to 50 Ω over the operating frequency band. This pin, if used, requires a DC block. If this attenuator is not used, the pin can be left unconnected. |
| — | EP | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance. See the <i>Layout Considerations</i> section. |

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1500MHz to 6000MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Detailed Description

The MAX19793 is a dual general-purpose analog VVA designed to interface with 50 Ω systems operating in the 1500MHz to 6000MHz frequency range. Each attenuator provides 23.3dB of attenuation range with a linear control slope of 8.4dB/V. Both attenuators share a common analog control and can be cascaded together to yield 46.6dB of total dynamic range with a combined linear control slope of 16.8dB/V. Alternatively, the on-chip 4-wire SPI-controlled 10-bit DAC can be used to control both attenuators. In addition, a step-up/down feature allows user-programmable attenuator stepping through command pulses without reprogramming the SPI interface.

Applications Information

Attenuation Control and Features

The device has various states used to control the analog attenuator along with some monitoring conditions. The device can be controlled by an external control voltage, an internal SPI bus, or a combination of the two. The various states are described in Table 1. The SPI bus has multiple registers used to control the device when not configured for the analog-only mode. For cases where CTRL is used, the control range is 1V to 4V for $V_{CC} = 5V$, and is 1V to 2.5V for $V_{CC} = 3.3V$.

Up to 23.3dB of attenuation control range is provided per attenuator. At the insertion-loss setting, the single attenuator's loss is approximately 4dB. If a larger attenuation-control range is desired, the second on-chip attenuator can be connected in series to provide an additional 23.3dB of gain-control range.

Note that the on-chip control driver simultaneously adjusts both on-chip attenuators. It is suggested that a current-limiting resistor be included in series with CTRL to limit the input current to less than 40mA, should the control voltage be applied when V_{CC} is not present. A series resistor of greater than 200 Ω provides complete protection for 5V control voltage ranges.

Analog-Only Mode Control

In the Table 1 state (0, 0), the attenuators are controlled using a voltage applied to the CTRL pin of the device and the on-chip DAC is disabled. In cases where features of the SPI bus are not needed, the part can be operated in a pure analog control mode by grounding pins 14–25. This method allows the MAX19793 to be pin compatible with the MAX19790.

DAC Mode Control

In the Table 1 state (1, 0), the attenuators are controlled by the on-chip 10-bit DAC register. See the *Register Mode Up/Down Operation* section. In this condition, no signal is applied to the CTRL pin and the load on the CTRL pin should be > 100k Ω . The DAC is set using the SPI-loaded code in the registers, along with the setting of the MODE pin.

Analog Mode Control with Alarm Monitoring

In the Table 1 state (0, 1), the attenuators are controlled using a voltage applied to the CTRL pin of the device. See the *Register Mode Up/Down Operation* section. In this condition, the DAC is enabled and a voltage is also applied to the CTRL pin. The on-chip switches are set to compare the DAC voltage to the CTRL voltage at the comparator input; the output of the comparator (COMP_OUT) trips from high to low when VCTRL exceeds the on-chip DAC voltage.

DAC Test Mode

In the Table 1 state (1, 1), the attenuators are controlled by the on-chip 10-bit DAC register. See the *Register Mode Up/Down Operation* section. In this condition, the DAC is enabled and the DAC voltage appears at the CTRL pin. In this condition, no signal can be applied to the CTRL pin and the load on the CTRL pin should be > 100k Ω . This mode is only used in production testing of the DAC voltage and is not recommended for customer use.

Register Mode Up/Down Operation

The device has four 13-bit registers that are used for the operation of the device. The first bit is the read/write bit, the following two are address bits, and the remaining 10 are the desired data bits. The read/write bit determines whether the register is being written to or read from. The next two address bits select the desired register to write or read from. These address bits can be seen in Table 2. Table 3 describes the contents of the four registers.

Figure 1 shows the configuration of the internal registers of the device and Figure 2 shows the timing of the SPI bus. Register 0 sets the DAC code to the desired value, register 1 selects the step-up code, and register 2 selects the step-down code.

The device also contains a mode control pin (Table 4), along with UP and DWN controls (Table 5). When MODE is 0, the contents of register 0 get loaded into the 10-bit DAC register and set the value of the on-chip DAC. In this condition, the UP and DWN control pins have no effect on

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1500MHz to 6000MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

the part. In MODE 1, the effective DAC code fed to the 10-bit DAC register is equal to:

$$m \times \text{Register 1} - n \times \text{Register 2}$$

where m and n are the number of UP and DWN control steps accumulated, respectively.

After powering up the device, UP and DWN should both be set to 0 to reset the m and n counters to 0. This results in a 10-bit all 0 code out of the mathematical block in Figure 1, and applied to the 10-bit DAC register that drives the DAC. To increase (decrease) the code using the UP (DWN) pin, the DWN (UP) pin must be high and the UP (DWN) pin should be pulsed low to high. The device is designed to produce no wraparounds when using UP and DWN stepping so that the DAC code maxes out at 1023 or goes no lower than 0. See Figure 3 for the UP and DWN control operation.

Switching back to MODE = 0 produces the same 10-bit DAC code as was previously loaded into register 0. Switching back to MODE = 1 results in the previous 10-bit DAC code from the register 1 and 2 combiner/multiplier block.

Register 3 is used to set the RDBK_EN register in the write mode and is used to read back the RDBK_EN register and COMP_OUT in the read mode.

SPI Interface

The device can be controlled with a 4-wire, SPI-compatible serial interface. Figure 2 shows a timing diagram for the interface. In the write mode, a 13-bit word is loaded into the device through the DIN pin, with $\overline{\text{CS}}$ set low. The first bit of the word in the write mode is 0, and the next two bits select the register to be written to (Table 2). The next 10 bits contain the data to be written to the selected register. After the 13 bits are shifted in, a low-to-high $\overline{\text{CS}}$ command is applied and this latches the 10 bits into the selected register. The entire write command is ignored if $\overline{\text{CS}}$ is pulsed low to high before the last data bit is successfully captured.

For the read cycle, the first bit clocked in is a 1 and this establishes that a register is to be read. The next two clocked bits form the address of the register to be read (Table 2). In this read mode, data starts to get clocked out of the DOUT pin after A0 is captured. The DOUT pin goes to a high-impedance state after the 10 bits are transmitted or if $\overline{\text{CS}}$ goes high at any point during the transmission.

Voltage Reference

The device has an on-chip voltage reference for the DAC and a provision to operate with an off-chip reference. Table 6 provides details in selecting the desired reference.

Table 1. Attenuator Control Logic States

| DAC_LOGIC | RDBK_EN (D9, REG 3) | INTERNAL SWITCH STATES | ATTENUATOR | 10-BIT DAC |
|-----------|---------------------|----------------------------------|--|--|
| 0 | 0 | S1 = closed S2, S3, S4 = open | Controlled by an external analog voltage on the CTRL pin. | Disabled |
| 1 | 0 | S1, S3, S4 = open S2 = closed | Controlled by an on-chip DAC; no voltage is applied to the CTRL pin. | Enabled |
| 0 | 1 | S1, S3, S4 = closed S2 = open | Controlled by an external analog voltage on the CTRL pin. CTRL is compared with the DAC output. The comparator drives the COMP_OUT pin. | Enabled (update DAC code to estimate voltage on the CTRL pin) |
| 1 | 1 | S1, S2 = closed S3, S4 = open | Controlled by an on-chip DAC. The DAC output is connected to the CTRL pin. This state can be used to test the DAC output. In this condition, no voltage can be applied to the CTRL pin and the load on this pin must be > 100kΩ. | Enabled |

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Table 2. Address Data Bits

| R/W | A1 | A0 | DESCRIPTION |
|-----|----|----|----------------------------------|
| 0 | 0 | 0 | Write to register 0 using DIN. |
| 0 | 0 | 1 | Write to register 1 using DIN. |
| 0 | 1 | 0 | Write to register 2 using DIN. |
| 0 | 1 | 1 | Write to register 3 using DIN. |
| 1 | 0 | 0 | Read from register 0 using DOUT. |
| 1 | 0 | 1 | Read from register 1 using DOUT. |
| 1 | 1 | 0 | Read from register 2 using DOUT. |
| 1 | 1 | 1 | Read from register 3 using DOUT. |

Table 3. Register Definitions

| D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| REGISTER 0 (Read/Write Bits, 10-Bit DAC Code) | | | | | | | | | |
| DAC MSB | — | — | — | — | — | — | — | — | DAC LSB |
| REGISTER 1 (Read/Write Bits, 10-Bit Step-Up Code) | | | | | | | | | |
| Step-up MSB | — | — | — | — | — | — | — | — | Step-up LSB |
| REGISTER 2 (Read/Write Bits, 10-Bit Step-Down Code) | | | | | | | | | |
| Step-down MSB | — | — | — | — | — | — | — | — | Step-down LSB |
| REGISTER 3 (Write Bits)* | | | | | | | | | |
| RDBK_EN | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 |
| REGISTER 3 (Read Bits)** | | | | | | | | | |
| RDBK_EN | COMP_OUT | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 | Not used set = 0 |

*RDBK_EN = Enable bit for the voltage comparator that drives the COMP_OUT pin.

**RDBK_EN = Enable bit for the voltage comparator that drives the COMP_OUT pin.

COMP_OUT = Read logic level of COMP_OUT pin.

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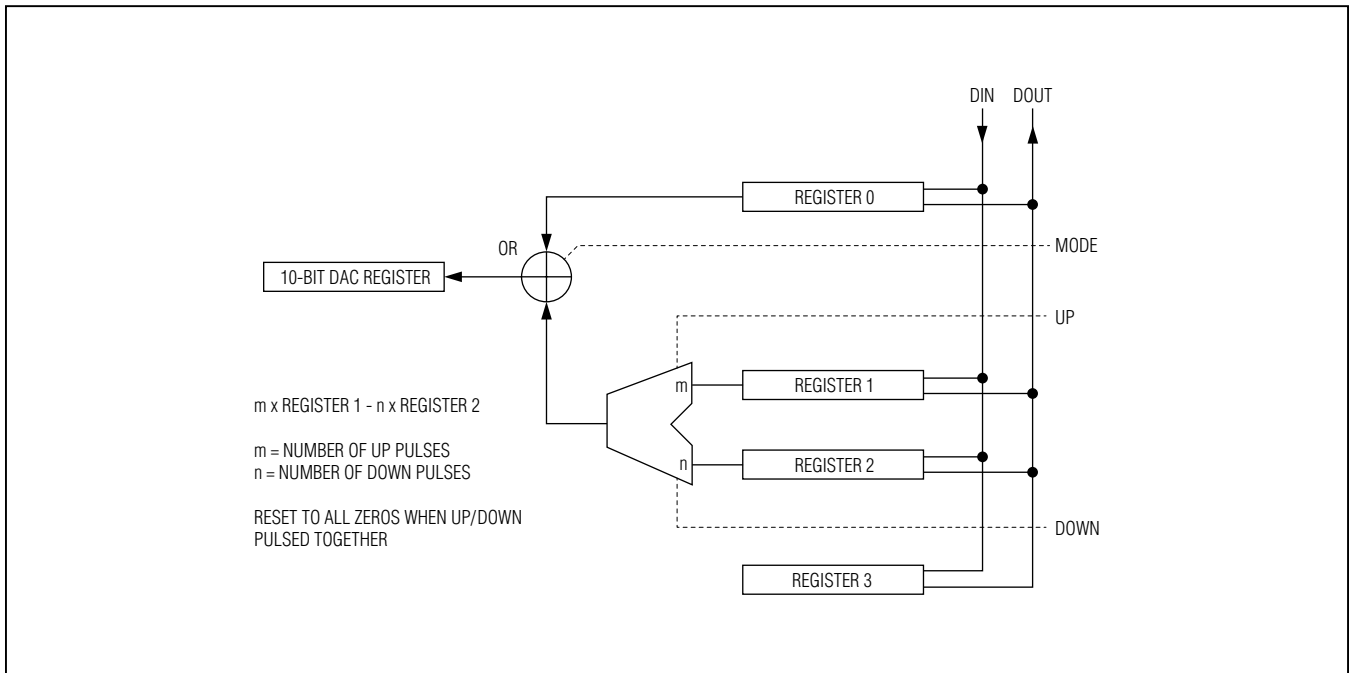


Figure 1. Register Configuration Diagram

Table 4. Attenuator-Mode Control Logic State

| MODE PIN | ATTENUATOR |
|----------|--|
| 0 | SPI-mode control (the DAC code is located in register 0). |
| 1 | Step-mode control using the UP and DWN pins (the step-up code is located in register 1 and the step-down code is located in register 2). |

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Table 5. Step-Mode Logic State (MODE = 1)

| UP | DWN | ATTENUATOR |
|---------------|---------------|--|
| Logic 0 | Logic 0 | Reset the DAC for the minimum attenuation state (DAC code = 0000000000). |
| Logic 0 pulse | Logic 1 | Increase the DAC code* by the amount located in register 1. UP is pulsed from high to low to high (see Figure 3). |
| Logic 1 | Logic 0 pulse | Decrease the DAC code* by the amount located in register 2. DWN is pulsed from high to low to high (see Figure 3). |

*Continued UP or DWN stepping results in saturation (no code wrapping).

Table 6. REF_SEL Logic State

| REF_SEL | DAC REFERENCE |
|---------|---|
| 0 | Uses an on-chip DAC reference. |
| 1 | User provides off-chip DAC reference voltage on REF_IN pin. |

SPI Interface Programming

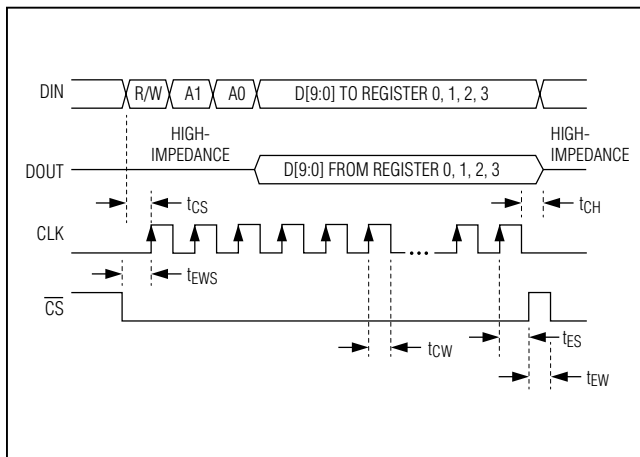


Figure 2. SPI Timing Diagram

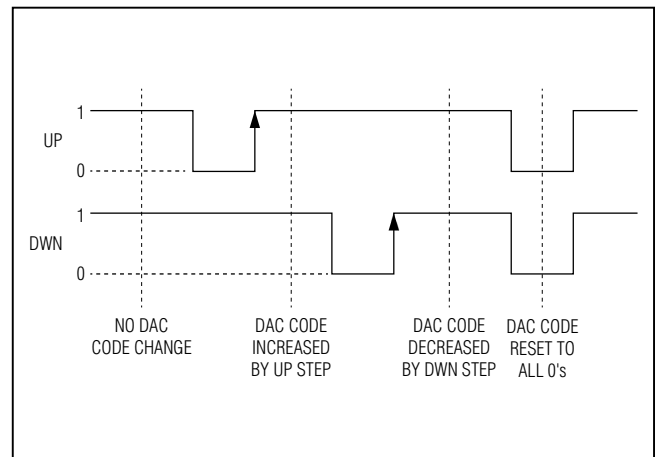


Figure 3. UP/DWN Control Diagram (MODE = 1)

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Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For best performance, route the ground-pin traces directly to the exposed pad underneath the package. This pad **MUST** be connected to the ground plane of the board by using multiple vias under the device to provide the best RF and thermal conduction path. Solder the exposed pad on the bottom of the device package to a PCB. Pins 4 and 31 for the MAX19793 have no internal connection. These two pins are in place to support the MAX19794 part in the family. The MAX19794 requires an additional bypass capacitor on each of these pins for proper operation. If desired to have a common layout to support the MAX19794, then include these capacitors in the common layout. Refer to the MAX19794 data sheet for details.

Power-Supply Bypassing

Proper voltage-supply bypassing is essential for high-frequency circuit stability. Bypass each VCC pin with capacitors placed as close as possible to the device. Place the smallest capacitor closest to the device. See the *Typical Application Circuit* and Table 7 for details.

Exposed Pad RF and Thermal Considerations

The exposed pad (EP) of the device's 36-pin TQFN package provides a low thermal-resistance path to the die. It is important that the PCB on which the IC is mounted be designed to conduct heat from this contact.

In addition, provide the EP with a low-inductance RF ground path for the device. The EP must be soldered to a ground plane on the PCB, either directly or through an array of plated via holes. Soldering the pad to ground is also critical for efficient heat transfer. Use a solid ground plane wherever possible.

Table 7. Typical Application Circuit Component Values

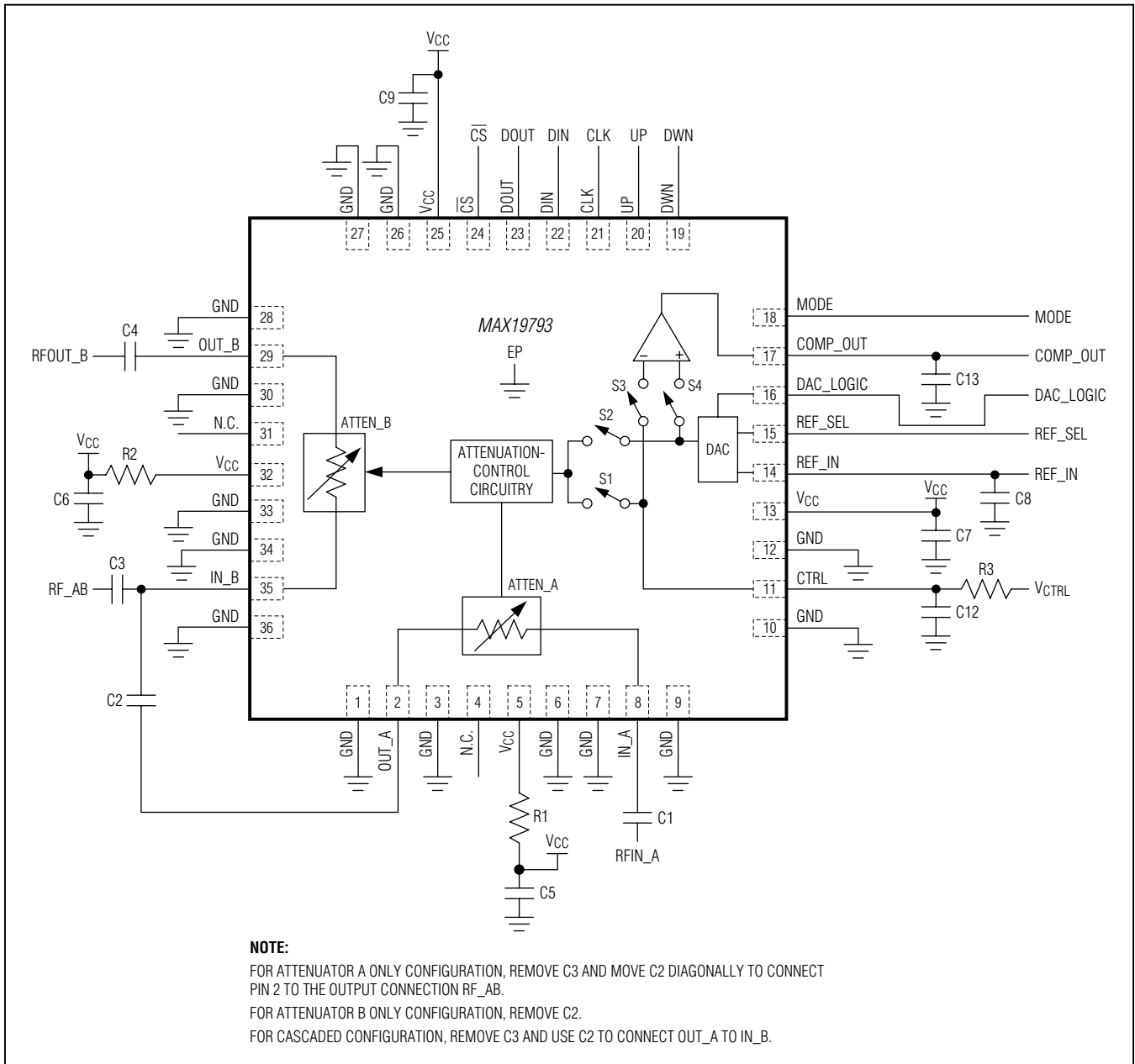
| DESIGNATION | QTY | DESCRIPTION |
|-------------|-----|---|
| C1, C2, C4 | 3 | 3.9pF \pm 0.25pF, 50V C0G ceramic capacitors (0402) |
| C3 | 1 | 3.9pF \pm 0.25pF, 50V C0G ceramic capacitor (0402) Not installed for two attenuators in cascade. |
| C5–C9 | 5 | 1000pF \pm 5%, 50V C0G ceramic capacitors (0402) |
| C12 | 1 | 120pF \pm 5%, 50V C0G ceramic capacitor (0402) Provides some external noise filtering along with R3. |
| C13 | 0 | Not installed, 4.7pF capacitor could be used to reduce any potential rise time glitching when the comparator changes state. |
| R1, R2 | 2 | 10 Ω \pm 5% resistors* (0402) |
| R3 | 1 | 200 Ω \pm 5% resistor (0402) Use this resistor to provide some lowpass noise filtering when used with C12. The value of R3 slows down the response time. R3 also provides protection for the device in case VCTRL is applied without VCC present. |
| U1 | 1 | Maxim MAX19793 |

*Add two additional 10 Ω series resistors between VCC's leading to C5 and C6, unless a VCC power plane is used.

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Typical Application Circuit



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1500MHz to 6000MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---------------|-----------------|-------------|
| MAX19793ETX+ | -40°C to +100°C | 36 TQFN-EP* |
| MAX19793ETX+T | -40°C to +100°C | 36 TQFN-EP* |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

T = Tape and reel.

Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 36 TQFN-EP | T3666+2 | 21-0141 | 90-0049 |

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Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 0 | 8/12 | Initial release | — |
| 1 | 5/15 | Removed military reference from data sheet | 1 |



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