PRODUCT INFORMATION LETTER

PIL IPD-PWR/13/8048
Dated 07 Aug 2013

Top metallization change from AlSiCu to AlCu on products using 4925 DMOS technology

Sales Type/product family label	See attached list
Type of change	Waferfab process change
Reason for change	Process rationalization
Description	The change from AlSiCu to AlCu top metallization has already been successfully implemented on several ST technologies. Usage of the same metal target on sputtering equipment will avoid changes of targets and consequently a longer equipment uptime and availability. The new metallization is in agreement with ST's standards and guarantees the same quality, reliability and electrical characteristics as the current one.
Forecasted date of implementation	01-Nov-2013
Forecasted date of samples for customer	31-Jul-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	31-Jul-2013
Involved ST facilities	Catania

DOCUMENT APPROVAL

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Reliability Evaluation Report

SD3931-10

Top metallization change from AlSiCu to AlCu on 4925 DMOS technology

General Information	
Product Line	*4925*
Product Description	*HF/VHF/UHF N-channel MOSFETs*
P/N	*SD3931-10*
Product Group	*IPD*
Product division	*POWER TRANSISTORS*
Package	*M174*
Silicon Process technology	*DISCRETE*

Locations	
Wafer fab	*CATANIA*
Assembly plant	*BOUSKOURA B/E*
Reliability Lab	*CTN Reliability Lab.*
Reliability assessment	*PASS.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	30-Jul-2013	8	A.Riciputo	G.Presti	

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
0061692	Reliability tests and criteria for qualifications

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

AlCu top metal extension to all high voltage technologies.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

175W – 100V HF/VHF DMOS transistor.

4.2 Construction note

	SD3931-10
Wafer/Die fab. information	
Wafer fab manufacturing location	CATANIA
Process family	DMOS
Die finishing back side	AuAs
Die size	6220x3420 micron
Bond pad metallization layers	AlCu
Wafer Testing (EWS) information	
Electrical testing manufacturing location	CATANIA
Assembly information	
Assembly site	BOUSKOURA B/E
Package description	M174
Die attach material	Au Eutectique
Wires bonding materials	Al-Si
Final testing information	
Testing location	BOUSKOURA B/E

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Lot	Data Code	Trace Code	Package	Product Line	Comments
1	553	1251	MAMI*20080YS	M174	4925	
2	556					
3	573	1321				

5.2 Test plan and results summary

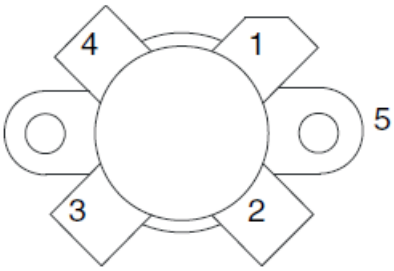
STAC150V2-350E

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die Oriented Tests									
HTFB	N	JESD22 A-108	Ta = 175°C, Vbias = +20V		168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
HTRB	N	JESD22 A-108	Ta = 175°C, Vbias = +200V		168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
HTSL	N	JESD22 A-103	Ta = 200°C		168 H	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
Package Oriented Tests									
TC	N	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77	0/77	
					200 cy	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	

6 ANNEXES

6.1 Device details

6.1.1 Pin connection

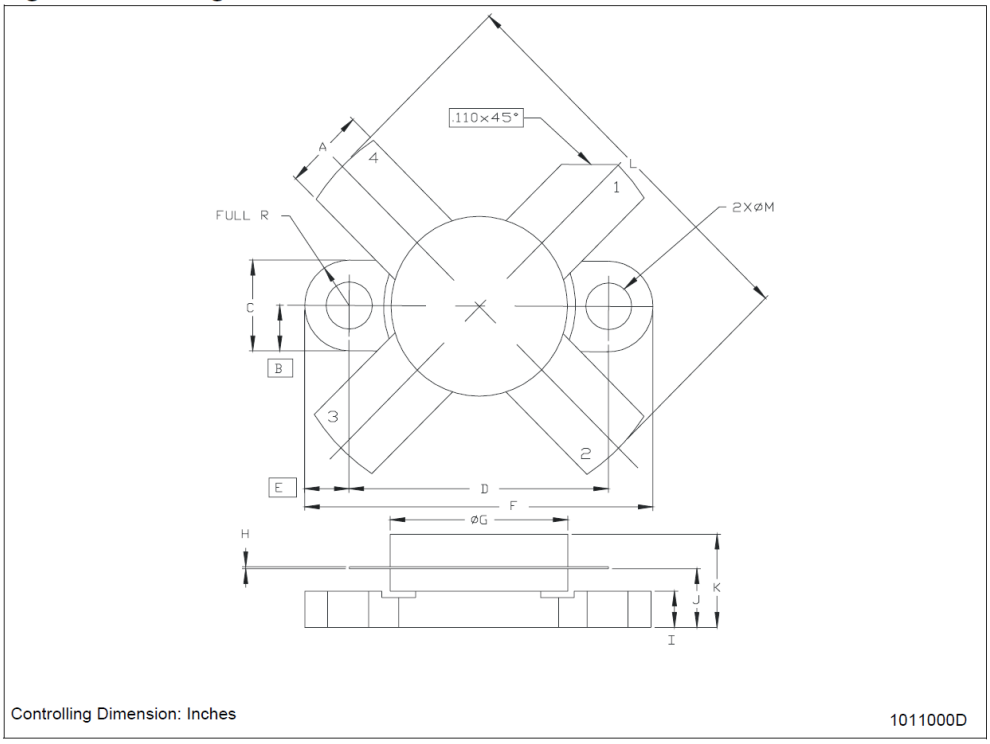


1. Drain
2. Source
3. Gate
4. Source
5. Source

6.1.2 Package outline/Mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.56		5.584	0.219		0.230
B		3.18			0.125	
C	6.22		6.48	0.245		0.255
D	18.28		18.54	0.720		0.730
E		3.18			0.125	
F	24.64		24.89	0.970		0.980
G	12.57		12.83	0.495		0.505
H	0.08		0.18	0.003		0.007
I	2.11		3.00	0.083		0.118
J	3.81		4.45	0.150		0.175
K			7.11			0.280
L	25.53		26.67	1.005		1.050
M	3.05		3.30	0.120		0.130

Figure 9. Package dimensions



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias **HTFB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

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