# NCP81148

*Advance Information*

# Synchronous Buck Controller with Auto Power Saving Mode and Built-In LDO

NCP81148 is a dual synchronous buck controller that is optimized for converting the battery voltage or adaptor voltage into multiple power rails required in desktop and notebook system. NCP81148 consists of two buck switching controllers with fixed 5.0 V output on channel 2, 3.3 V on channel 1 and two on−board LDOs with three outputs: 5 V / 60 mA and 3.3 V or 12 V / 10 mA. NCP81148 supports high efficiency, fast transient response and provides power good signals. ON Semiconductor proprietary adaptive−ripple control enables seamless transition from CCM to DCM, where converter runs at reduced switching frequency with much higher efficiency at light load. The part operates with supply voltage ranging from 5.5 V to 28 V. NCP81148 is available in a 28−pin QFN package.

### Features

- Wide Input Voltage Range: from 5.5 V to 28 V
- Built−in 5 V / 60 mA LDO
- Built−in selectable 3.3 V or 12 V / 10 mA LDO
- Three Selectable Fixed Frequency 300 KHz, 400 KHz or 600 KHz
- 180 Interleaved Operation Between the Two Channels in Continue−Conduction−Mode (CCM)
- Selected Power−Saving Mode/Forced PWM Mode
- Transient−Response−Enhancement (TRE) Control
- Input Supply Voltage Feed Forward Control
- Resistive or Lossless Inductor's DCR Current Sensing
- Over−Temperature Protection
- Internal Fixed 8.5 ms Soft−Start
- Fixed Output Voltages 5 V and 3.3 V
- Power Good Outputs for Both Channels
- Built−in Adaptive Gate Drivers
- Output Discharge Operation
- Built−in Over−Voltage, Under−Voltage Protection
- Accurate Over−Current Protection
- Thermal Shutdown

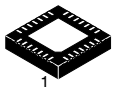
### Applications

- Desktop / Notebook Computers
- System Power Supplies
- I/O Power Supplies

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**ON Semiconductor®**

**http://onsemi.com**



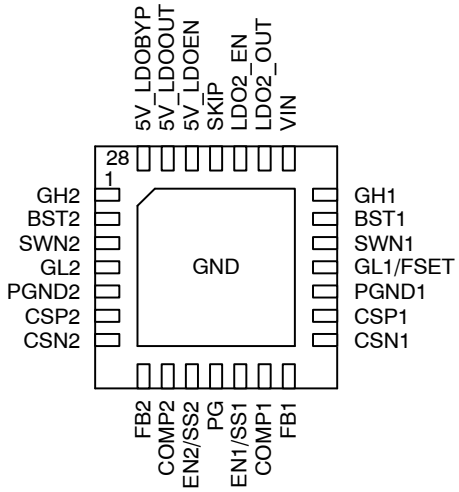
**28 PIN QFN, 4x4**
**MN SUFFIX**
**CASE 485AR**

**MARKING DIAGRAM**


81148 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**PIN CONNECTIONS**




(Top View)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCP81148MNTWG | QFN−28 (Pb−Free) | 4,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

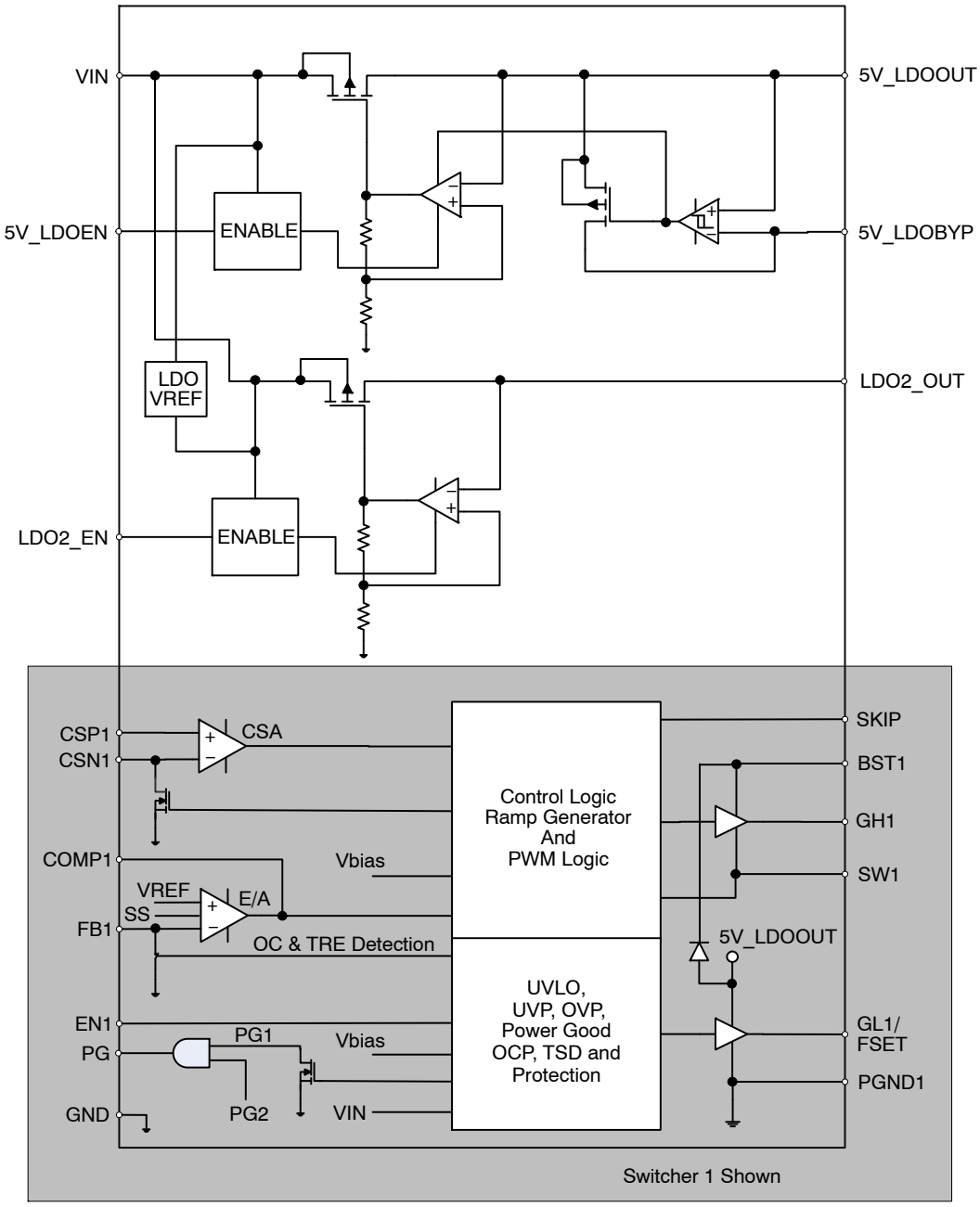



**Figure 1. Block Diagram**

**Table 1. PIN DESCRIPTIONS**

| Pin No. | Symbol | Description |
|---|---|---|
| 1, 21 | GH1, GH2 | Gate driver output of the top N−channel MOSFET. |
| 2, 20 | BST1, BST2 | Top gate driver input supply, a bootstrap capacitor connection between SWNx and this pin. |
| 3, 19 | SWN1, SWN2 | Switch node between the top MOSFET and bottom MOSFET. |
| 4 | GL2 | Gate driver output of bottom N−channel MOSFET in channel2. |
| 18 | GL1/FSET | Gate driver output of bottom N−channel MOSFET in channel1. And it is also used to set up switching frequency by connecting a resistor from this pin to ground. |
| 5, 17 | PGND1, PGND2 | Power ground for channel 1 & 2. |
| 6, 16 | CSP1, CSP2 | Inductor current differential sense non−inverting input. |
| 7, 15 | CSN1, CSN2 | Inductor current differential sense inverting input. |
| 8, 14 | FB1, FB2 | Output voltage feed back. |
| 9, 13 | COMP1, COMP2 | Output of the error amplifier. |
| 10, 12 | EN1, EN2 | Channel 1 and channel 2 enable pin. Short this pin to ground to disable the switcher channel. Pull this pin high to enable the switcher channel. |
| 11 | PG | Power good indicator for both output voltages. Open−drain output. |
| 22 | VIN | Battery or Adaptor input voltage |
| 23 | LDO2_OUT | Second internal LDO output. A capacitor of minimum 1.0 μF is recommended to connect between this pin and ground. |
| 24 | LDO2_EN | Enable for second internal LDO<br>− Tie to VCC to setup LDO2 output at 12 V<br>− Tie to 1/2VCC to setup LDO2 output at 3.3 V<br>− Tie to ground to disable LDO |
| 25 | SKIP | DCM programming pin:<br>− Ground this pin to setup automatic CCM−DCM transfer with 33 KHz minimum switching frequency limitation;<br>− Connect this pin to VCC to force CCM operation;<br>− Leave this pin open to give automatic CCM−DCM transfer with 33 KHz minimum switching frequency for channel 1 but forced CCM for channel 2. |
| 26 | 5V_LDOEN | Enable for internal 5 V LDO. |
| 27 | 5V_LDOOUT | The output for internal 5 V LDO. A capacitor of minimum 4.7 μF is recommended to connect between this pin and ground. |
| 28 | 5V_LDOBYP | 5 V LDO bypass pin. |
|  | E−Pad | GND. |

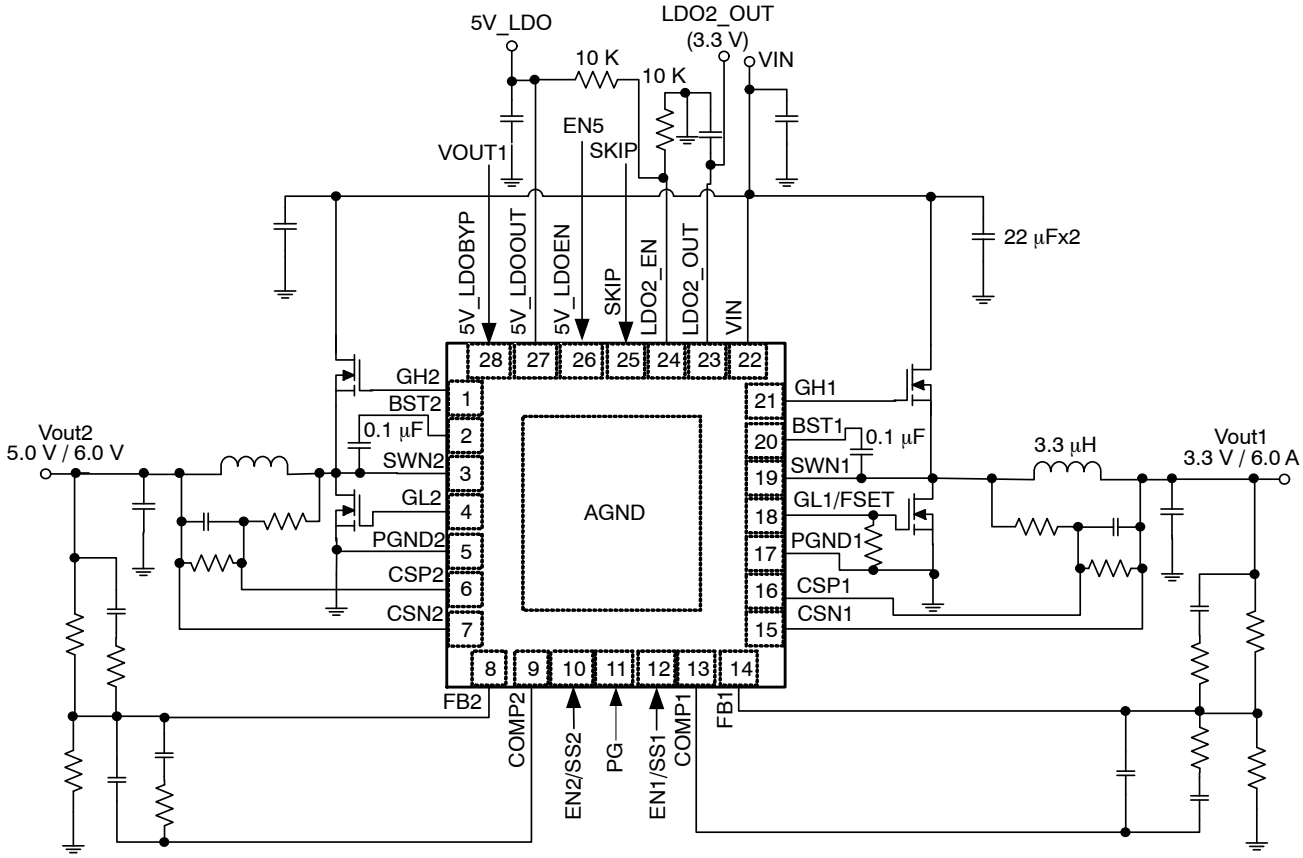



**Figure 2. Application Circuit**

**Table 2. ABSOLUTE MAXIMUM RATINGS** (Note 1)

| | |
|---|---|
| VIN to GND, 5V_LDOEN to GND | −0.3 V (DC) to 28 V −1.0 V for T < 100 n |
| SWN1, SWN2 to GND | −0.6 V to 28 V, −10.0 V for T < 20 ns |
| BST1, BST2 to GND | −0.6 V to 34 V |
| GH1, GH2 to GND | −0.6 V to 34 V, −5.0 V for T < 100 ns |
| PGND1, PGND2 | −0.3 V to 0.3 V |
| All other pin | −0.3 V to 6.0 V, −1.0 V for T < 100 ns |
| Operating Temperature Range, $T_A$ | −40°C to +125°C |
| Junction Temperature, $T_J$ | −40°C to +150°C |
| Storage Temperature Range, $T_S$ | −55°C to +150°C |
| Pkg Power Dissipation (TA = +25°C), $P_D$ (Note 2) | 2.45 W max |
| | $R_{\theta JA}$ = 51°C/W |
| | $R_{\theta J-Lead}$ = 26°C/W |
| | $R_{\theta J-BoardTop}$ = 3.2°C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Operation at −40°C to 0°C guaranteed by design, not production tested.
2. These data are based on JEDEC JESD51.7 highly conductive PCB multiple layer PCB (2 power and/or 2 ground planes 76 mm x 76 mm 1 oz each) connected by 20 thermal vias. 100 sq mm Cu heat spreader, 2 oz.

**Table 3. ELECTRICAL CHARACTERISTICS**
(VIN = 12 V, Vout = 5.0 V, TA = +25°C for typical value; −40°C < TA < 125°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Input Supply Voltage | VIN | | 5.5 | | 28 | V |
| **INTERNAL LDO OUTPUT** | | | | | | |
| 5V_LDOOUT Voltage | | VIN =12 V, $I_{5V\_LDOOUT}$ = 60 mA | 4.85 | 5.0 | 5.15 | V |
| 5V_LDOOUT Current | | VIN =12 V, EN1 = EN2 = 0 | | 100 | | mA |
| 5V_LDO Switch to Bypass Threshold | | | 4.7 | | 4.95 | V |
| 5V_LDOOUT to 5V_IDOBYP Impedance | | LDOBYP = 5 V | | 1.0 | | Ω |
| Hysteresis | | | 100 | 200 | | mV |
| LDO2_OUT Voltage | | LDO2_EN = VCC, VIN = 15 V, Load Current = 10 mA | 11.4 | 12 | 12.6 | V |
| | | LDO2_EN = 1/2 VCC, VIN = 15 V, Load Current = 10 mA | 3.2 | 3.3 | 3.46 | V |
| LDO2_OUT Current | | | 10 | 15 | | mA |
| **SUPPLY CURRENT** | | | | | | |
| BSTx Quiescent Current | $I_{BST}$ | $V_{FB}$ = 1.5 V, EN = 5.0 (No Switching), GH and GL are open | | | 0.3 | mA |
| BSTx Shutdown Supply Current | $I_{BST\_SD}$ | EN = 0, BST = 5 V, SWN = 0 | | | 6.0 | μA |
| Vin Pin Supply Current | | Iload = 0 | | 2.0 | | mA |
| Shutdown Current | $I_{VIN\_SD}$ | EN1, EN2, LDOEN, LDO2_EN = 0 | | 5.0 | | μA |
| | | EN1, EN2, LDOEN = 5 V, LDO2_EN = 5 V | | 1.15 | | mA |
| | | EN1, EN2 = 0, LDOEN = 5 V, LDO2_EN = 2.5 V | | 1.57 | | mA |
| | | EN1, EN2 = 0, LDOEN = 5 V, LDO2_EN = 0 | | 1.11 | | mA |
| **OSCILLATOR** | | | | | | |
| Oscillator Frequency | Fsw | Rset = 1.8 k | 270 | 300 | 330 | KHz |
| | | Rset = 9.1 k | 340 | 400 | 460 | KHz |
| | | Rset = 16 k | 540 | 600 | 660 | KHz |
| Oscillator Frequency Accuracy | | | | | ±10 | % |
| **ERROR AMPLIFIER** | | | | | | |
| Open Loop DC Gain (Note 3) | | | 80 | | | dB |
| Open Loop Unity Gain Bandwidth (Note 3) | $F_{0dB,EA}$ | | 10 | 15 | | MHz |
| Open Loop Phase Margin (Note 3) | | | 60 | | | deg |
| Input Bias Current (Note 3) | | | −200 | | 200 | nA |
| Input Offset Voltage (Note 3) | | V+ = V− = 0.8 V | −1.0 | | 1.0 | mV |
| Slew Rate | | COMP pin to GND = 10 pF | | 2.5 | | V/μs |
| Maximum Output Voltage | | 10 mV of overdrive, $I_{SOURCE}$ = 2.0 mA | 3.3 | | | V |
| Minimum Output Voltage | | 10 mV of overdrive, $I_{SINK}$ = 2.0 mA | | | 0.3 | V |
| Output Source Current | | 10 mV of overdrive, $V_{out}$ = 3.5 V | 2.0 | | | mA |
| Output Sink Current | | 10 mV of overdrive, $V_{out}$ = 1.0 V | 2.0 | | | mA |

3. Guaranteed by Design
4. Parameters are for design only, not for product test.

**Table 3. ELECTRICAL CHARACTERISTICS**
(VIN = 12 V, Vout = 5.0 V, TA = +25°C for typical value; −40°C < TA < 125°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **FEEDBACK VOLTAGE** | | | | | | |
| Reference Voltage | $V_{REF}$ | | 792 | 800 | 808 | mV |
| Feedback Voltage Line Regulation | | 5V_LDOOUT = 4.5 V ~ 5.5 V | | | 0.25 | %/V |
| **DIFFERENTIAL CURRENT SENSE AMPLIFIER** | | | | | | |
| CSP and CSN Common−mode Input Voltage Range | | Refer to AGND | −0.2 | | 5.5 | V |
| Current Sense Input to Output Gain | | (CSP)−(CSN) = 10 mV | | 200 | | μA/V |
| Differential Input Voltage Range | | | −60 | | 60 | mV |
| **OVER CURRENT PROTECTION** | | | | | | |
| OCP Threshold Voltage | | V(CSP)−V(CSN) @ 25°C | 35 | 40 | 45 | mV |
| | | V(CSP)−V(CSN) @ 0 ~ 85°C | 34 | | 46 | mV |
| OCP Trigger Clock Tick | | After EN, latch off after trigger # clocks | | 16 | | |
| Short Circuit OCP Threshold Voltage | | | | 60 | | mV |
| **GATE DRIVER** | | | | | | |
| GH Pull−High Resistance | RH_GH | Source, V(BST−GH) = 0.1 | | 2.5 | | Ω |
| GH Pull−Low Resistance | RL_GH | Sink, V(GH−SWN) = 0.1 V | | 1.5 | | Ω |
| GL Pull−High Resistance | RH_GL | Source, V(VCC−GL) = 0.1 V | | 2.0 | | Ω |
| GL Pull−Low Resistance | RL_GL | Sink, V(GL−PGND) = 0.1 V | | 1.0 | | Ω |
| Dead Time | | GL off to GH on | 10 | 20 | 30 | ns |
| | | GH off to GL on | 10 | 20 | 30 | ns |
| **VOLTAGE MONITOR** | | | | | | |
| VCC Start Threshold | | | 3.7 | 4.2 | 4.4 | V |
| VCC UVLO Hysteresis | | | 100 | 200 | 300 | mV |
| Power Good Threshold | | PG in from lower | 91.5 | 95 | 97.5 | % |
| | | PG hysteresis | | 5.0 | | % |
| Power Good High Delay | | After soft start is done | | 500 | | μs |
| Power Good Low Delay | | | | 1.5 | | μs |
| Power Good Sink Current | | PG = 0.4 V | 2.5 | 5.0 | | mA |
| Output Overvoltage Rising Threshold | | After VCC POR, with respect to VFB | 106 | 110 | 118 | %Vref |
| Overvoltage Fault Blanking Time | | | | 1.5 | | μs |
| Output Under-Voltage Trip Threshold | | After soft start, with respect to VFB | 45 | 50 | 55 | %Vref |
| Under-voltage Protection Blanking Time | | | | $t_{ss}$ | | ms |
| Under−voltage Protection Delay | | | | 2.0 | | ms |
| **PWM** | | | | | | |
| Minimum Controllable ON Time | | | | 50 | | ns |
| Minimum OFF Time | | | | 100 | 150 | ns |
| PWM Ramp Offset | | | 0.36 | 0.4 | 0.44 | V |
| PWM Ramp Amplitude | | VIN = 5 V | | 1.25 | | V |
| | | VIN = 12 V | | 3.0 | | V |
| PWM Comparator Propagation Delay | | 10 mV to 20 mV overdrive | | 25 | 30 | ns |

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**Table 3. ELECTRICAL CHARACTERISTICS**
(VIN = 12 V, Vout = 5.0 V, TA = +25°C for typical value; −40°C < TA < 125°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **INTERNAL BST DIODE** | | | | | | |
| Forward Voltage Drop | | IF = 10 mA, TA = 25°C | | 0.3 | | V |
| Reverse−bias Leakage Current | | VBST = 34 V, VSW = 28 V, TA = 25°C | | 0.1 | 6.0 | μA |
| **SOFT−STOP** | | | | | | |
| Output Discharge On−Resistance | | EN = 0, Vout = 0.5 V | | 20 | 30 | Ω |
| Discharge Threshold in Vcc | | | | 0.7 | | V |
| **SOFT−START** | | | | | | |
| Soft−Start Ramp Time | tss | From EN assertion to Vout ready | 6.0 | 12 | 18 | ms |
| **EN** | | | | | | |
| EN1/EN2 Threshold | | HI Threshold | 1.4 | | | V |
| | | LO Threshold | | | 0.4 | V |
| | | Hysteresis | | 200 | | mV |
| | | Source Current, pull high to 5 V internally | | 0.75 | | μA |
| 5V_LDOEN Threshold | | HI Threshold | 1.4 | | | V |
| | | LO Threshold | | | 0.4 | V |
| | | Hysteresis | | 200 | | mV |
| LDO2_EN | | Vout = 3.3 V | 1.5 | 2.5 | 3.5 | V |
| | | Vout = 12 V | 4.95 | | 5.5 | V |
| | | Vout = 0 | | | 0.4 | V |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown Threshold (Note 3) | | | | 150 | | °C |
| Thermal Shutdown Hysteresis (Note 3) | | | | 40 | | °C |

3. Guaranteed by Design
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## DETAILED DESCRIPTION

### Overview

The NCP81148 is a cost effective dual output controllers with three selectable LDO outputs suitable for desktop and server application. It provides one independent LDO which is 5 V/100 mA, two selectable LDOs which is 12 V or 3.3 V/10 mA, and two synchronous PWM controllers that incorporate all the control and protection circuitry necessary to satisfy a wide range of applications. The NCP81148 PWM switchers employ adaptive−ripple control to provide seamless transition between CCM and DCM while maintain high efficiency during light load. It also provides fast transient response and excellent stability. The features of the NCP81148 include a precision reference, selectable switching frequency, an error amplifier, adaptive gate driver, programmable soft−start, and very low shutdown current. The protection features of the NCP81148 include fixed/programmable soft−start, over−current protection, wide input voltage range, power good monitor, over voltage and under voltage protection, built in output discharge and thermal shutdown.

### 5V LDO and Switchover (5V_LDOOUT)

The NCP81148 includes a high−current (100 mA) linear regulator that is configured for 5 V operation, which is bias supply necessary to power up the main analog supply rail for the IC and provides the current for the gate drivers. When the 3.3 V switching regulator is running and the 5 V switching regulator is still off (EN2 = 0), the 5 V linear regulator can provide about 80 mA to external load, while the remaining 20 mA is consumed by the 3.3 V regulator's MOSFETS' switching, giving typical switching frequency and MOSFETS' gate capaciatance. Once the 5 V switching regulator is enabled, this 5V_LDO may be bypassed using 5V_LDOBYP input. Typically, a capacitor with 10−μF or higher is needed to keep 5V_LDO stable. Additionally, if VOUT2 voltage exceeds 4.75 V, the 5V_LDO is switched off and VOUT2 (5V buck output) is connected to 5V_LDOOUT through a bypass FET (typical 1 ohm) to provide 5 V rail. With this bypass function, the whole system efficiency is improving. The 5V_LDOEN pin is high voltage and can be connected to VIN voltage. However, 5V_LDOEN is not allowed to go beyond VIN pin voltage.

### LDO2_OUT

The NCP81148 includes 10 mA linear regulators that can be programmed for 12 V or 3.3 V operations. LDO2 can be enabled only when VCC is present. When LDO2_EN is connected to VCC, LDO2_OUT is programmed at 12 V. When LDO2_EN is connected to 1/2VCC, LDO2_OUT is set at 3.3 V. Typically, a minimum capacitor with 1.0−μF or higher is needed to keep LDO2_OUT stable.

### Reference Voltage

The NCP81148 incorporates an internal reference that allows output voltages as low as 0.8 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents.

### Oscillator Frequency

A fixed precision oscillator is provided. The actual switching frequency is set at 300 KHz, 400 KHz or 600 KHz by the resistor on GL1/FSET pin. The resistor and frequency can be referred to the table below.

| FSET resistor | 1.8 K | 9.1 K | 16 K |
|---|---|---|---|
| Switching Frequency | 300 KHz | 400 KHz | 600 KHz |

### Error Amplifier

The error amplifier's primary function is to regulate the converter's output voltage using a resistor divider connected from the converter's output to the FB pin of the controller, as shown in the Applications Schematic. A type III compensation network must be connected around the error amplifier to stabilize the converter. It has a bandwidth of greater than 15 MHz, with open loop gain of at least 80 dB. The COMP output voltage is clamped to a level above the oscillator ramp in order to improve large−scale transient response.

### Soft−Start

To limit the start−up inrush current, an internal soft start circuit is used to ramp up the reference voltage from 0 V to its final value linearly. The internal soft start time is 13 ms typically, from EN assertion to Vout ready. It includes a delay of 240 μs from EN assertion to the Vout ramp starting. 500 μs after both channel Vout ready, the PG (Power Good) is asserted.

### Soft−Stop

Soft−Stop or discharge mode is always on during faults or disable. In this mode, a fault (UVP, OCP, TSD) or disable (EN) causes the output to be discharged through an internal 20−ohm transistor inside of VO terminal. The time constant of soft−stop is a function of output capacitance and the resistance of the discharge transistor.

### Adaptive Non−Overlap Gate Driver

In a synchronous buck converter, a certain dead time is required between the low side drive signal and high side drive signal to avoid shoot through. During the dead time, the body diode of the low side FET free-wheels the current. The body diode has much higher voltage drop than that of the MOSFET, which reduces the efficiency significantly. The longer the body diode conducts, the lower the efficiency. NCP81148 implements adaptive dead time control to minimize the dead time, as well as preventing shoot through from happening.

#### Forced Pulse Width Modulation (FPWM Mode)

The device is operating as force PWM mode if SKIP is tied to VCC. Under this mode, the low−side gate driver signal is forced to be the complement of the high−side gate driver signal. This mode allows reverse inductor current, in such a way that it provides more accurate voltage regulation and better (fast) transient response. During the soft start operation, the NCP81148 automatically runs as FPWM mode regardless of the SKIP setting at either FPWM or SKIP mode to make sure to have smooth power up.

#### Power Save Mode (Skip Mode)

If the load current decreases, the converter will enter power save mode operation when SKIP pin is grounded. During power save mode, the converter skips switching and operates with reduced frequency but with minimum switching frequency of 33 KHz, which minimizes the quiescent current and maintains high efficiency. If SKIP pin is open, the channel 1 will enter power saving mode with reduced load but with minimum switching frequency of 33 KHz and channel 2 will stay in forced PWM mode.

#### Transient Response Enhancement (TRE)

For a conventional trailing−edge PWM controller in CCM, the minimum response delay time is one switching period in the worst case. To further improve transient response, a transient response enhancement circuitry is introduced to the NCP81148. The controller continuously monitors the COMP signal, which is the output voltage of the error amplifier, to detect load transient events. A desired stable close−loop system with the NCP81148 has a ripple voltage in the COMP signal, which peak−to−peak value is normally in a range from 200 mV to 500 mV. There is a threshold voltage made in a way that a filtered COMP signal pluses an offset voltage. Once a large load transient occurs, the COMP signal is possible to exceed the threshold and then TRE is tripped in a short period, which is typically around one normal switching cycle. In this short period, the controller runs at higher frequency and therefore has faster response. After that the controller comes back to normal operation.

## PROTECTIONS

#### Under Voltage Lockout (UVLO)

There are two undervoltage lock out protections (UVLO) in NCP81148. One is for $V_{IN}$, which has a typical trip threshold voltage 3.9 V and trip hysteresis 200 mV. The other is for VCC (5V_LDOOUT serves as VCC internally), which has a typical trip threshold voltage 4.2 V and trip hysteresis 300 mV. If either is triggered, the device resets and waits for the voltage to rise up over the threshold voltage and restart the part. Please note this protection function DOES NOT trigger the fault counter to latch off the part.

#### Over Voltage Protection (OVP)

When VFB voltage is above 110% (typical) of the nominal VFB voltage, the top gate drive is turned off and the bottom gate drive is turned on trying to discharge the output. It over voltage condition still exists after 1.5 μs, an OV fault is set. The power good will go low at the same time. The bottom gate drive will be turned off when VFB drops below the under voltage threshold. If then over voltage condition happens again, the high side MOSFET stays off and low side MOSFET will turn on again till output voltage drops down to under voltage threshold. Then low side gate will be off. EN resets or power recycle the device can exit the fault.

#### Under Voltage Protection (UVP)

An UVP circuit monitors the VFB voltage to detect under voltage event. The under voltage limit is 50% (typical) of the nominal VFB voltage. If the VFB voltage is below this threshold over 1 ms, an UV fault is set and the device is latched off such that both top and bottom gate drives are off. EN resets or power recycle the device can exit the fault. UVP is delayed for soft start period (8.5 ms) after EN goes high.

#### EN1 and EN2

EN1 and EN2 are logic level control signals to turn on or off buck converters individually. If ENx is below 0.4 V, the buck will be off. When ENx is above 1.8 V, the buck is turning on. In both ENx pins, there are about 0.75 μA source currents to pull them up to 5 V internally.

#### Power Good Monitor (PG)

NCP81148 provides window comparator to monitor the output voltage. When the output voltage is above 95% of regulation voltage, the power good pin outputs a high signal. Otherwise, PG stays low. The PG pin is open drain 5−mA pull down output. During startup, PG stays low until the feedback voltage is within the specified range for 128 clocks or about 0.5 ms. If feedback voltage falls outside the tolerance band, the PG pin goes low within microseconds.

#### Over Current Protection (OCP)

The NCP81148 protects converter if over−current occurs. The current through each channel is continuously monitored with differential current sense. Current limit threshold Vth_OC between CS+ and CS− is internally fixed to 40 mV. The current limit can be programmed by inductor's DCR and current sensing resistor divider with Rs1 and Rs2.

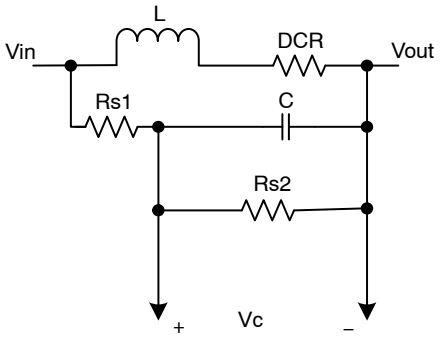



**Figure 3. X**

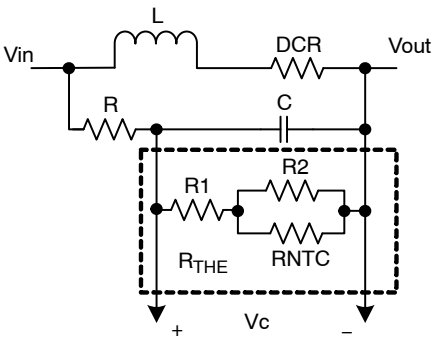



**Figure 4. X + 1**

The Rs1, Rs2 and C can be calculated as:

$$C \cdot \left(R_{S1} // R_{S2}\right) = \frac{L}{DCR}$$

The inductor peak current limit is:

$$I_{LIM(Peak)} = \frac{V_{th\_DC}}{k \cdot DCR}, \text{where } k = \frac{R_{S2}}{R_{S1} + R_{S2}}$$

The DC current limit is:

$$I_{LIM} = I_{LIM(Peak)} - \frac{V_O \cdot (V_{in} - V_O)}{2 \cdot V_{in} \cdot f_{SW} \cdot L}$$

where Vin is the input supply voltage of the power stage, and fsw is normal switching frequency.

Fig. X+1 shows NTC resistor network to compensate the temperature drift of DCR.

If inductor current exceeds the current threshold, the high−side gate driver will be turned off cycle−by−cycle. In the mean time, an internal OC fault timer will be triggered. If the fault still exists after 16 clocks, the part latches off, both the high−side MOSFET and the low−side MOSFET are turned off. If the sensed current reaches 60 mV, the part will latch off right away. The fault remains set until the system has shutdown and re−applied VCC and/or the enable signal EN is toggled.

### Pre−Bias Startup

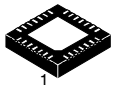
In some applications the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. NCP81148 supports pre−bias start up by holding Low side FETs off till soft start ramp reaches the FB pin voltage.

### Thermal Shutdown

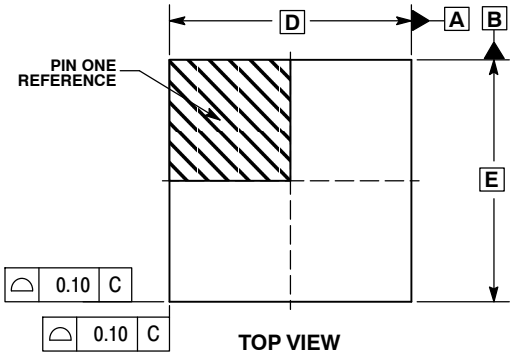
The NCP81148 protects itself from over heating with an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold the voltage at the COMP pin will be pulled to GND and both the upper and lower MOSFETs will be shut OFF.

**QFN28 4x4, 0.4P**
CASE 485AR−01
ISSUE A

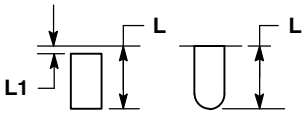
DATE 20 NOV 2009



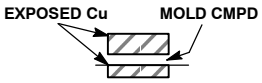
**SCALE 2:1**



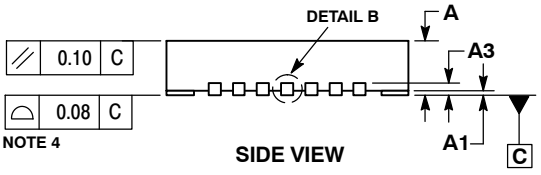

**TOP VIEW**



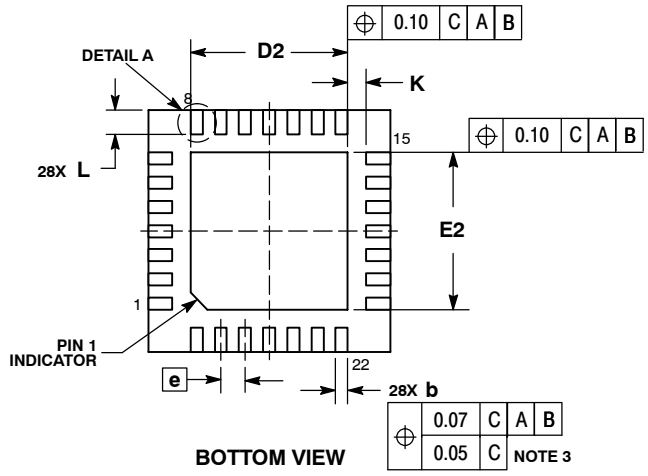

**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**




**DETAIL B**
**ALTERNATE CONSTRUCTION**




**SIDE VIEW**

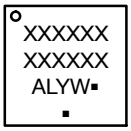



**BOTTOM VIEW**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.15 | 0.25 |
| D | 4.00 BSC | |
| D2 | 2.50 | 2.70 |
| E | 4.00 BSC | |
| E2 | 2.50 | 2.70 |
| e | 0.40 BSC | |
| K | 0.30 REF | |
| L | 0.30 | 0.50 |
| L1 | −−− | 0.15 |

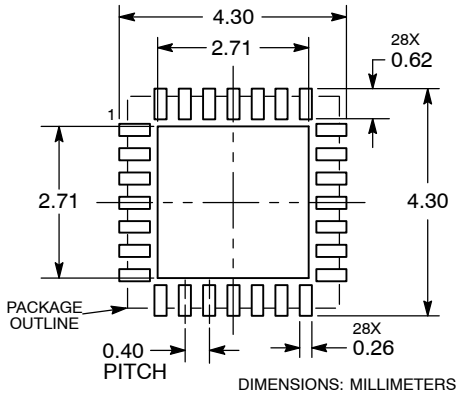
**GENERIC MARKING DIAGRAM***




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

**RECOMMENDED MOUNTING FOOTPRINT**




DIMENSIONS: MILLIMETERS

| ISSUE | REVISION | DATE |
|---|---|---|
| O | RELEASED FOR PRODUCTION. REQ. BY M. LIN. | 15 MAY 2008 |
| A | CHANGED DIMENSIONS D2, E2, K, L, MOUNTING FOOTPRINT AND MARKING DIAGRAM INFORMATION. REQ. BY J. LIU. | 20 NOV 2009 |
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