

Migrating from the Teridian 73S8024RN to the 73S8009R

Introduction

This application note highlights the main differences between a Teridian 73S8009R and industry-standard 8024 ICs (including the Teridian 73S8024RN). The note describes the main system-level aspects a designer should be aware of to migrate from an 8024-based design to the higher-performance, lower-cost 73S8009R.

For STBs and DTVs that currently use the Teridian 73S8024RN or any other 8024-like device for a Conditional Access or a payment interface slot, the Teridian 73S8009R is an attractive alternate solution with real technical advantages and eventually a lower cost.

The 73S8009R is a “transparent” smart card interface which means the IC provides an image of each smart card signal through dedicated digital I/Os to the host processor, whereas the 73S8024RN adds card clock dividing circuits, card activation sequencing and a crystal oscillator circuit that are not implemented in the 73S8009R. While this provides more flexibility to the 73S8009R, certain hardware and firmware changes may be necessary in order to accommodate 8024 designs for the more simplistic 73S8009R IC. This application note assumes the host processor is typically an A/V decoder processor that already handles the smart card protocol layer to communicate with smart cards.

Why Consider a 73S8009R Instead of a 73S8024RN?

1. **1.8 V smart card support:** 8024-like ICs support only 5 V and 3 V smart cards. More recent, lower-power and higher-performance smart cards require a 1.8 V supply. The 73S8009R will make an STB or a DTV ready to support such Conditional Access or for-payment smart cards (since the *EMV 4.1 Specification* now includes 1.8 V requirement for payment cards).
2. **Power Down mode:** While the boxes are getting smaller and smaller, power dissipation is becoming a growing concern. Furthermore, Energy Star and Code of Conduite (CoC) requirements are pushing designers to significantly reduce the power consumption. The 73S8009R features a Power Down mode that lowers the power consumption to less than 1 μ A, which compares to several mA for 8024 type of ICs (that have no Power Down mode), hence an **improvement factor of about 1,000**.
3. **Cost competitive:** The 73S8009R is the simplest ISO 7816-3 electrical interface IC that can be thought of: Digital circuitry that appears to be unnecessary in typical STB implementations has been removed, to reduce the die size to its minimum. As a result, a reduction on price can be expected when migrating from 8024-like ICs to the 73S8009R.
4. **Compatibility with all key standards:** ISO 7816-3, EMV4.1, NDS and Nagravision are fully supported by the 73S8009R, which makes this IC the most versatile of the market.

Why Consider a 73S8009R Instead of a TDA8024 / ST8024?

1. All the above benefits of the 73S8009R are valid against traditional TDA8024 devices, making the 73S8009R a more universal, cost competitive IC, better tailored to meet new low power requirements.
2. The 73S8009R IC generates the smart card voltage (VCC) through a low-drop-out regulator (LDO) that offers dramatic improvements in terms of signal integrity and analog performance compared to the low performance charge-pump capacitor based converter of the TDA8024 or ST8024 ICs. Refer to the Appendix for further details about 73S8009R versus TDA8024 type of devices.

Functional Differences (73S8009R versus 8024 ICs)

1. **Clock source:** The 8024 devices incorporate an oscillator, with a configurable divider (i.e. the frequency of the card clock output is selectable: $F_{CLK} = F_{XTALIN} / 1; /2; /4 \text{ or } /8$). Practically, in most of the STB designs, the oscillator is not used as such, and a system clock is directly fed into the XTALIN input pin of the 73S8024RN, while the division rate /1 is most often used. In such a case, the migration to the 73S8009R is very straight forward, and the pin CLKIN replaces the pin XTALIN of the S8024 devices.

Note that the clock signal to CLKIN must have a duty cycle better than 48% to 52% to ensure a CLK signal duty cycle of 45 to 55%.

2. **Card activation and deactivation state machine:** Unlike the S8024 devices, the 73S8009R does not implement the smart card activation / deactivation sequencing, as per ISO 7816-3, EMV or NDS specifications. This actually provides more flexibility to the designer since the activation / deactivation timings can be mastered and adjusted. As a result, the state machine must be implemented in the host firmware when using a 73S8009R instead of an 8024 device. A sample flowchart for this state machine is provided in Figure 9.

Note that in case of hardware fault (card extraction, card overcurrent, power supply drop), the 73S8009R will automatically deactivate the smart card following ISO7816 recommendation. In normal situations, the host processor is responsible for card deactivation, and therefore it must implement the card deactivation sequence.

3. **New features – two more digital I/Os are required:** The 73S8009R offers extended features – 1.8 V card support and Power Down. Two additional digital outputs are needed from the host processor in order to support these features. Should the designer not need them, the two extra outputs would not be needed. Note: the 3V/5V pin on the 8024 devices is no longer necessary and can be reassigned for one of these new digital outputs.
4. **The 73S8009R incorporates a chip select (CS) pin:** This pin allows multiple 73S8009R devices to be cascaded. The CS pin must be set high for the control pins to operate properly.

Power Supply Requirements

Operating Voltage Range

Table 1 lists the operating supply voltages.

Table 1: Operating Supply Voltages

	Power Supply Requirement (voltage range)		
	73S8024RN	73S8009R	TDA8024 / ST8024
Analog Power Supply	VPC Pin 6 (SO28) Pin 3 (QFN32) Pin 2 (QFN20) Voltage range: 4.75 V~6.0 V	VPC Pin 15 (SO28) Pin 9 (QFN20) Voltage range: 4.75 V~6.0 V	VDDP Pin 6 (SO28) Voltage range:TDA8024 3.0 V ~ 6.5 V (ICC < 20 mA) 4.0 V ~ 6.5 V (ICC > 20 mA) Voltage range: ST8024 4.75 V ~ 6.5 V
Digital Power Supply	VDD Pin 21 (SO28) Pin 20 (QFN32) Pin 12 (QFN20) Voltage range: 2.7 V ~5.5 V	VDD Pin 28 (SO28) Pin 17 (QFN20) Voltage range: 2.7 V ~3.6 V	VDD Pin 21 (SO28) Voltage range: 2.7 V ~ 6.5 V

Power Consumption

Table 2 shows actual power measurements of the TDA8024T, 73S8024RN and 73S8009R devices. The measurements were made on the VDD and VPC(VDDP) supplies for each device with the following conditions; VCC = 5 V with 10 mA load, VCC = 5 V with 65 mA load, VCC = 0 V (off) and power down.

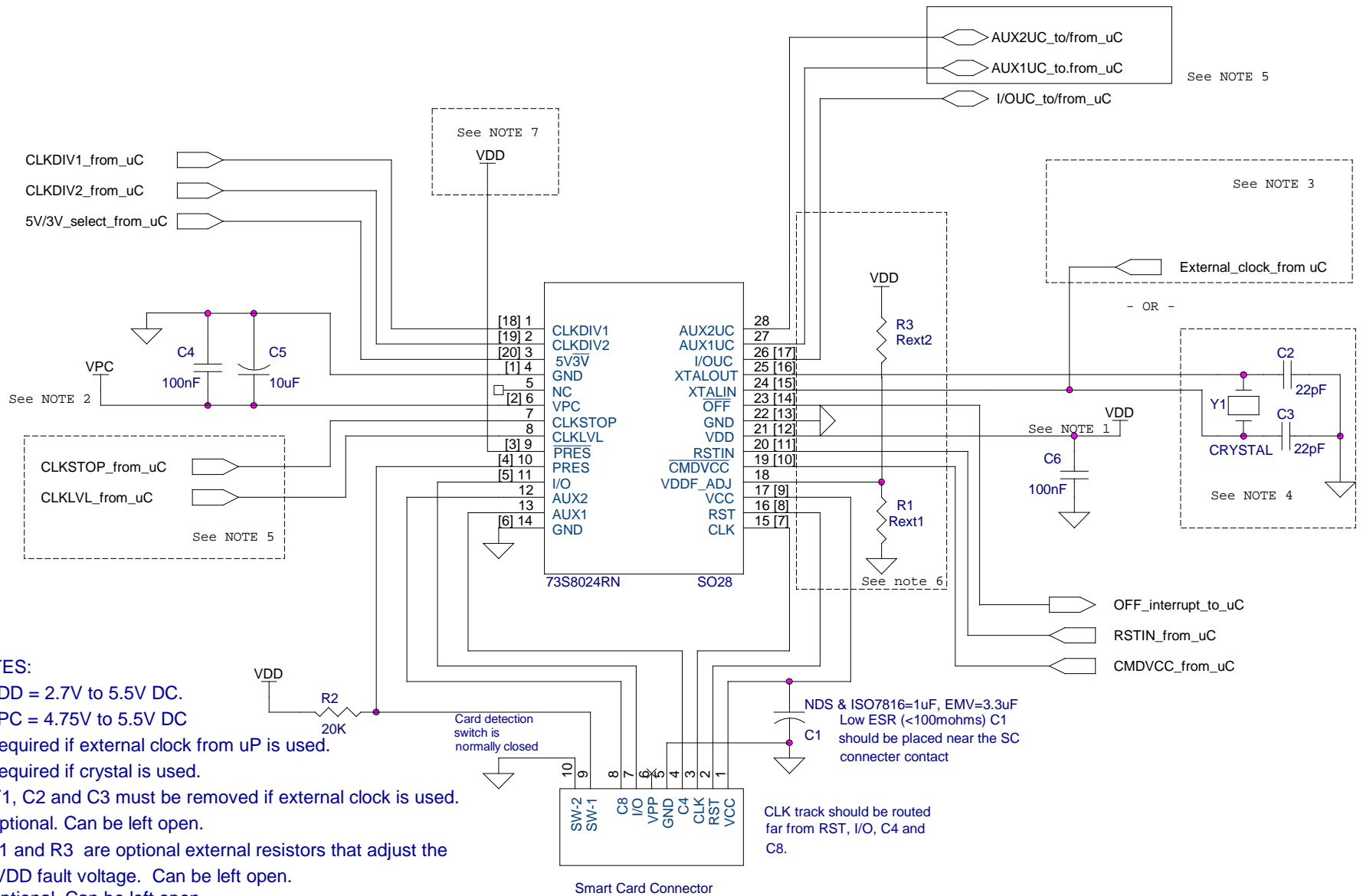
Table 2: Operating Supply Current Measurements

Condition	73S8009R		73S8024RN		TDA8024	
	IDD	IPC	IDD	IPC	IDD	IDDP
5 V @ 10 mA	673 μ A	10.35 mA	1.13 mA	10.5 mA	770 μ A	21.61 mA
5 V @ 65 mA	673 μ A	65.4 mA	1.13 mA	66 mA	790 μ A	145.7 mA
Lowest power consumption mode (Smart card deactivated, device powered)	0.2 μ A (Power Down)	0.1 μ A (Power Down)	1.12 mA	350 μ A	570 μ A	0.2 μ A

Practical Implementation: Hardware Aspects

Typical Electrical Schematics

Figure 1 shows a schematic for a typical electrical implementation for the Teridian 73S8024RN (SO28). Figure 2 shows a typical electrical implementation for the 73S8009R. For each 73S80xx IC, the default pin numbers correspond to the SO28 packages, whereas the pin numbers in parenthesis correspond to the QFN20 packages.



NOTES:

- 1) VDD = 2.7V to 5.5V DC.
- 2) VPC = 4.75V to 5.5V DC
- 3) Required if external clock from uP is used.
- 4) Required if crystal is used.
Y1, C2 and C3 must be removed if external clock is used.
- 5) Optional. Can be left open.
- 6) R1 and R3 are optional external resistors that adjust the VDD fault voltage. Can be left open.
- 7) Optional. Can be left open.

Figure 1: Conditional or Payment Smart Card Implementation – 73S8024RN

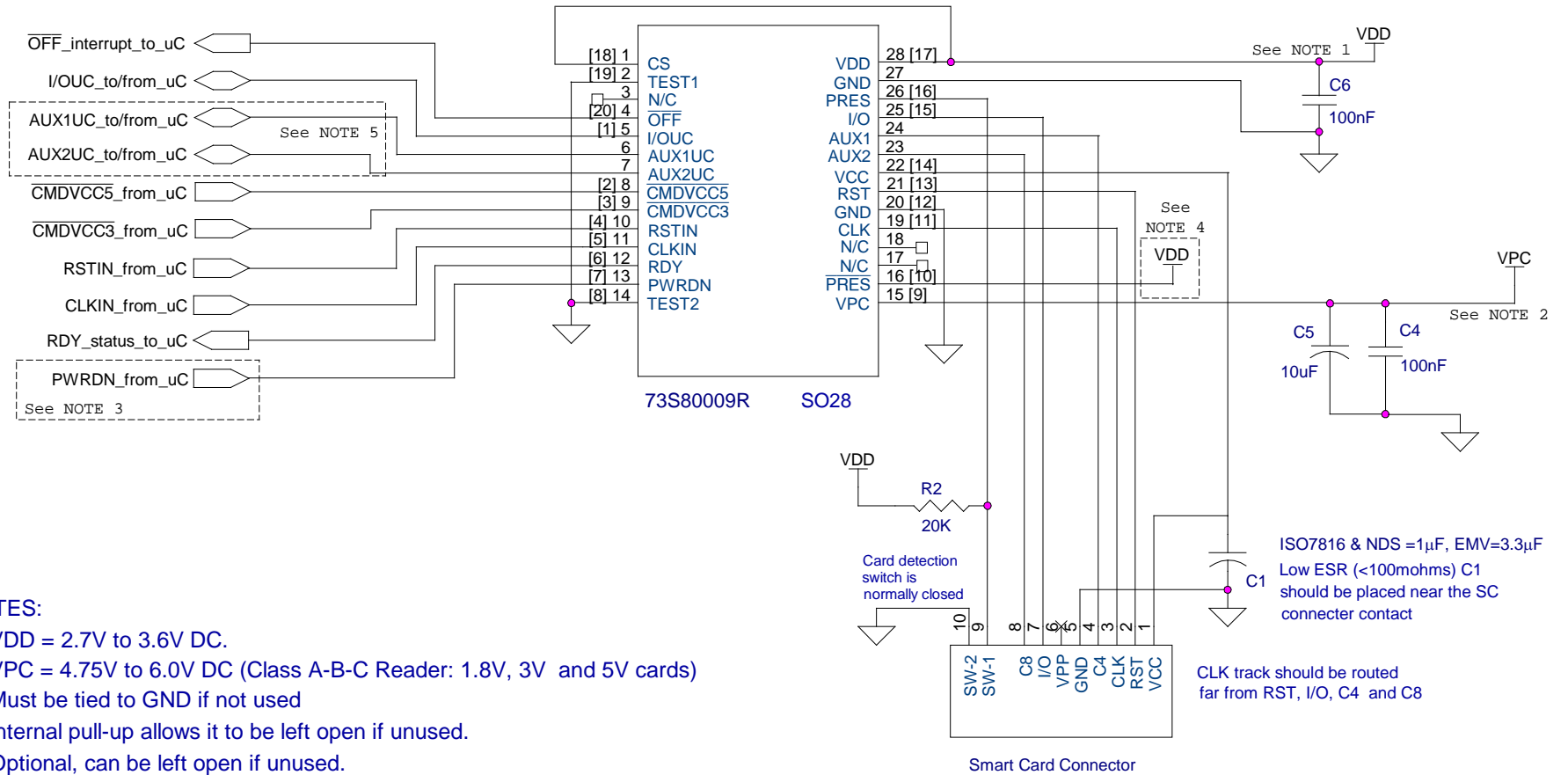


Figure 2: Conditional or Payment Smart Card Implementation – 73S8009R

Pin Description and Comparison (TDA8024/ST8024 – 73S8024 – 73S8009R)

The differences between the 73S8009R and the 8024 type of ICs result in a different pinout. While 73S8024RN, TDA8024 and ST8024 ICs are pin compatible (SO28), the 73S8009R, because of its slightly different architecture, and its added features, is a not a drop-in replacement IC.

Table 3 lists all the pins of each IC and highlights the differences.

Table 3: 8024 and 73S8009R Pinout Comparison

8024-ICs			73S8009R		Comment
8024 Pin Number (SO28)	TDA8024T Pin Name	73S8024RN Pin Name	8009R Pin Number (SO28 [QFN20])	73S8009R Pin Name	
1	CLKDIV1	CLKDIV1	–	N/A	There is no clock divider in the 73S8009R. The frequency of the signal fed into the pin CLKIN (73S8009R) must be the card clock frequency. Same situation as when using an 8024-IC with division rate = /1.
2	CLKDIV2	CLKDIV2	–	N/A	
3	5V/3V	5V/3V	9 [3]	CMDVCC3	See Table 5 description.
4	PGND	GND	–	N/A	Ground connections.
5	S2	NC	–	N/A	TDA8024' / ST8024' charge pump capacitor connected between S1 and S2 are not needed when using Teridian 73S8009R (or 73S8024RN) ICs – Can be removed for cost saving.
6	VDDP	VPC	15 [9]	VPC	+5.0 V standard power supply pin.
7	S1	CLKSTP	–	N/A	Same as pin number 5.
8	VUP	CLKLVL	–	N/A	Teridian 73S80xxR ICs have no DC-DC converter, this pin is used to implement a card clock stop mode in 73S8024RN – No corresponding function in 73S8009R. The decoupling capacitor required by the TDA8024 / ST8024 can be removed in Teridian-based designs (cost savings).
9	PRES	PRES	16 [10]	PRES	Card presence switch input – similar function.
10	PRES	PRES	26[16]	PRES	
11	I/O	I/O	25 [15]	I/O	Smart card pins – similar functions (AUX signals only available on 28 SO pkg).
12	AUX2	AUX2	23	AUX2	
13	AUX1	AUX1	24	AUX1	
14	CGND	GND	20 [12]	GND	
15	CLK	CLK	19 [11]	CLK	
16	RST	RST	21 [13]	RST	
17	VCC	VCC	22 [14]	VCC	
18	PORADJ	VDDF_ADJ	–	N/A	System power supply – voltage monitoring function only available in 8024 ICs, including Teridian 73S8024RN. Feature not supported by the 73S8009R.
19	CMDVCC	CMDVCC	8 [2]	CMDVCC5	See Table 5 description.

8024-ICs			73S8009R		Comment
8024 Pin Number (SO28)	TDA8024T Pin Name	73S8024RN Pin Name	8009R Pin Number (SO28 [QFN20])	73S8009R Pin Name	
20	RSTIN	RSTIN	10 [4]	RSTIN	No differences.
21	VDD	VDD	28 [17]	VDD	Digital power supply (also defines digital, interfacing level with the host) – Similar function between all ICs.
22	GND	GND	27	GND	Ground connections.
23	$\overline{\text{OFF}}$	$\overline{\text{OFF}}$	4 [20]	$\overline{\text{OFF}}$	Interrupt output – open drain – to report card insertion status and other hardware faults to the host processor. Similar function between all ICs.
24	XTAL1	XTALIN	11 [5]	CLKIN	Similar function between all 8024 ICs, including 73S8024RN. However, the 73S8009R has no oscillator, and a clock source must be provided from the host to the pin CLKIN (card clock frequency).
25	XTAL2	XTALOUT	–	N/A	
26	I/OUC	I/OUC	5 [1]	I/OUC	Host digital I/O pins (main + auxiliary) – half duplex lines, images of the smart card I/O and C4 / C8 I/O lines. Similar function between all ICs. (AUX signals only available on the 28 SO package.)
27	AUX1UC	AUX1UC	6	AUX1UC	
28	AUX2UC	AUX2UC	7	AUX2UC	
–	N/A	N/A	1 [18]	$\overline{\text{CS}}$	Chip Select signals enables cascading of multiple 73S8009R devices. Control signals disabled when CS is low.
–	N/A	N/A	2 [19]	TEST1	Device test pins. Tie to ground.
–	N/A	N/A	14 [8]	TEST2	Device test pins. Tie to ground.
–	N/A	N/A	12 [6]	$\overline{\text{RDY}}$	Ready output signals host when VCC is stable. Not necessary for normal operation if a short delay is used. Any failure will cause $\overline{\text{OFF}}$ to go low.
–	N/A	N/A	13 [7]	$\overline{\text{PWRDN}}$	Power Down input pin. Setting high when VCC is off will place the device in a low power mode where current draw is less than 1 μA .

Dual Implementation 8024-like and 73S8009R

Should the designer want to keep dual source between a 73S8024RN (or any other 8024 type of IC) and the 73S8009R IC, Teridian suggests implementing a PCB layout with a dual footprint PCB implementation, compatible with either a 73S8024RN / TDA8024 / ST8024 SO28 integrated circuit or a 73S8009R QFN20 package integrated circuit.

Electrical Schematic – Dual Footprint Implementation (8024 device and 73S8009R)

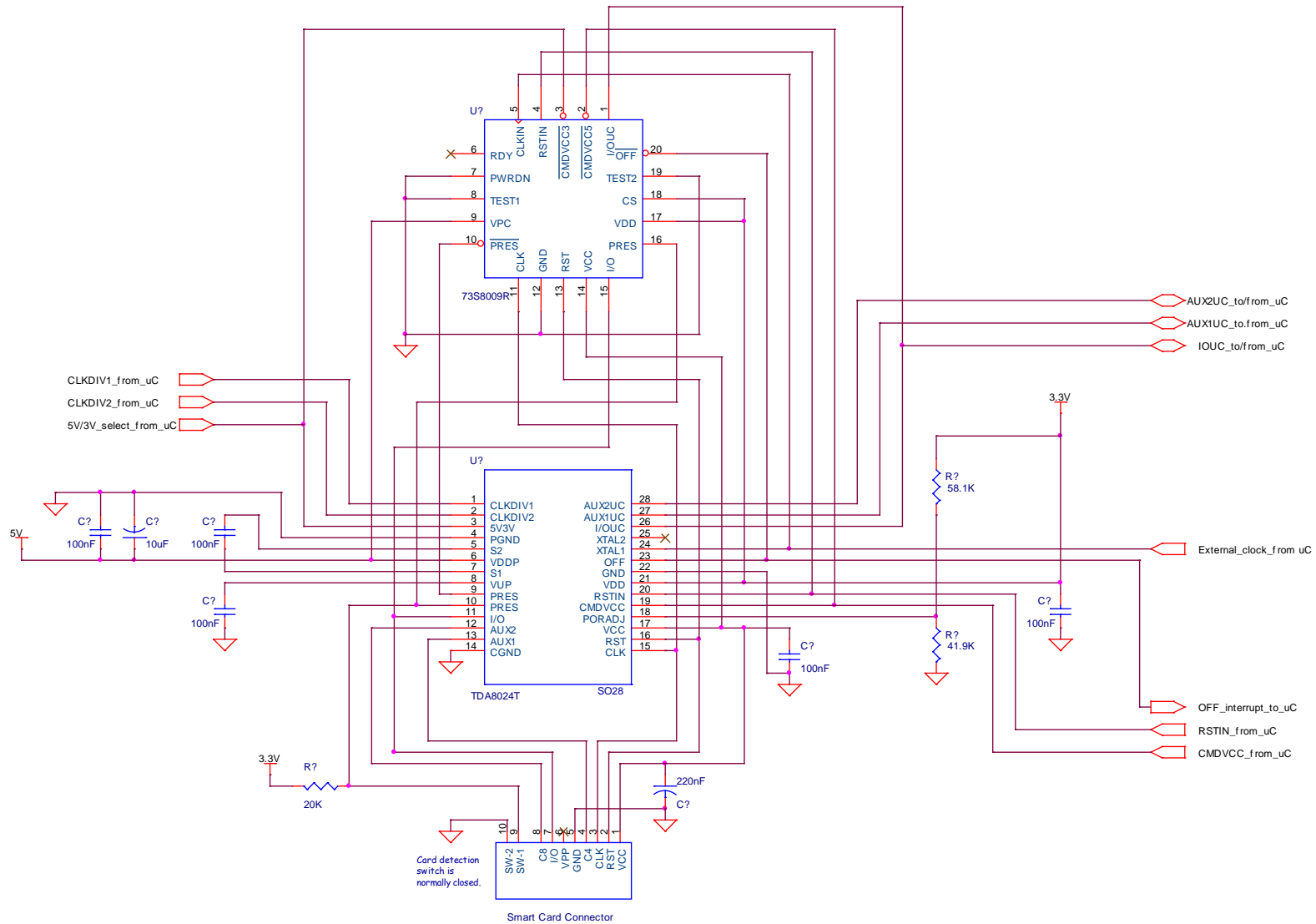


Figure 3: Dual-Footprint Implementation (8024 and 73S8009R)

IC Pinouts and PCB Layout

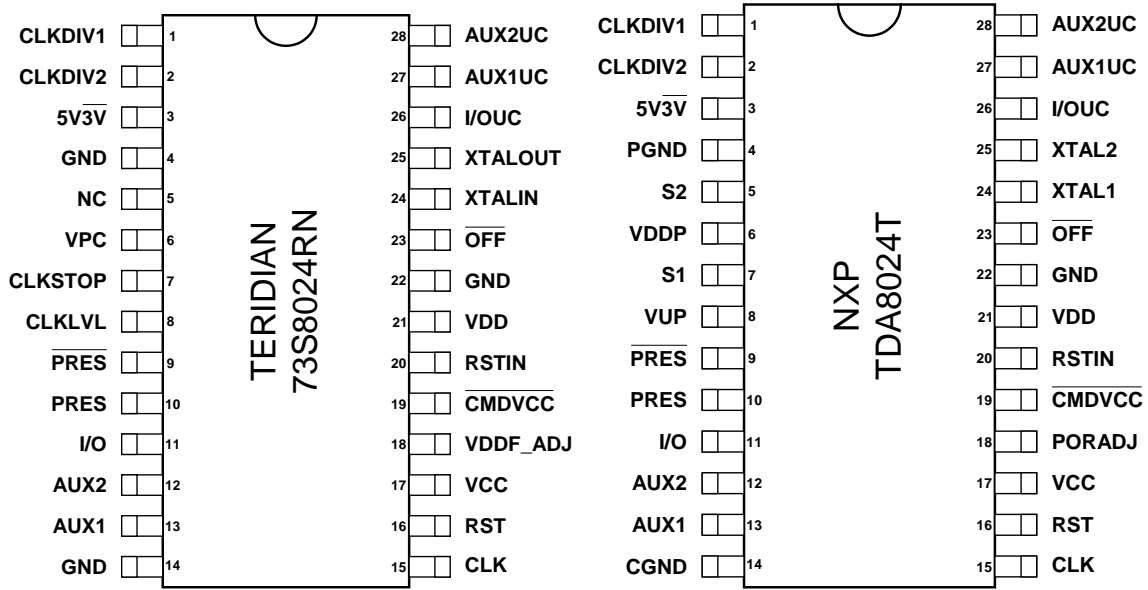


Figure 4: Teridian 73S8024RN and NXP TDA8024T Pinouts

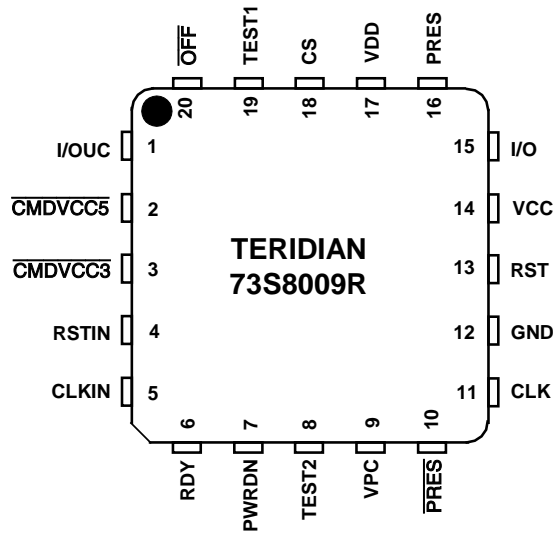
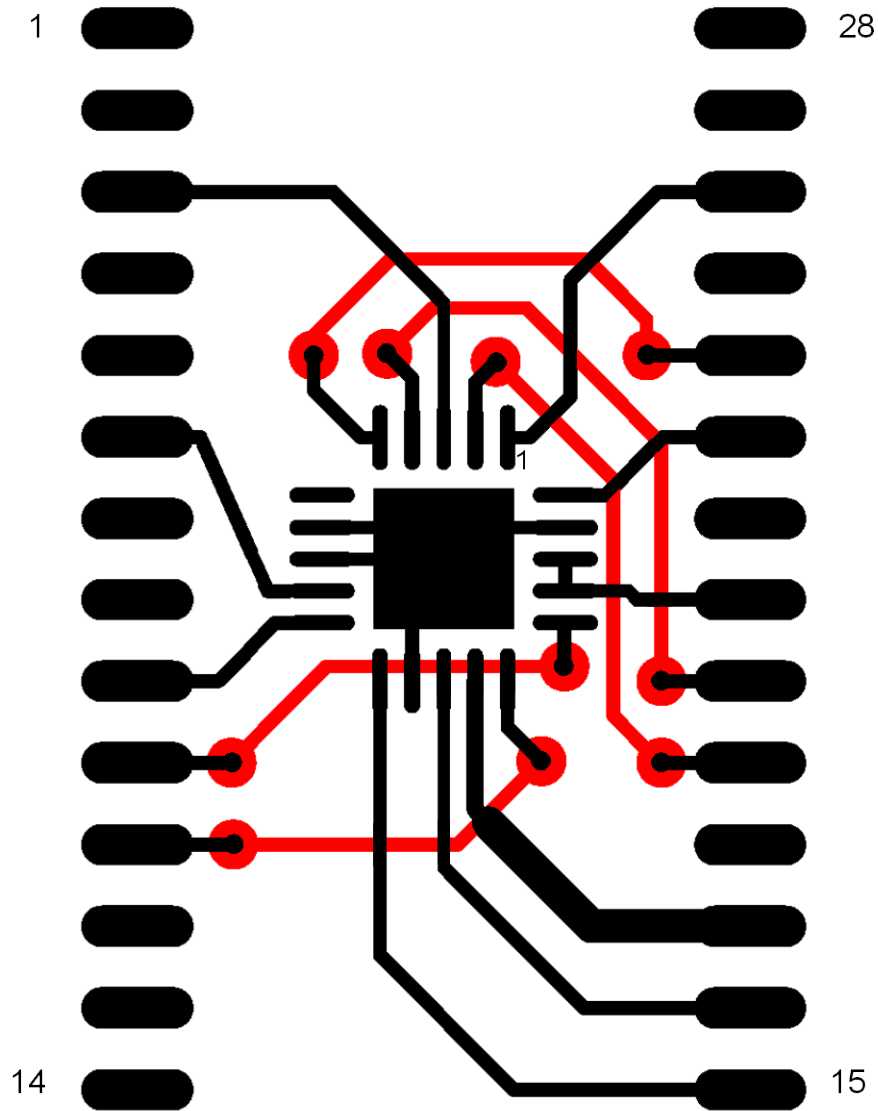


Figure 5: Teridian 73S8009R QFN 20 Pin Pinout

The dual footprint PCB layout of the above schematic is shown below. The black (dark) traces are the top layer and the red (light) traces are the bottom layer.

Note: The Teridian 73S8009R 20QFN package has a thermal pad on the bottom of the package that is connected to the substrate ground on the 73S8009R die. The thermal pad is not necessary for thermal purposes and connection to ground is optional as the 73S8009R is a low power device and generates very little heat. If not using a matching exposed pad on the PCB, any traces and vias underneath the 73S8009R should have solder mask to prevent any potential short circuits.



**Figure 6: Dual Footprint with 73S8009R QFN20
– Detail of the signal routing within the 8024 SO28 –**

Bills of Materials

Table 4 shows the differences in bills of materials between each device: 73S8009R, 73S8024RN and TDA8024 / ST8024. **The fewer components required by the Teridian 73S8009R / 73S8024RN ICs result in a cost saving in the range of a few cents with regard to BOM and assembly costs.**

Table 4: Part Differences between the 8024 Devices and the 73S8009R

Component Description	TDA8024T	ST8024	73S8024RN	73S8009R
VPC large Capacitor	10 μ F	10 μ F	10 μ F	10 μ F
VPC small Capacitor	0.1 μ F	0.1 μ F	0.1 μ F	0.1 μ F
DC/DC converter capacitor (S1/S2)	0.1 μ F	0.1 μ F	–	–
DC/DC converter decoupling capacitor (V_{UP})	0.1 μ F	0.1 μ F	–	–
VCC decoupling capacitors	0.1 μ F, 200 nF	0.1 μ F, 200 nF	1 μ F	1 μ F
VDD decoupling capacitor	0.1 μ F	0.1 μ F	0.1 μ F	0.1 μ F

Practical Implementation: Firmware Aspects

1. **Card Voltage Selection:** The control of the $\overline{\text{CMDVCC}}$ / $5\text{V}/3\text{V}$ signals on 8024-based designs need to transition to the $\overline{\text{CMDVCC5}}$ / $\overline{\text{CMDVCC3}}$ respective signals on the Teridian 73S8009R. Table 5 shows the truth table for both 8024-based designs and the Teridian 73S8009R.

Table 5: VCC Control Signal Differences

8024-based			73S8009R		
$\overline{\text{CMDVCC}}$	$5\text{V}/3\text{V}$	VCC	$\overline{\text{CMDVCC5}}$	$\overline{\text{CMDVCC3}}$	VCC
0	0	5 V	0*	0*	1.8 V
0	1	3 V	0	1	5 V
1	0	0 V	1	0	3 V
1	1	0 V (Off)	1	1	0 V (Off)

* The $\overline{\text{CMDVCC5}}$ and $\overline{\text{CMDVCC3}}$ signals must both go low within 400 ns of each other to properly generate the 1.8 V output. See the Teridian *73S8009R Data Sheet* for details.

The firmware must be modified to handle the changes shown in the truth table above. This should be simple to implement as the control signals are typically controlled by general purpose I/Os on the host processor.

2. **Card Activation / Deactivation:** Each of the 8024 type devices has specific activation and deactivation timings. The 73S8024RN has a built in sequencer that differs from the other 8024 types of devices. See the *Teridian 73S8024RN versus Phillips TDA8024T Application Note* for further information regarding the sequencer on the 73S8024RN.

The activation sequence is initiated by taking $\overline{\text{CMDVCC}}$ low. The sequencer in each device will start the activation sequence differently depending on the state of the RSTIN signal at the falling edge of $\overline{\text{CMDVCC}}$. Figure 7 shows the activation timing for the 73S8024RN when RSTIN is low during activation. The timing of the ST8024 and TDA8024T are slightly different where t_2 is 50 to 130 μ s from t_0 , t_3 is 200 ns after t_2 and they will enable the RST output be follow the RSTIN input after only a maximum time of 220 μ s from t_0 (t_4).

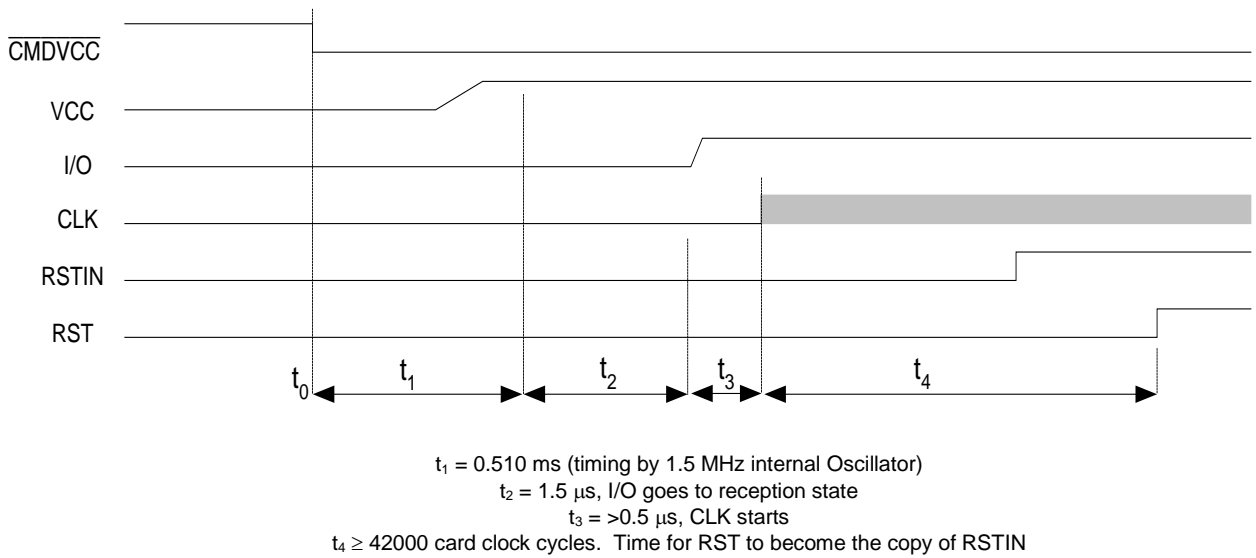


Figure 7: 73S8024RN Activation Timing with RSTIN Low

Figure 8 shows the 73S8024RN activation sequence when RSTIN is high during activation. In this mode, the activation sequence is halted until the RSTIN input is taken low by the host. At this point, the activation will continue normally.

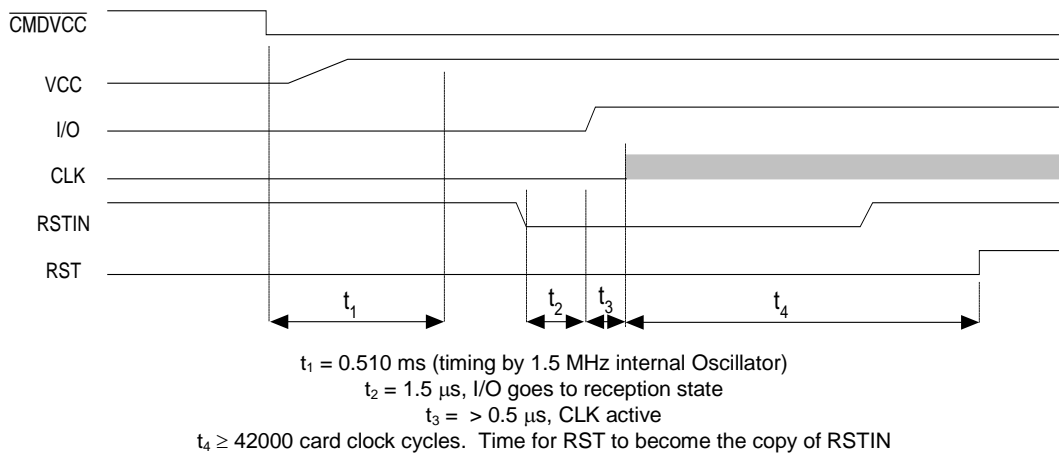


Figure 8: 73S8024RN Activation Timing with RSTIN High

When using the 73S8009R, the timing of the smart card signals is entirely up to the host to control. As a result, the host firmware has to control the timing of the I/O, CLKIN and RSTIN signals. Figure 9 shows the flowchart of the firmware control necessary for the 73S8009R device.

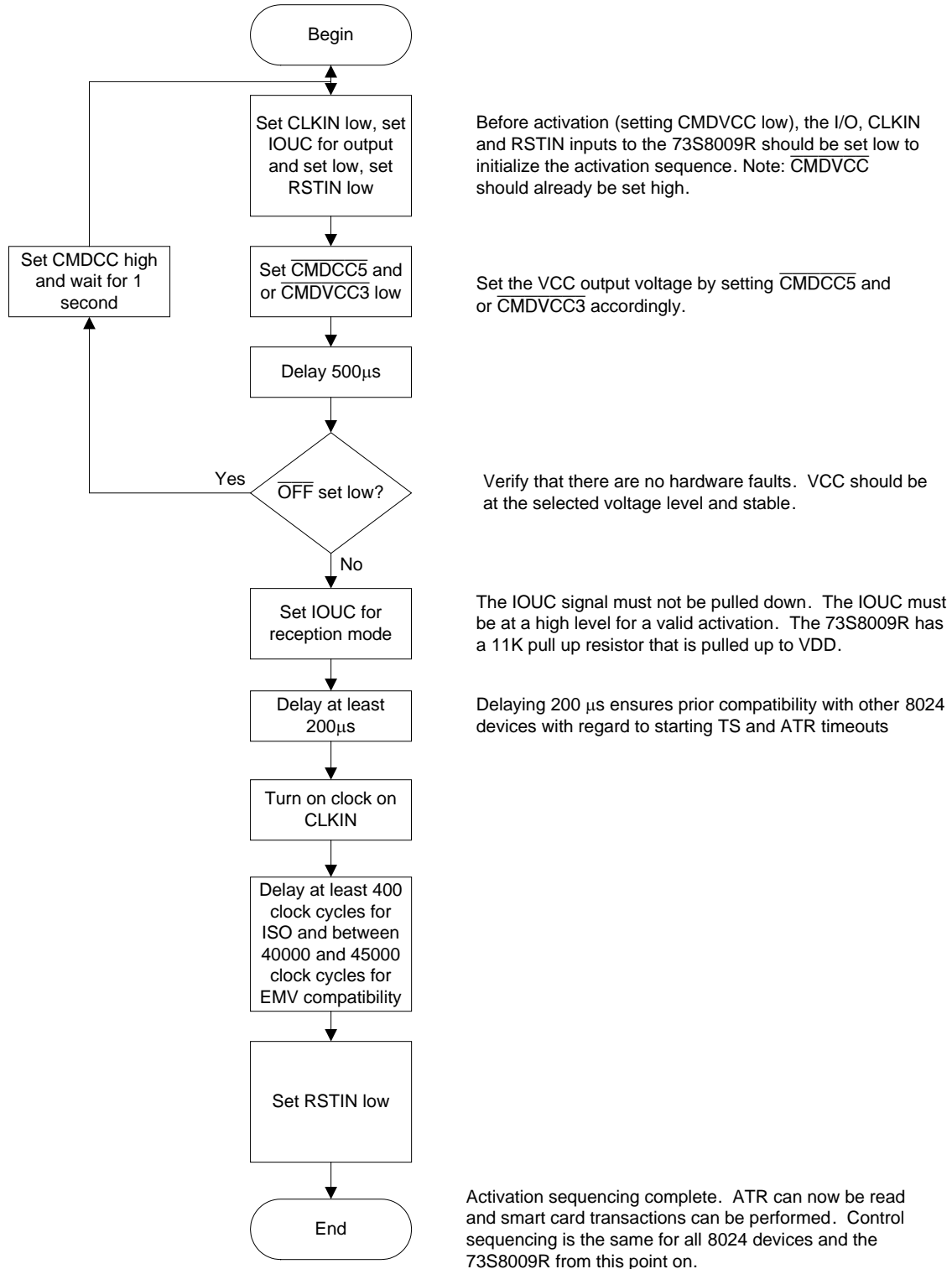


Figure 9: Activation Flowchart for the 73S8009R

The 73S8009R has an emergency deactivation controller that works the same as the 8024 devices. The deactivation timing of the 73S8009R by card removal is shown in Figure 10. The timing is the same if both $\overline{\text{CMDCC5}}$ and $\overline{\text{CMDVCC3}}$ are set high. It should be noted that an emergency deactivation might truncate the CLK output. For this reason, the host should manually deactivate the IOUC, CLK and RSTIN signals. The RSTIN should be set low first. Wait for about 10 μs and stop the clock after a full cycle has completed where CLK is low. Wait about 10 μs and then set the IOUC signal for output and set it low. Wait 10 μs and set both $\overline{\text{CMDCC5}}$ and $\overline{\text{CMDVCC3}}$ high.

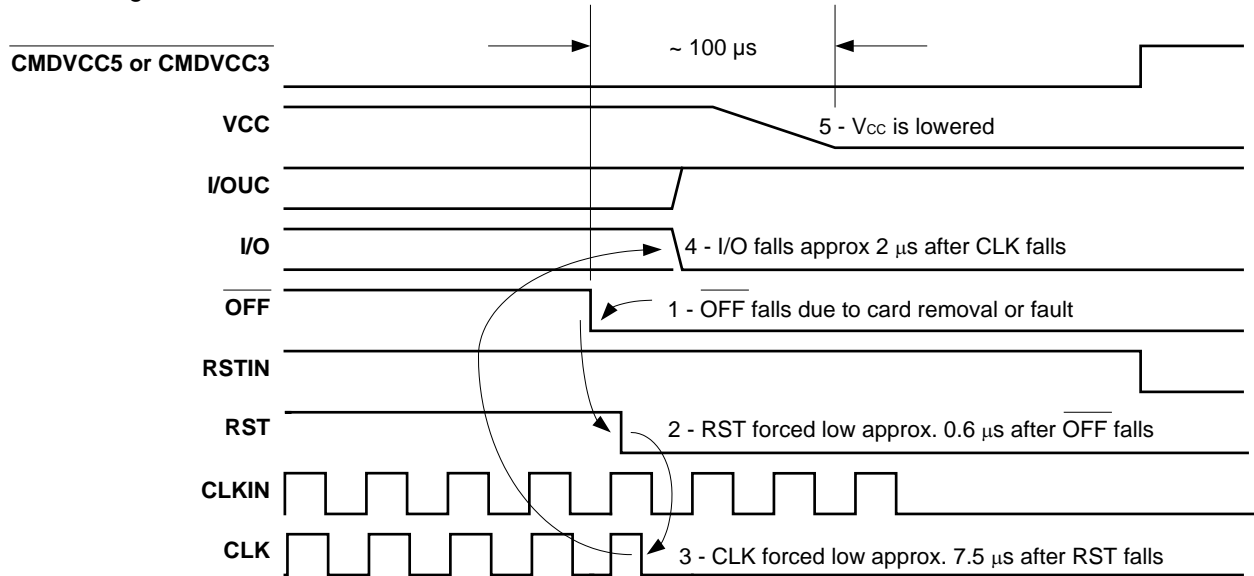


Figure 10: Deactivation Timing for the 73S8009R

Appendix – 73S8009R versus TDA8024 / ST8024

The Teridian LDO regulator-based interface devices (73S8024RN, 73S8009R and any 73S80xxR) hold several advantages over the traditional low-performance charge-pump capacitor based 8024 devices. These advantages are especially apparent in the areas of low noise and low power dissipation.

Low Noise

Like any other 73S80xxR devices, the advantages of the Teridian 73S8009R are easily seen when monitoring and comparing the noise on the ground and supply pins against those of the other 8024 parts. This comparison compares the 73S8024RN / 73S8009R against the TDA8024T. The TDA8024T shares the same kind of DC – DC as the ST8024, so the performance of each device should be similar.

The comparisons between the Teridian 73S8024RN (73S8009R) and NXP TDA8024T were measured on the same reference PCB. The Teridian 73S8024RN (73S8009R) had from four to ten times less noise on the supply and ground pins. Table 6 and Figures 11 through 16 show the actual measurements and the oscilloscope pictures that clearly show the superiority of the Teridian 73S8024RN (73S8009R) IC.

Table 6: Noise Comparison

	LDO - 73S8024RN(73S8009R)	DC/DC Converter – TDA8024T	Figure #
	Peak-to-Peak [mVpp]	Peak-to-Peak [mVpp]	
GND (Pin 4)	40	125	Fig. 11, 12
VPC/VDDp (Pin 6)	160	808	Fig. 13, 14
VDD (Pin 21)	62	121	Fig. 15, 16

Test Conditions

V_{PC}/V_{DDP} (Pin 6) = 5.0 [V]

V_{DD} (Pin 21) = 3.3 [V]

I_{CC} (@ V_{CC}) ~ 55 mA

Ta: Room temperature

All signals are measured with respect to a pre-defined reference point. (GND on test PCB)

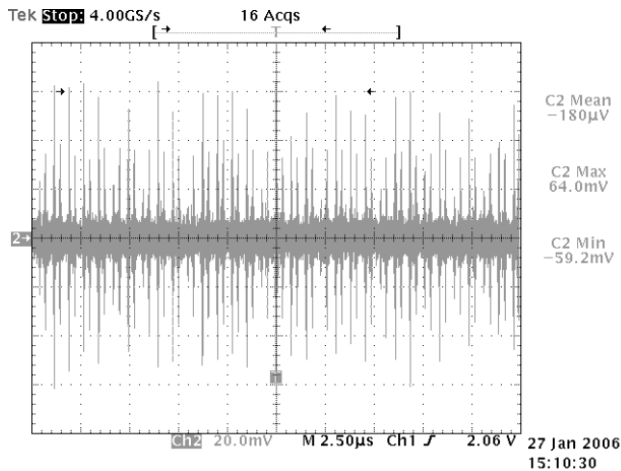


Figure 11: Teridian 73S8024RN (73S8009R), GND

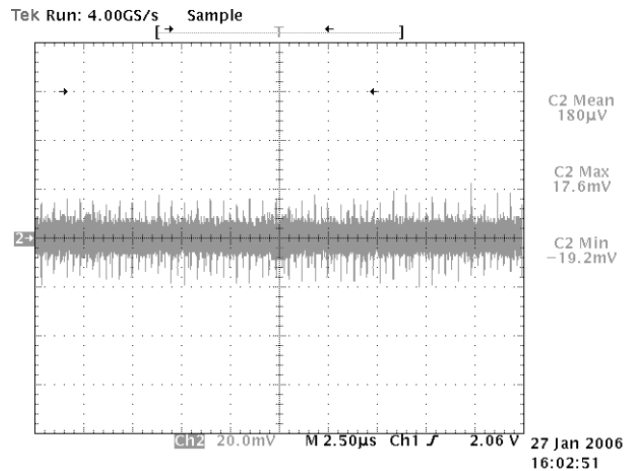


Figure 12: Philips TDA8024T, GND

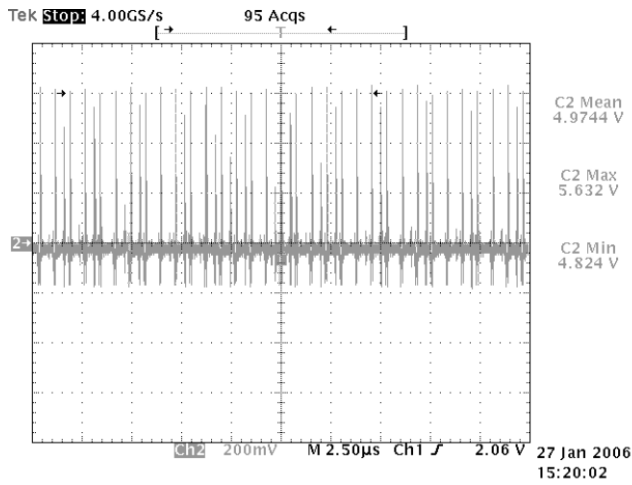


Figure 13: 73S8024RN (73S8009R) VPC, Regulator Supply

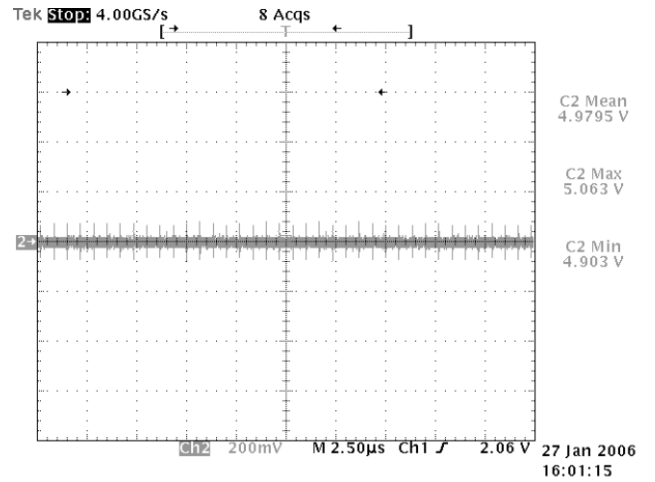


Figure 14: TDA8024T VDDP, DC/DC Converter Power Supply

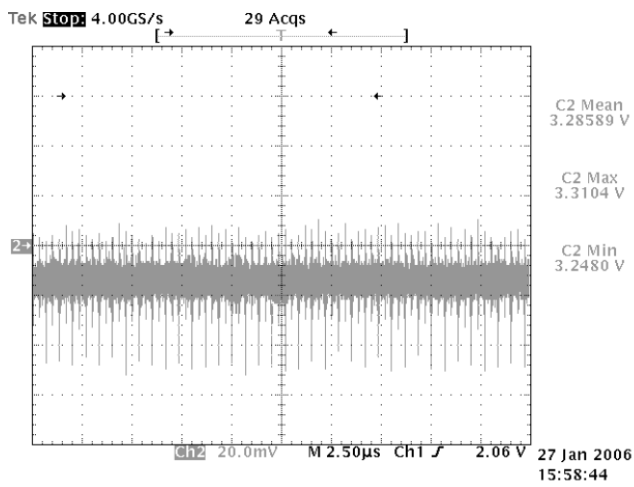


Figure 15: 73S8024RN (73S8009R) V_{DD} Digital Power Supply (Pin 21)

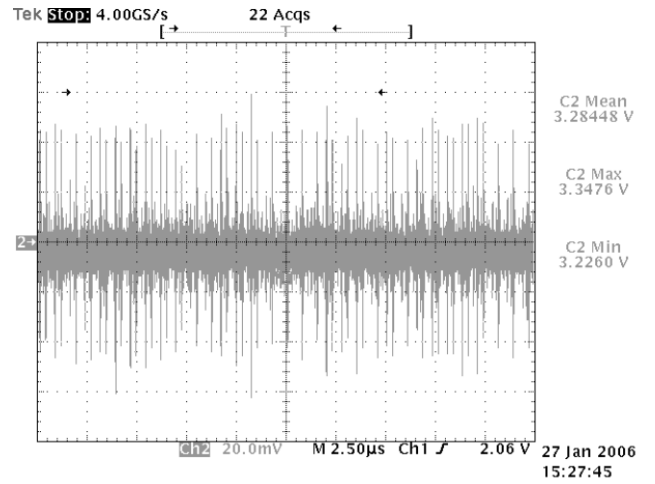


Figure 16: TDA8024T V_{DD} Digital Power Supply (Pin 21)

Low Power Dissipation

The 73S8009R uses an LDO regulator for the smart card power supply (V_{CC}), while the NXP TDA8024T device use a DC/DC converter, which is not nearly as efficient as an LDO regulator. The following graph shows the difference between the TDA8024T converter loss and the 73S8024RN (73S8009R) regulator loss.

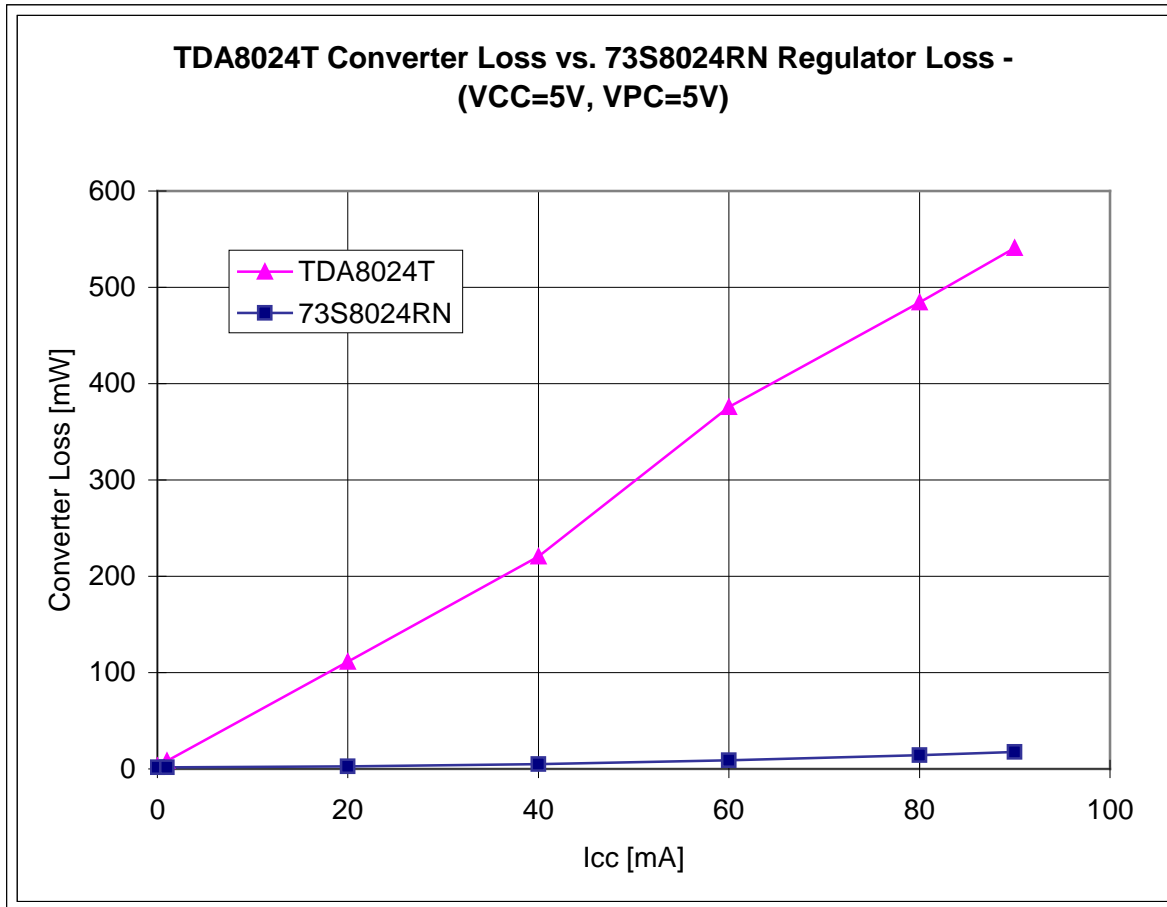


Figure 17: Teridian 73S8024RN (73S8009R), GND

Revision History

Revision	Date	Description
1.0	3/31/2008	First publication.
1.1	2/11/2010	Assigned new document number. Miscellaneous editorial changes.