# DATA SHEET

## PCK12429

25–400 MHz differential PECL clock generator

Product data
Supersedes data of 2002 Mar 15

2002 Jun 03

Philips Semiconductors

PHILIPS

# 25–400 MHz differential PECL clock generator PCK12429

## INTRODUCTION

The PCK12429 is a general purpose synthesized clock source targeting applications that require both serial and parallel interfaces. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4, or 8. With the output configured to divide the VCO frequency by 2, and with a 16.000 MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1 MHz steps. The PLL loop filter is fully integrated so that no external components are required.

## FEATURES

- 25 to 400 MHz differential PECL outputs
- ±25 ps peak-to-peak output jitter
- Fully integrated phase-locked loop
- Minimal frequency over-shoot
- Synthesized architecture
- Serial 3-wire interface
- Parallel interface for power-up
- Quartz crystal interface
- Package offer: SO28, PLCC28, and LQFP32
- Operates from 3.3 V power supply

## DESCRIPTION

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 16 before being sent to the phase detector.

The VCO output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated in 50 Ω to $V_{CC}$–2.0. The positive reference for the output driver and the internal logic is separated from the power supply for the phase-locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

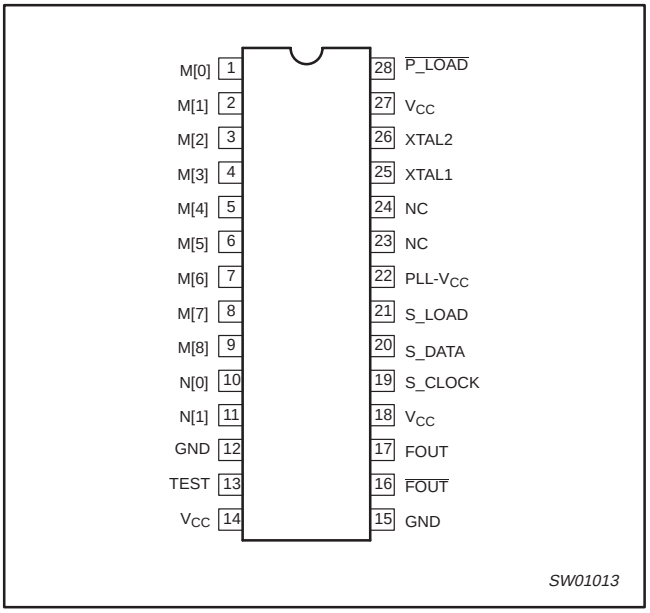
The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

## ORDERING INFORMATION

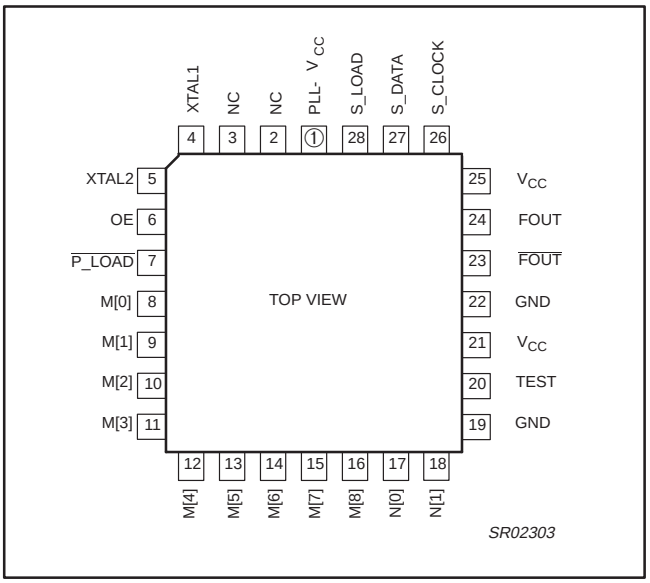
| PACKAGES | TEMPERATURE RANGE | ORDER CODE | DRAWING NUMBER |
|---|---|---|---|
| 28-Pin Plastic SO | 0 to +70 °C | PCK12429D | SOT136-1 |
| 28-Pin Plastic PLCC | 0 to +70 °C | PCK12429A | SOT261-2 |
| 32-pin Plastic LQFP | 0 to +70 °C | PCK12429BD | SOT358-1 |

## PIN CONFIGURATION

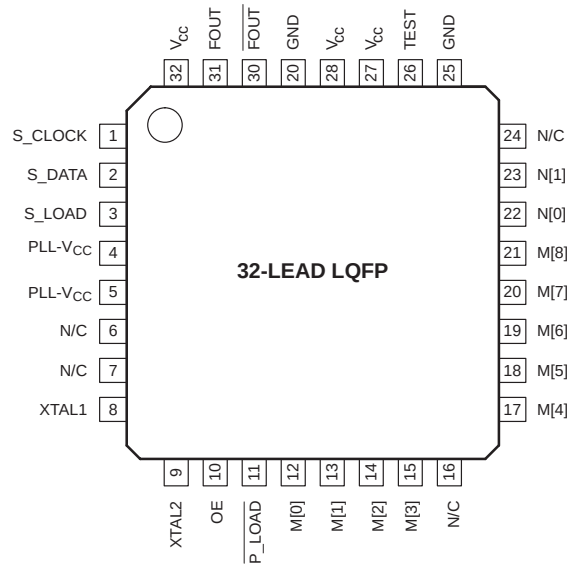
### 28-Pin SO




### 28-Pin PLCC



### 32-Pin LQFP

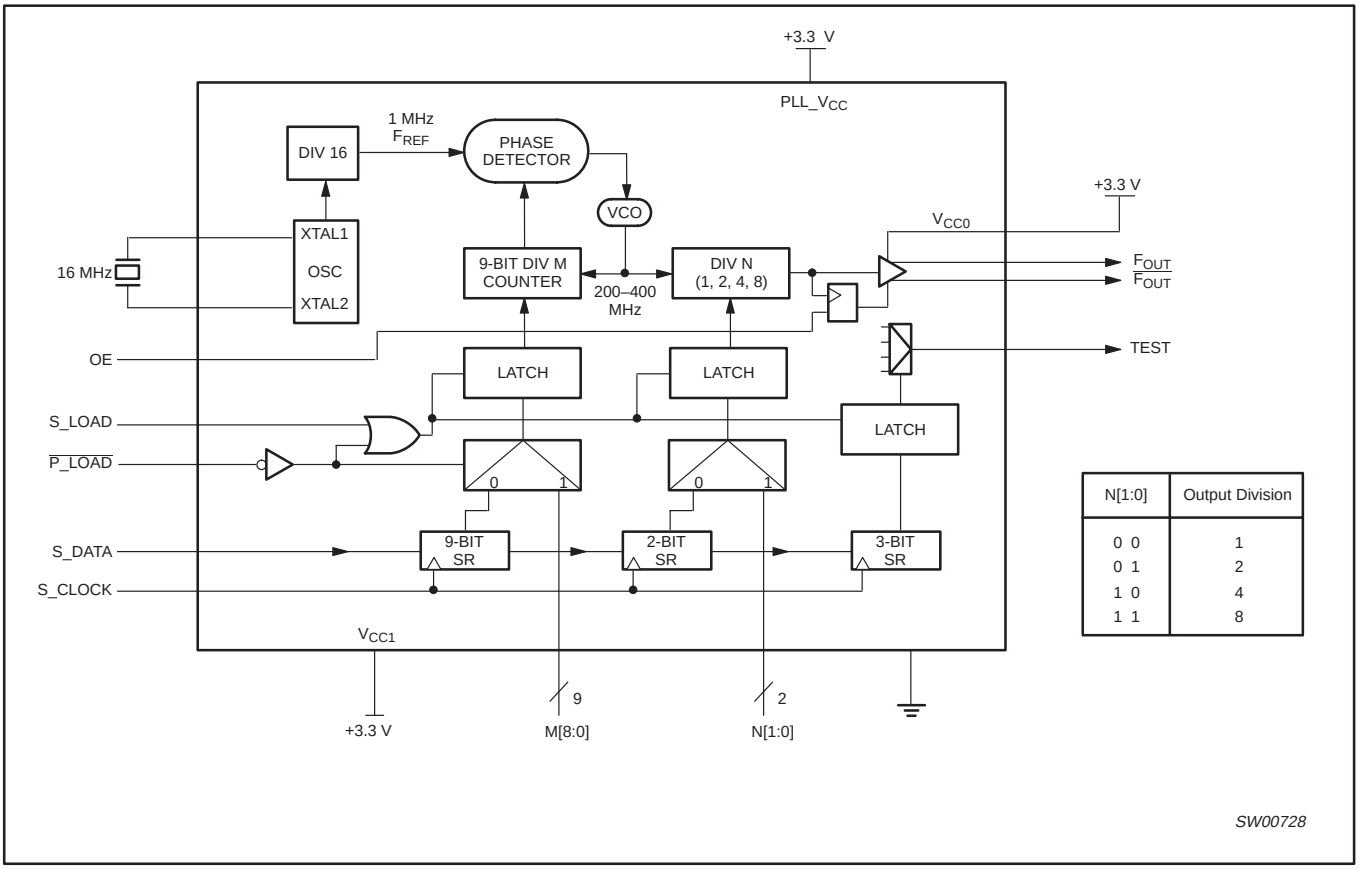



*SW01012*

### PIN DESCRIPTION

| SYMBOL | FUNCTION |
|---|---|
| XTAL1, XTAL2 | These pins form an oscillator when connected to an external series-resonant crystal. |
| S_LOAD (Int. pulldown) | This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation. |
| S_DATA (Int. pulldown) | This pin acts as the data input to the serial configuration shift registers. |
| S_CLOCK (Int. pulldown) | This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge. |
| $\overline{\text{P\_LOAD}}$ (Int. pullup) | This pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation. |
| M[8:0] (Int. pullup) | These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of P_LOAD, M[8] is the MSB, M[0] is the LSB. |
| N[1:0] (Int. pullup) | These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$. |
| OE (Int. pullup) | Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the $F_{OUT}$ output. |
| $F_{OUT}$, $\overline{F_{OUT}}$ | These differential positive-referenced ECL signals (PECL) are the output of the synthesizer. |
| TEST | The function of this output is determined by the serial configuration bits T[2:0]. |
| $V_{CC1}$ and $V_{CCO}$ | This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3 V ($V_{CC}$ = PLL_$V_{CC}$). |
| PLL_$V_{CC}$ | This is the positive supply for the PLL, and should be as noise-free as possible for low-jitter operation. This supply is connected to +3.3 V ($V_{CC}$ = PLL_$V_{CC}$). |
| GND | These pins are the negative supply for the chip and are normally all connected to ground. |

## BLOCK DIAGRAM




| N[1:0] | Output Division |
|---|---|
| 0 0 | 1 |
| 0 1 | 2 |
| 1 0 | 4 |
| 1 1 | 8 |

## PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$F_{OUT} = (F_{XTAL} \div 16) \times M \div N \quad (1)$$

Where $F_{XTAL}$ is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \le M \le 400$ for a 16 MHz input reference.

Assuming that a 16 MHz reference frequency is used, the above equation reduces to:

$$F_{OUT} = M \div N$$

Substituting the four values for N (1, 2, 4, or 8) yields:

$F_{OUT} = M$, $F_{OUT} = M \div 2$,
$F_{OUT} = M \div 4$ and $F_{OUT} = M \div 8$
for $200 \le M \le 400$

The user can identify the proper M and N values for the desired frequency from the above equations. The four output frequency ranges established by N are 200–400 MHz, 100–200 MHz, 50–100 MHz, and 25–50 MHz respectively. From these ranges the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example, if an output frequency of 131 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 131 MHz falls within the frequency range set by an N value of 2 so N [1:0] = 01. For N = 2 $F_{OUT} = M \div 2$ and $M = 2 \times F_{OUT}$. Therefore, $M = 131 \times 2 = 262$, so M[8:0] = 100000110. Following this same procedure a user can generate any whole frequency desired between 25 and 400 MHz. Note that for $N \ge 2$ fractional values of $F_{OUT}$ can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to $F_{XTAL} \div 16 \div N$.

For input reference frequencies other than 16 MHz, the set of appropriate equations can be deduced from equation 1. For computer applications another useful frequency base would be 16.666 MHz. From this reference, one can generate a family of output frequencies at multiples of the 33.333 MHz PCI clock. As an example, to generate a 133.333 MHz clock from a 16.666 MHz reference, the following M and N values would be used:

$$F_{OUT} = 16.666 \div 16 \times M \div N = 1.041625 \times M \div N$$

Let N = 2, M = 256,
$F_{OUT} = 1.041625 \times 256 \div 2 = 133.328$ MHz

The value for M falls within the constraints set for PLL stability, therefore N[1:0] = 01 and M[8:0] = 100000000. If the value for M fell outside of the valid range a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will

affect the $F_{OUT}$ output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14-bit shift register. Note that the $\overline{P\_LOAD}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1, and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH_to_LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 1 illustrates the timing diagram for both a parallel and a serial load of the PCK12429 synthesizer.

M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available. To minimize transients in the frequency domain, the output should be varied in the smallest step size possible. The bandwidth of the PLL is such that frequency stepping in 1 MHz steps at the maximum S_CLOCK frequency or less will cause smooth, controlled slewing of the output frequency.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents $F_{OUT}$, the CMOS output may may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1, and T0 control bits are preset to '000' when $\overline{P\_LOAD}$ is LOW so that the PECL $F_{OUT}$ outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the PCK12429 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the PCK12429 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the $F_{OUT}$ differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed broad level functional test or debug. Bypassing the PLL and driving $F_{OUT}$ directly, gives the user more control on the test clocks sent through the clock tree. Figure 2 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250 MHz or less. This means the fastest the $F_{OUT}$ pin can be toggled via the S_CLOCK is 125 MHz, as the minimum divide ratio of the N counter is 2. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

**Table 1. Test modes**

| T2 | T1 | T0 | TEST (Pin 20) |
|---|---|---|---|
| 0 | 0 | 0 | SHIFT REGISTER OUT |
| 0 | 0 | 1 | HIGH |
| 0 | 1 | 0 | $F_{REF}$ |
| 0 | 1 | 1 | M COUNTER OUT |
| 1 | 0 | 0 | $F_{OUT}$ |
| 1 | 0 | 1 | LOW |
| 1 | 1 | 0 | PLL BYPASS |
| 1 | 1 | 1 | $F_{OUT}$/4 |

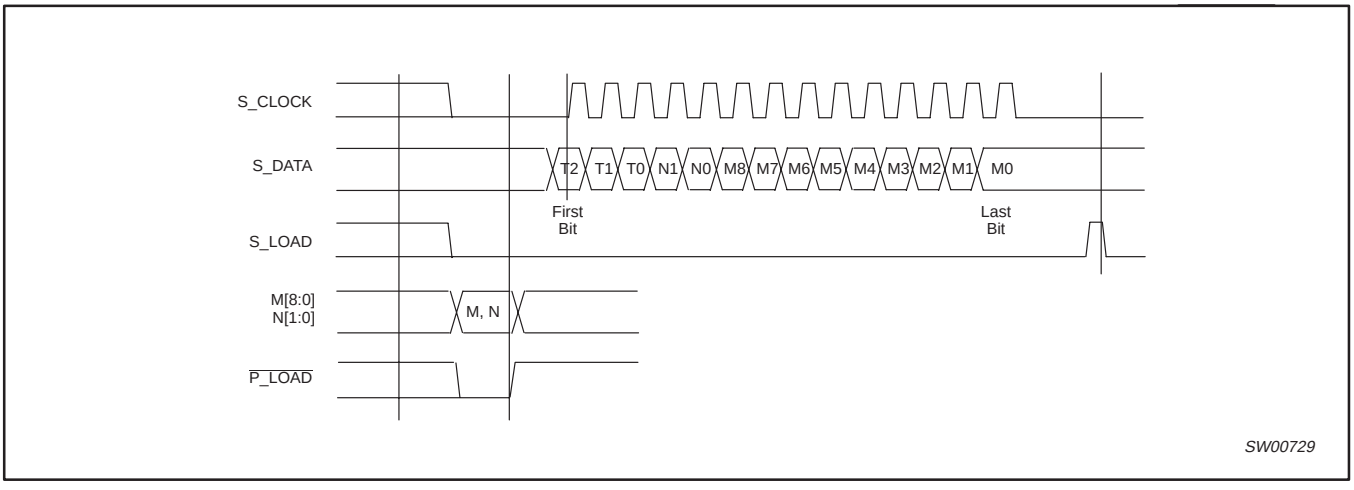
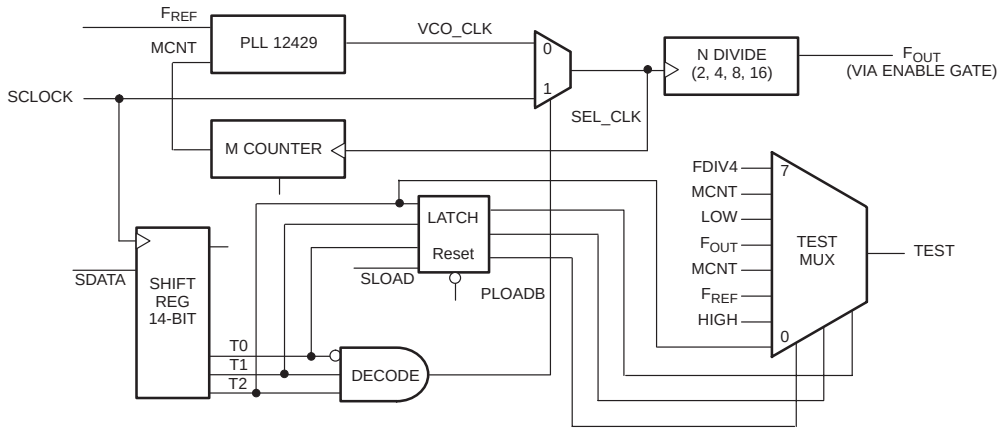



**Figure 1. Timing Diagram**




- T2 = T1 = 1. T0 = 0: Test Mode
- SCLOCK is selected, MCNT is on TEST output, SCLOCK DIVIDE BY N is on $F_{OUT}$ pin.

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

*SW00730*

**Figure 2. Serial Test Clock Block Diagram**

## DC CHARACTERISTICS ($T_{amb}$ = 0 to 70 °C, $V_{CC}$ = 3.3 V ± 5%)

| SYMBOL | PARAMETER | | CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $V_{IH}$ | Input HIGH Voltage | | $V_{CC}$ = 3.3 V | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | | $V_{CC}$ = 3.3 V | — | — | 0.8 | V |
| $I_{IN}$ | Input Current | | | — | — | 1.0 | mA |
| $V_{OH}$ | Output HIGH Voltage | TEST | $I_{OH}$ = –0.8 mA | 2.5 | — | | V |
| $V_{OL}$ | Output LOW Voltage | TEST | $I_{OL}$ = 0.8 mA | — | — | 0.4 | V |
| $V_{OH}$ | Output HIGH Voltage | $F_{OUT}$<br>$\overline{F_{OUT}}$ | $V_{CC0}$ = 3.3 V (Notes 1 and 2) | 2.17 | — | 2.50 | V |
| $V_{OL}$ | Output LOW Voltage | $F_{OUT}$<br>$\overline{F_{OUT}}$ | $V_{CC0}$ = 3.3 V (Notes 1 and 2) | 1.41 | — | 1.76 | V |
| $I_{CC}$ | Power Supply Current | $V_{CC1}$<br>PLL_$V_{CC}$ | | — | 85<br>15 | 100<br>20 | mA |

**NOTES:**
1. Output levels will vary 1:1 with $V_{CC0}$ variation.
2. 50 Ω to $V_{CC}$ – 2.0 V pulldown.

**AC CHARACTERISTICS** ($T_{amb}$ = 0 to 70 °C, $V_{CC}$ = 3.3 V ± 5%)

| SYMBOL | PARAMETER | | TEST CONDITIONS | LIMITS $T_{amb}$ = 0 to +70 °C | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| $F_{MAXI}$ | Maximum Input Frequency | S_CLOCK | Note 1 | — | 10 | MHz |
| | | Xtal Oscillator | | 10 | 20 | |
| $F_{MAXO}$ | Maximum Output Frequency | VCO (Internal) | Note 2 | 200 | 400 | MHz |
| | | $F_{OUT}$ | | 25 | 400 | |
| $t_{LOCK}$ | Maximum PLL Lock Time | | | — | 10 | ms |
| $t_{jitter}$ | RMS jitter (peak-to-peak) | | Note 2 See Applications Section | — | ±25 | ps |
| $t_s$ | Setup Time | S_DATA to S_CLOCK | | 20 | — | ns |
| | | S_CLOCK TO S_LOAD | | 20 | — | |
| | | M, N to $\overline{P\_LOAD}$ | | 20 | — | |
| $t_n$ | Hold Time | S_DATA to S_CLOCK | | 20 | — | ns |
| | | M, N to $\overline{P\_LOAD}$ | | 20 | — | |
| $tpw_{MIN}$ | Minimum Pulse Width | S_LOAD | Note 2 | 50 | — | ns |
| | | $\overline{P\_LOAD}$ | | 50 | — | |
| $t_r$, $t_f$ | Output Rise/Fall | $F_{OUT}$ | 20%–80%, Note 2 | 100 | 400 | ps |
| Duty Cycle | | | | 45 | 55 | % |

**NOTES:**
1. 10 MHz is the maximum frequency to load the feedback device registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6. Crystal frequency of 16MHz verified at productiontest. 10 to 20MHz operationguaranteed by design.
2. 50 Ω to $V_{CC}$–2.0 V pulldown.

## APPLICATIONS INFORMATION

### Using the on-board crystal oscillator

The PCK12429 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the PCK12429 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the XTAL terminals, loading variation introduced by crystals from different vendors could be a potential issue.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the PCK12429 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 2 specifies the performance requirements of the crystals to be used with the PCK12429.

### Table 2. Test modes

| PARAMETER | VALUE |
|---|---|
| Crystal Cut | Fundamental AT Cut |
| Resonance | Series Resonance* |
| Frequency Tolerance | ±75 ppm at 25 °C |
| Frequency/Temperature Stability | ±150 pm 0 to 70 °C |
| Operating Range | 0 to 70 °C |
| Shunt Capacitance | 5–7 pF |
| Equivalent Series Resistance (ESR) | 50 to 80 Ω |
| Correlation Drive Level | 100 μW |
| Aging | 5 ppm/Yr (first 3 years) |

**NOTE:**
* See accompanying text for series versus parallel resonant discussion.

## Power supply filtering

The PCK12429 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The PCK12429 provides separate power supplies for the digital circuitry ($V_{CC}$) and the internal PLL (PLL_$V_{CC}$) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_$V_{CC}$ pin for the PCK12429.

Figure 3 illustrates a typical power supply filter scheme. The PCK12429 is most susceptible to noise with spectral content in the 1 kHz to 2 MHz range. A good choice of pole placement should be close to 32 kHz. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the PLL_$V_{CC}$ pin of the PCK12429. From the data sheet the $I_{PLL\_VCC}$ current (the current sourced through the PLL_$V_{CC}$ pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 3.0 V must be maintained on the PLL_$V_{CC}$ pin, very little DC voltage drop can be tolerated when a 3.3 V $V_{CC}$ supply is used. The resistor shown in Figure 3 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

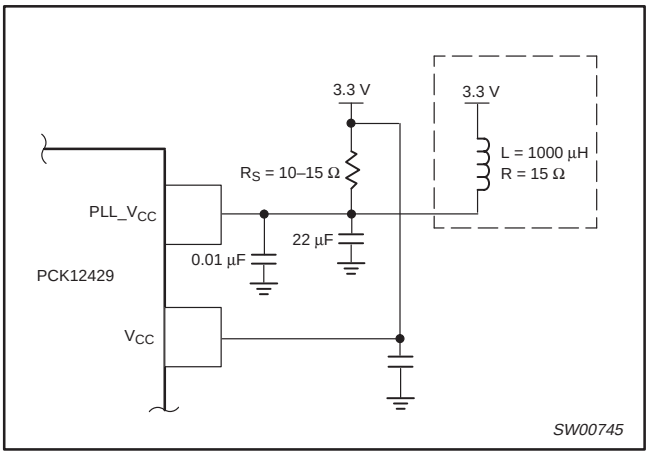



**Figure 3. Power supply filter**

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. Figure 3 shows a 1000 µH choke, this value choke will show a significant impedance at 10 KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_$V_{CC}$ pin, a low DC resistance inductor is required (less than 15 Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement, and provide an adequate level of supply filtering.

The PCK12429 provides sub-nanosecond output edge rates, and thus a good power supply bypassing scheme is a must. Figure 4 shows a representative board layout for the PCK12429. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 4 is the low impedance connections between $V_{CC}$ and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the PCK12429 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

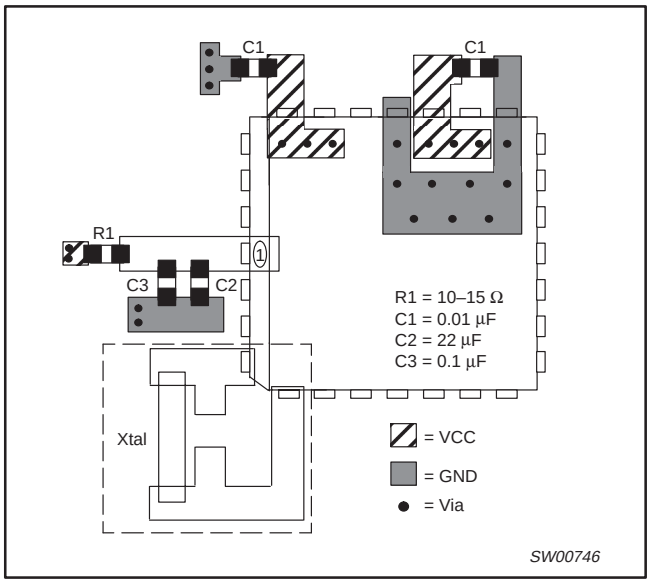



**Figure 4. PCB board layout for PCK12429**

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal, as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator.

Although the PCK12429 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

**Jitter performance of the PCK12429**

The PCK12429 exhibits long term and cycle-to-cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

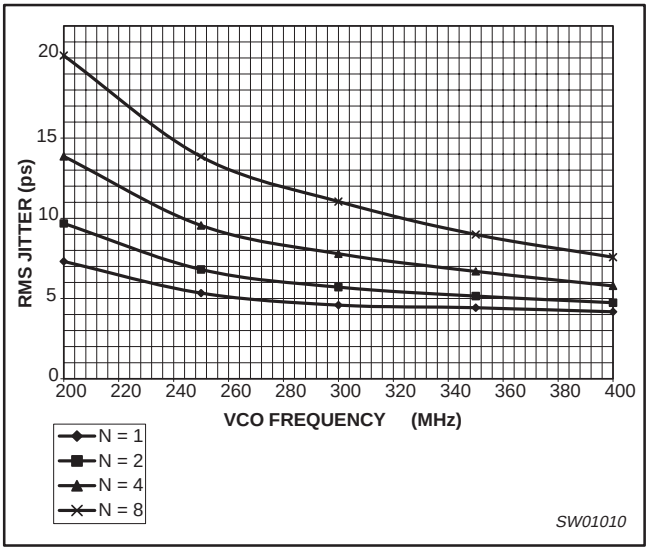



**Figure 5. RMS PLL jitter versus VCO frequency**

Figure 5 illustrates the RMS jitter performance of the PCK12429 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data. In addition the data represents long term period jitter, the cycle-to-cycle jitter could not be measured to the level of accuracy required with available test equipment but certainly will be smaller than the long term period jitter.

The most commonly specified jitter parameter is cycle-to-cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the PCK12429. As a result, different methods are used which approximate cycle-to-cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements, and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce period jitter values somewhat larger than if consecutive cycles (cycle-to-cycle jitter) were measured. All of the jitter data reported on the PCK12429 was collected in this manner.

Figure 6 shows the jitter as a function of the output frequency. For the PCK12429, this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25 ps peak-to-peak long term period jitter. The graph shows that for output frequencies from 125 to 400 MHz the jitter falls within the ±25 ps peak-to-peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

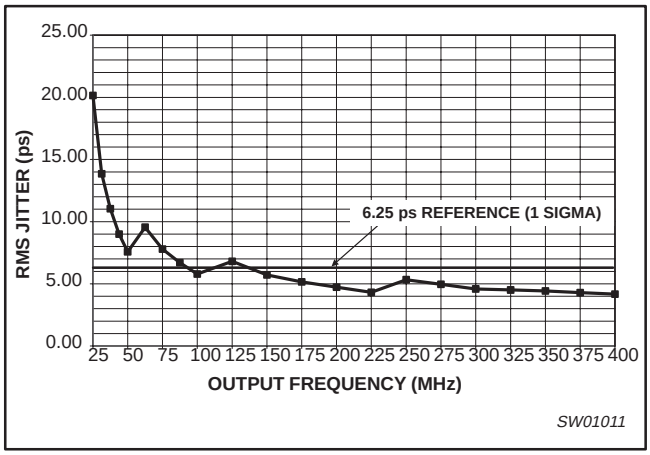
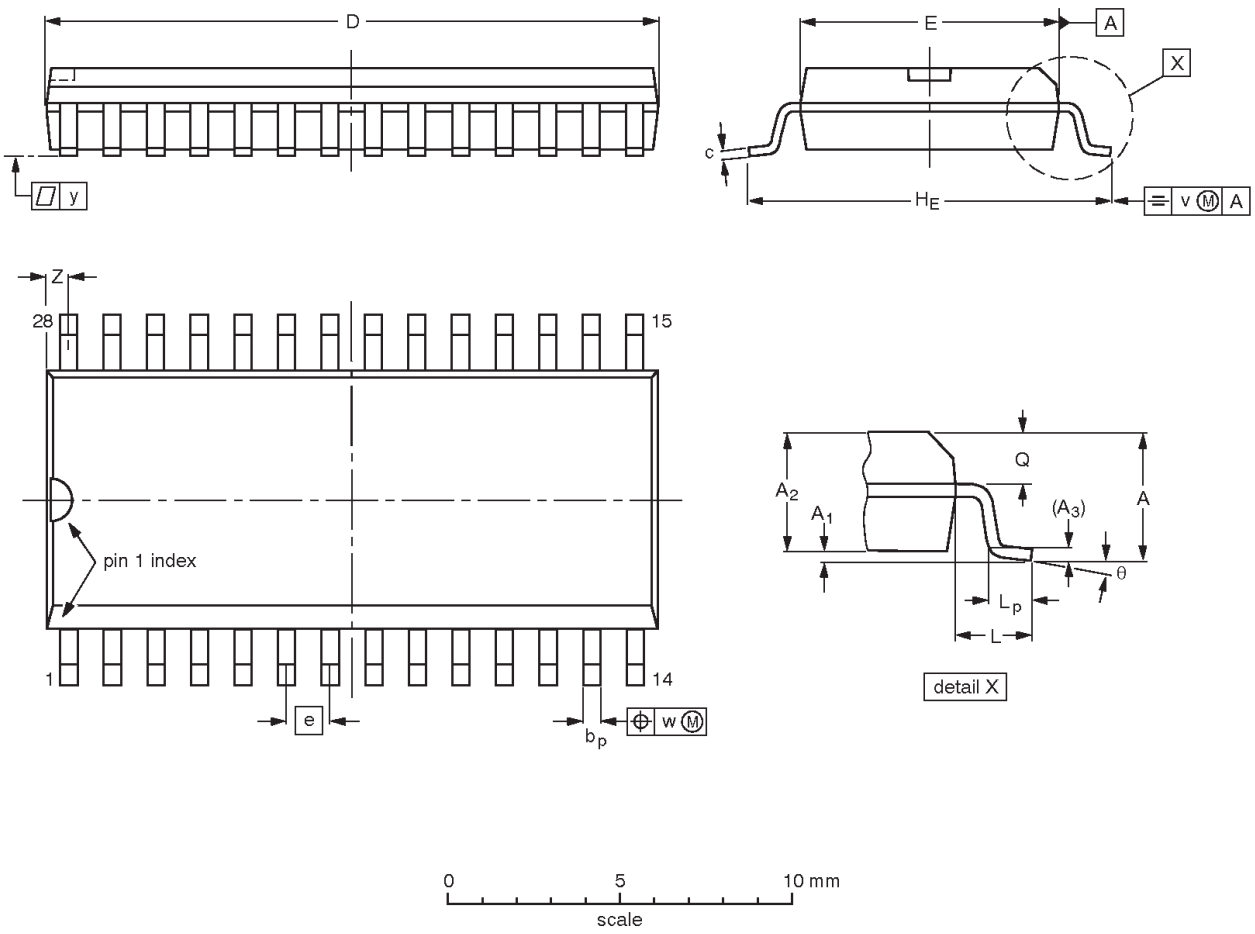



**Figure 6. RMS jitter versus output frequency**

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

**SO28: plastic small outline package; 28 leads; body width 7.5 mm** **SOT136-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

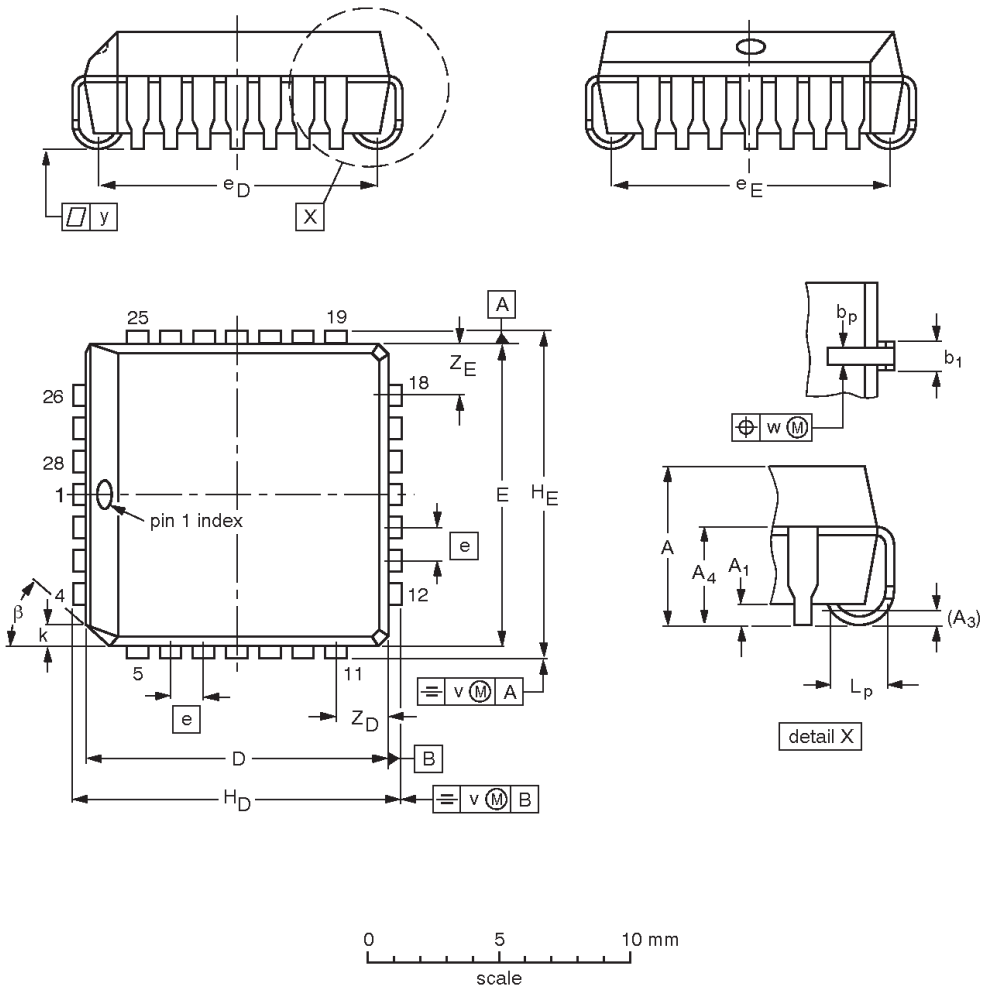
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.30<br>0.10 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 18.1<br>17.7 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.10 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.71<br>0.69 | 0.30<br>0.29 | 0.050 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT136-1 | 075E06 | MS-013 | | | | ~~97-05-22~~<br>99-12-27 |

**PLCC28: plastic leaded chip carrier; 28 leads** **SOT261-2**




**DIMENSIONS (mm dimensions are derived from the original inch dimensions)**

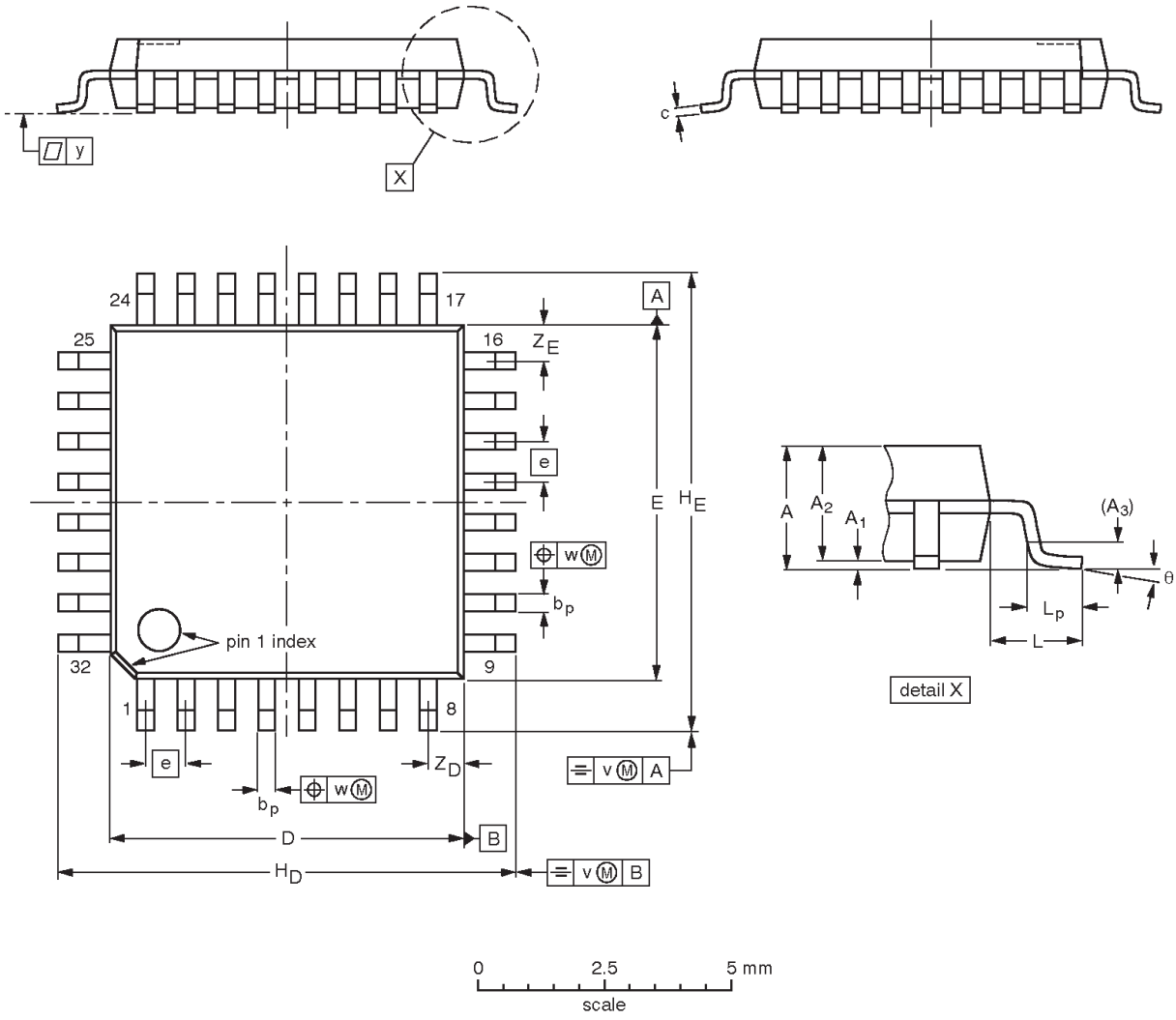
| UNIT | A | $A_1$ min. | $A_3$ | $A_4$ max. | $b_p$ | $b_1$ | $D^{(1)}$ | $E^{(1)}$ | e | $e_D$ | $e_E$ | $H_D$ | $H_E$ | k | $L_p$ | v | w | y | $Z_D^{(1)}$ max. | $Z_E^{(1)}$ max. | β |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.57<br>4.19 | 0.51 | 0.25 | 3.05 | 0.53<br>0.33 | 0.81<br>0.66 | 11.58<br>11.43 | 11.58<br>11.43 | 1.27 | 10.92<br>9.91 | 10.92<br>9.91 | 12.57<br>12.32 | 12.57<br>12.32 | 1.22<br>1.07 | 1.44<br>1.02 | 0.18 | 0.18 | 0.1 | 2.16 | 2.16 | 45° |
| inches | 0.180<br>0.165 | 0.02 | 0.01 | 0.12 | 0.021<br>0.013 | 0.032<br>0.026 | 0.456<br>0.450 | 0.456<br>0.450 | 0.05 | 0.43<br>0.39 | 0.43<br>0.39 | 0.495<br>0.485 | 0.495<br>0.485 | 0.048<br>0.042 | 0.057<br>0.040 | 0.007 | 0.007 | 0.004 | 0.085 | 0.085 | |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT261-2 | 112E08 | MS-018 | EDR-7319 | | | ~~99-12-27~~<br>01-11-15 |

**LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm** **SOT358-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.60 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.4<br>0.3 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.8 | 9.15<br>8.85 | 9.15<br>8.85 | 1.0 | 0.75<br>0.45 | 0.2 | 0.25 | 0.1 | 0.9<br>0.5 | 0.9<br>0.5 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT358 -1 | 136E03 | MS-026 | | | | ~~99-12-27~~<br>00-01-19 |

## Data sheet status

| Data sheet status [1] | Product status [2] | Definitions |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

## Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information —** Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support —** These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes —** Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## Contact information

For additional information please visit
**http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
**sales.addresses@www.semiconductors.philips.com**.



Date of release: 06-02

Document order number: 9397 750 09913

Let's make things better.

**Philips Semiconductors**

PHILIPS