

## SN74LVC2G08-Q1 Dual 2-Input Positive-AND Gate

### 1 Features

- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range (DCU package)
  - Device Temperature Grade 3: –40°C to +85°C Ambient Operating Temperature Range (DCT package)
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Can be Used as a Down Translator to Translate Input from a Maximum of 5.5 V Down to the  $V_{CC}$  Level.
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

### 2 Applications

- Combine Power Good signals for Multiple Power Rails
- Prevent a Signal from Being Passed Until a Condition is True
- Combine Active-Low Error Signals

### 3 Description

This dual 2-input positive-AND gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G08-Q1 performs the Boolean function  $Y = A \cdot B$  or  $Y = \overline{\overline{A} + \overline{B}}$  in positive logic.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2G08DCT-Q1	SM8 (8)	2.95 mm $\times$ 2.80 mm
SN74LVC2G08DCU-Q1	VSSOP (8)	2.30 mm $\times$ 2.00 mm

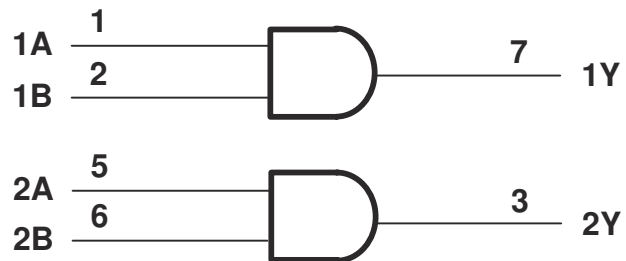


Figure 3-1. Logic Diagram (Positive Logic)



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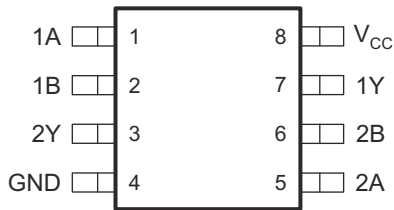
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## 4 Revision History

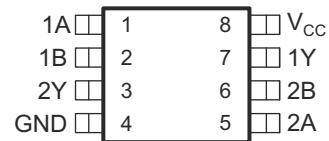
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (March 2010) to Revision E (October 2020)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Removed Typical $V_{OLP}$ (Output Ground Bound) $<0.8$ V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$ from <i>Features</i> section.....	1
• Removed Typical $V_{OHV}$ (Output $V_{OHV}$ Undershoot) $>2$ V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$ from <i>Features</i> section.....	1
• Removed the <i>Ordering Information</i> table from <i>Description</i> section.....	1
• Added a <i>Device Information</i> table to the <i>Description</i> section.....	1
• Added the <i>Logic Diagram (Positive Logic)</i> figure to the <i>Description</i> section.....	1
• Added the <i>Pin Configuration and Functions</i> section.....	3
• Added SN74LVC2G08DCT-Q1 and SN74LVC2G08DCU-Q1 minimum and maximum operating free-air temperature ranges to the <i>Recommended Operating Conditions</i> section.....	5
• Added the $T_A$ temperature ranges ( $-40^\circ\text{C}$ to $85^\circ\text{C}$ and $-40^\circ\text{C}$ to $125^\circ\text{C}$ ) for the $t_{pd}$ parameter to the <i>Switching Characteristics</i> section .....	6
• Added the <i>Typical Characteristics</i> section.....	7
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## 5 Pin Configuration and Functions



**Figure 5-1. DCT Package  
8-Pin SM8  
Top View**



**Figure 5-2. DCU Package  
8-Pin VSSOP  
Top View**

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1 logic input
1B	2	I	Channel 1 logic input
1Y	7	O	Logic level output
2A	5	I	Channel 2 logic input
2B	6	I	Channel 2 logic input
2Y	3	O	Logic level output
GND	4	—	Ground
V <sub>CC</sub>	8	—	Power Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(1)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(1)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(1) (2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current		-50	mA
$I_{OK}$	Output clamp current		-50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature range	-65	150	°C

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) The value of  $V_{CC}$  is provided in the *Recommended Operating Conditions* table.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 3 V to 3.6 V		0.8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		-4	mA
		V <sub>CC</sub> = 2.3 V		-8	
		V <sub>CC</sub> = 3 V		-16	
		V <sub>CC</sub> = 4.5 V		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 3 V		16	
		V <sub>CC</sub> = 4.5 V		24	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V		10	
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
T <sub>A</sub>	Operating free-air temperature	SN74LVC2G08DCU-Q1	-40	125	°C
		SN74LVC2G08DCT-Q1	-40	85	

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LVC2G08-Q1		UNIT
		DCT (SM8)	DCU (VSSOP)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	220	201.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	117.2	91.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	100	122.6	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	42.4	31.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	98.9	122.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = –100 μA	1.65 V to 5.5 V	V <sub>CC</sub> – 0.1			V
		I <sub>OH</sub> = –4 mA	1.65 V	1.2			
		I <sub>OH</sub> = –8 mA	2.3 V	1.9			
		I <sub>OH</sub> = –16 mA	3 V	2.4			
		I <sub>OH</sub> = –24 mA		2.3			
		I <sub>OH</sub> = –32 mA	4.5 V	3.8			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	V
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		I <sub>OL</sub> = 8 mA	2.3 V			0.3	
		I <sub>OL</sub> = 16 mA	3 V			0.4	
		I <sub>OL</sub> = 24 mA				0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μA
I <sub>CC</sub>		V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V			10	μA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND, T <sub>A</sub> = –40°C to 85°C	3 V to 5.5 V			500	μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, T <sub>A</sub> = –40°C to 85°C	3.3 V	5			pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## 6.6 Switching Characteristics

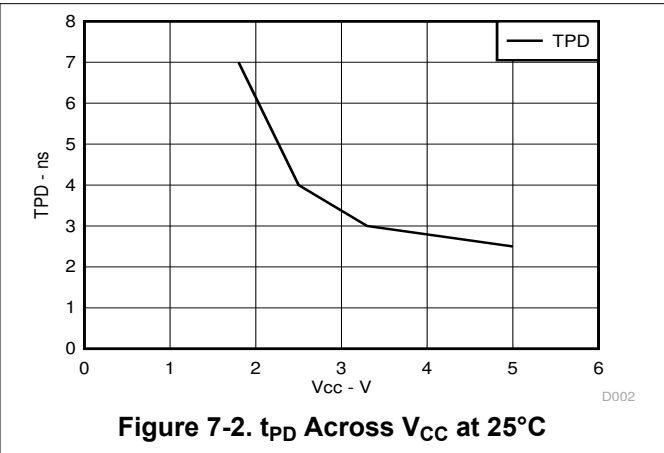
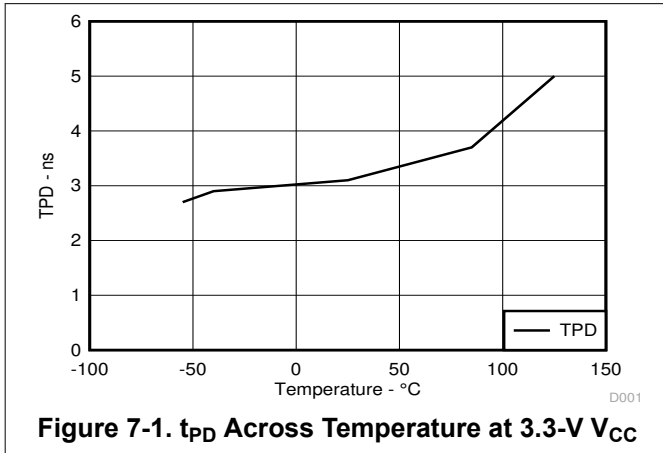
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub>	V <sub>CC</sub>	MIN	MAX	UNIT
t <sub>pd</sub>	A or B	Y	–40°C to 85°C	V <sub>CC</sub> = 1.8 V ± 0.15 V	2.6	9	ns
				V <sub>CC</sub> = 2.5 V ± 0.2 V	1	5.1	
				V <sub>CC</sub> = 3.3 V ± 0.3 V	1	4.7	
				V <sub>CC</sub> = 5 V ± 0.5 V	1	3.8	
			–40°C to 125°C	V <sub>CC</sub> = 1.8 V ± 0.15 V	2.6	9.8	
				V <sub>CC</sub> = 2.5 V ± 0.2 V	1	5.8	
				V <sub>CC</sub> = 3.3 V ± 0.3 V	1	5.3	
				V <sub>CC</sub> = 5 V ± 0.5 V	1	4.8	

## 6.7 Operating Characteristics

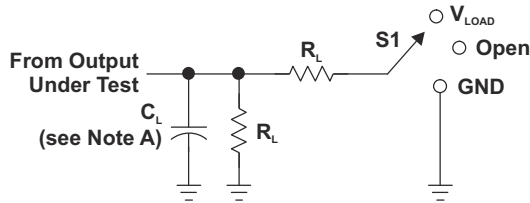
T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
		TYP	TYP	TYP	TYP		
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	17	17	17	20	pF

## 7 Typical Characteristics



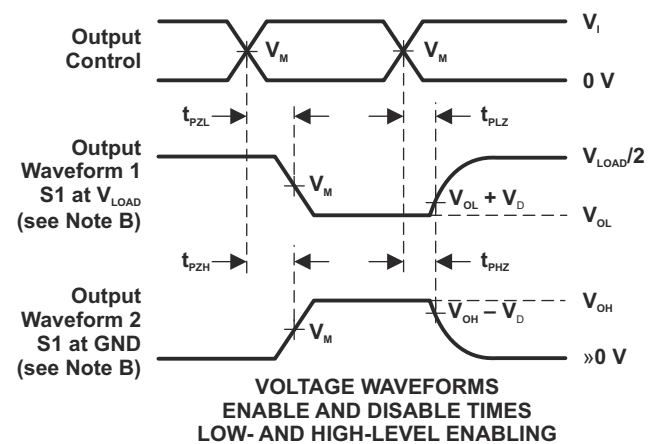
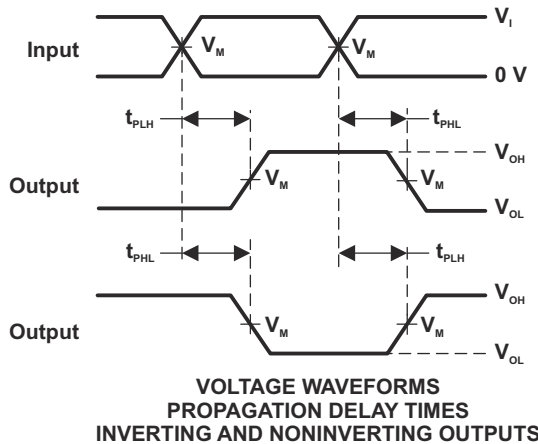
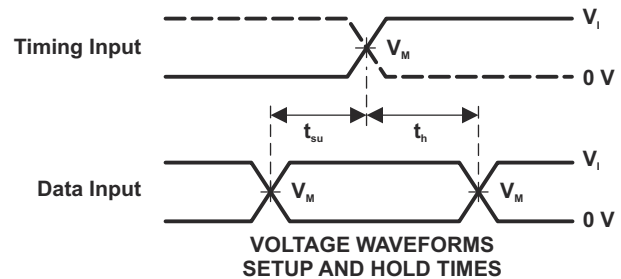
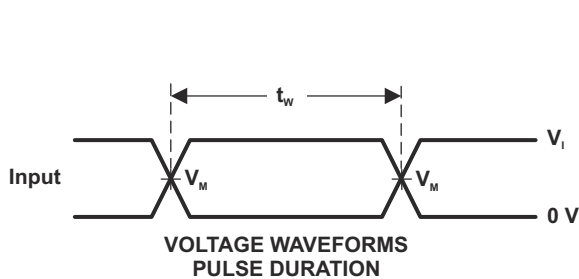
## 8 Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_D$
	$V_I$	$t/t_i$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	£2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kW	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	£2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 W	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	£2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	£2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 W	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 8-1. Load Circuit and Voltage Waveforms

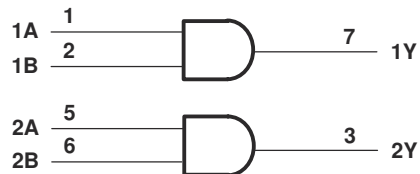


## 9 Detailed Description

### 9.1 Overview

The SN74LVC2G08-Q1 device contains two 2-input positive AND gates and performs the Boolean function  $Y = A \cdot B$  or  $Y = \overline{A + B}$ . This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

#### 9.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

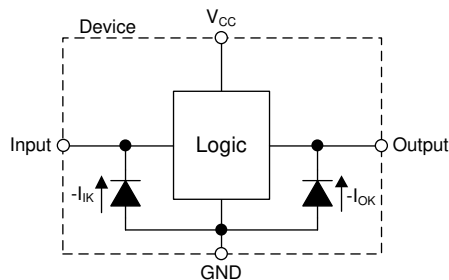
Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors, however a 10-k $\Omega$  resistor is recommended and will typically meet all requirements.

#### 9.3.3 Clamp Diode Structure

The inputs and outputs to this device have negative clamping diodes only as depicted in [Figure 9-1](#).

#### CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**Figure 9-1. Electrical Placement of Clamping Diodes for Each Input and Output**

**9.3.4 Partial Power Down ( $I_{off}$ )**

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the  $I_{off}$  specification in the *Electrical Characteristics* table.

**9.4 Device Functional Modes**

Table 9-1 lists the functional modes of the SN74LVC2G08-Q1.

**Table 9-1. Function Table**

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

## 10 Application and Implementation

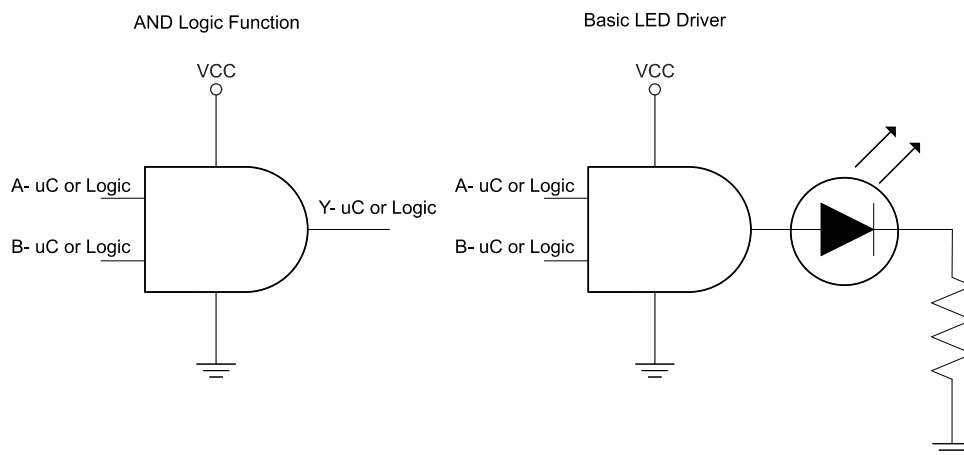
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The SN74LVC2G08-Q1 is a high-drive CMOS device that can be used for implementing AND logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V, making it ideal for driving multiple outputs and good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate down to  $V_{CC}$ .

### 10.2 Typical Application



**Figure 10-1. Typical Application**

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

##### 10.2.1.1 Detailed Design Procedure

#### 1. Recommended Input Conditions

- Rise time and fall time specs. See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
- Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as ( $V_I$  maximum) in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .

#### 2. Recommended Output Conditions

- Load currents must not exceed ( $I_O$  maximum) per output and must not exceed total current (continuous current through  $V_{CC}$  or GND) for the part. These limits are located in the [Recommended Operating Conditions](#) table.
- Outputs must not be pulled above  $V_{CC}$  in normal operating conditions.

## 11 Application Curves

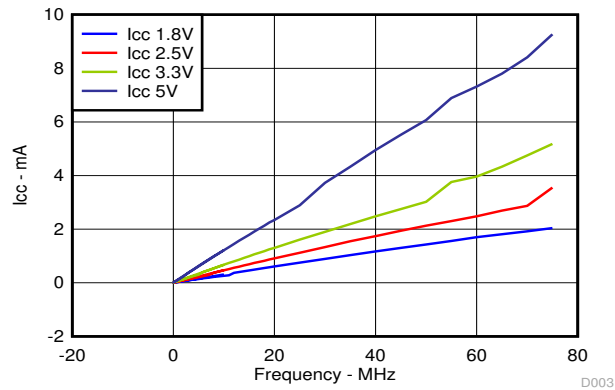


Figure 11-1. I<sub>CC</sub> vs Frequency

## 12 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table. Each V<sub>CC</sub> pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F capacitor is recommended and if there are multiple V<sub>CC</sub> pins then 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results

## 13 Layout

### 13.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub> whichever make more sense or is more convenient.

### 13.2 Layout Example

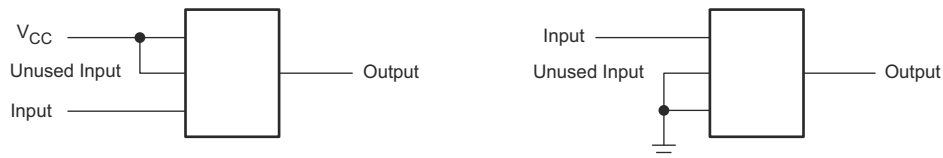


Figure 13-1. Layout Example

## 14 Device and Documentation Support

### 14.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 14.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 14.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

### 14.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G08IDCTRQ1	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C08 Z	<a href="#">Samples</a>
SN74LVC2G08QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HLRQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC2G08-Q1 :**

- Catalog: [SN74LVC2G08](#)
- Enhanced Product: [SN74LVC2G08-EP](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

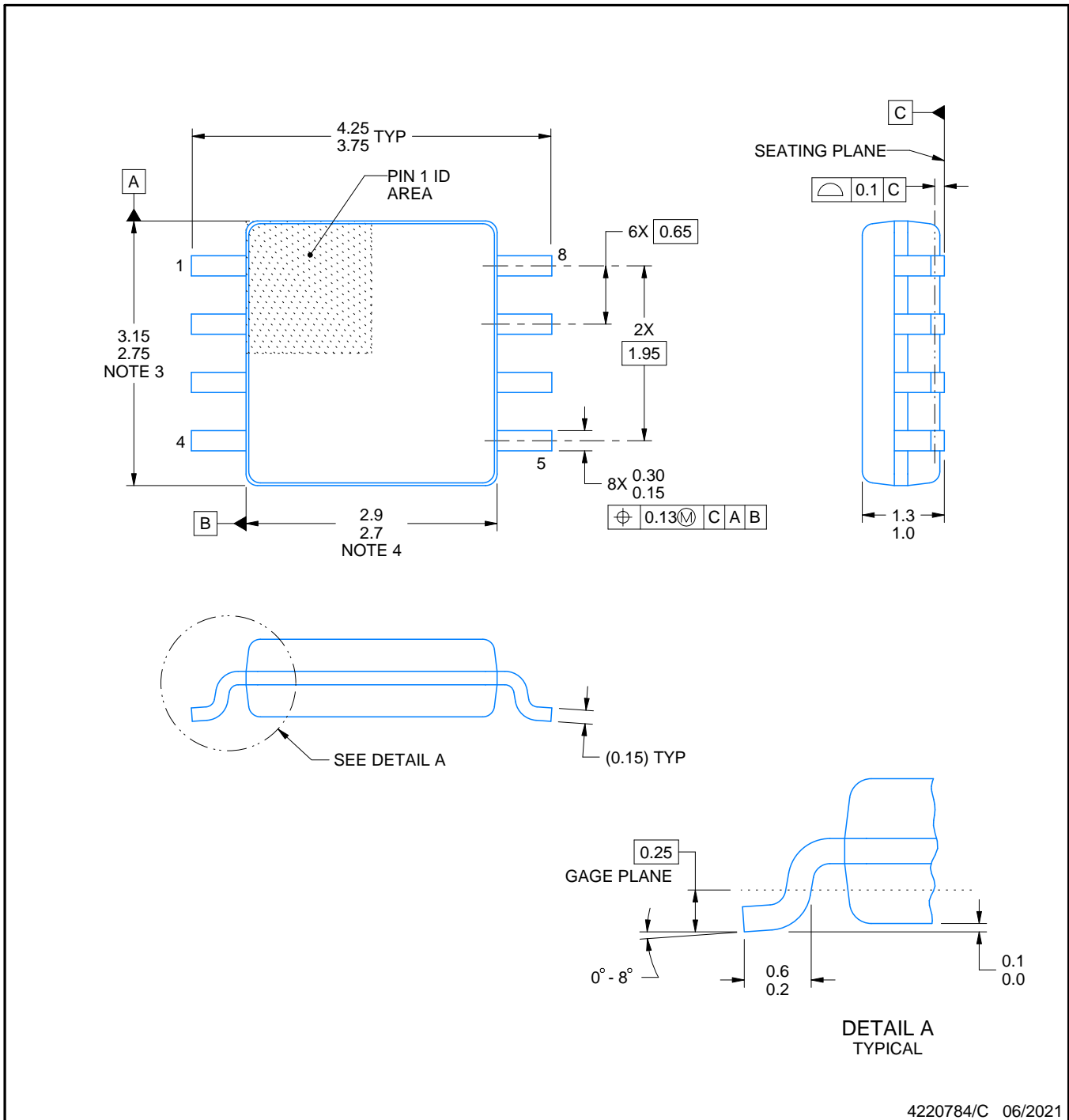
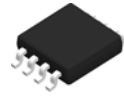
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G08QDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G08QDCURQ1	VSSOP	DCU	8	3000	183.0	183.0	20.0



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NOTES:

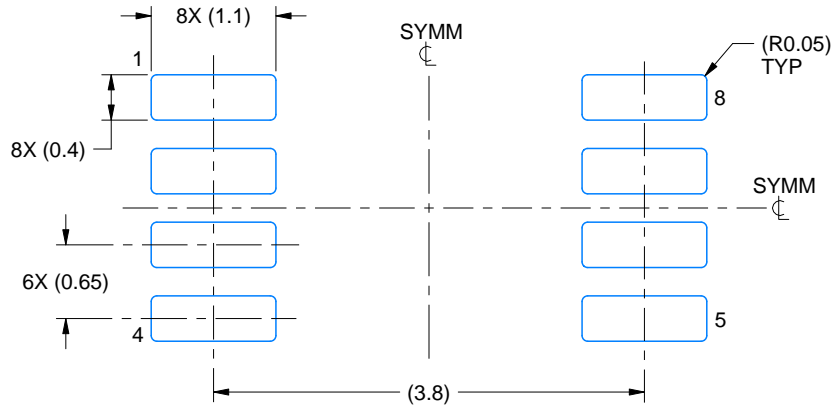
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

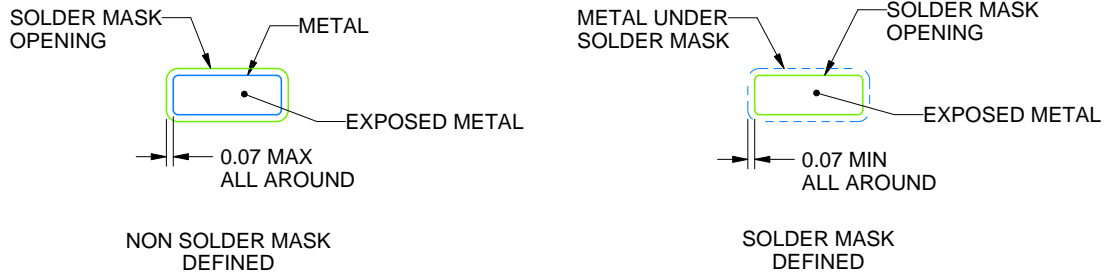
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

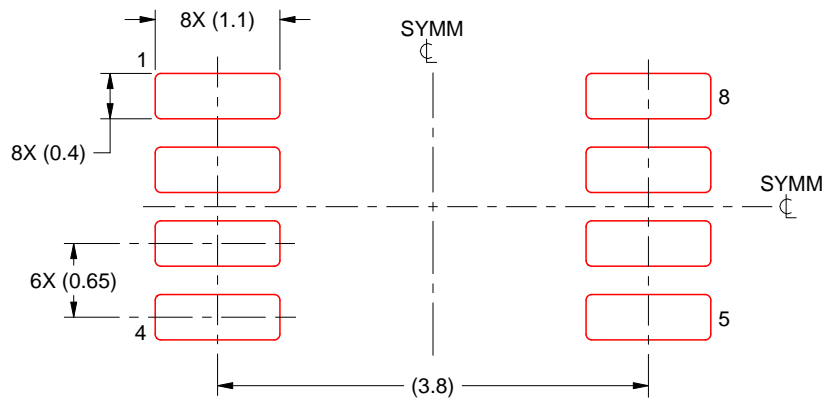
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

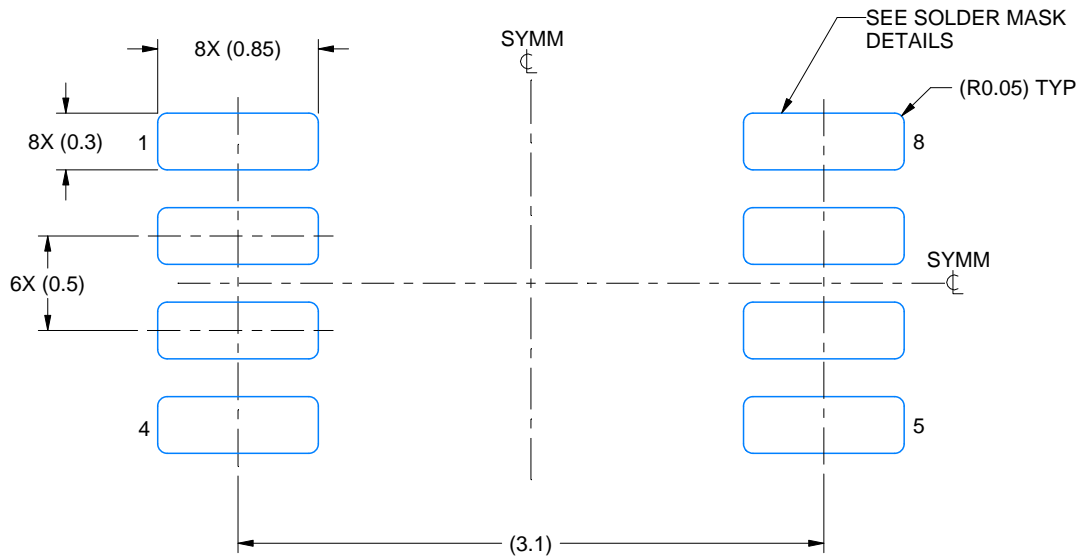


# EXAMPLE BOARD LAYOUT

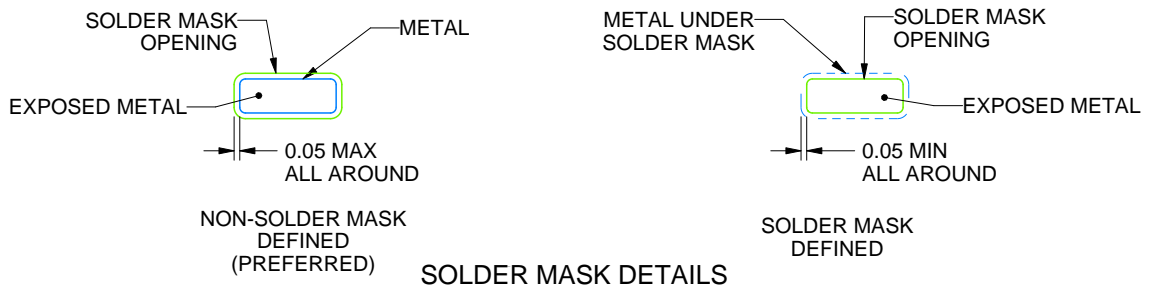
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

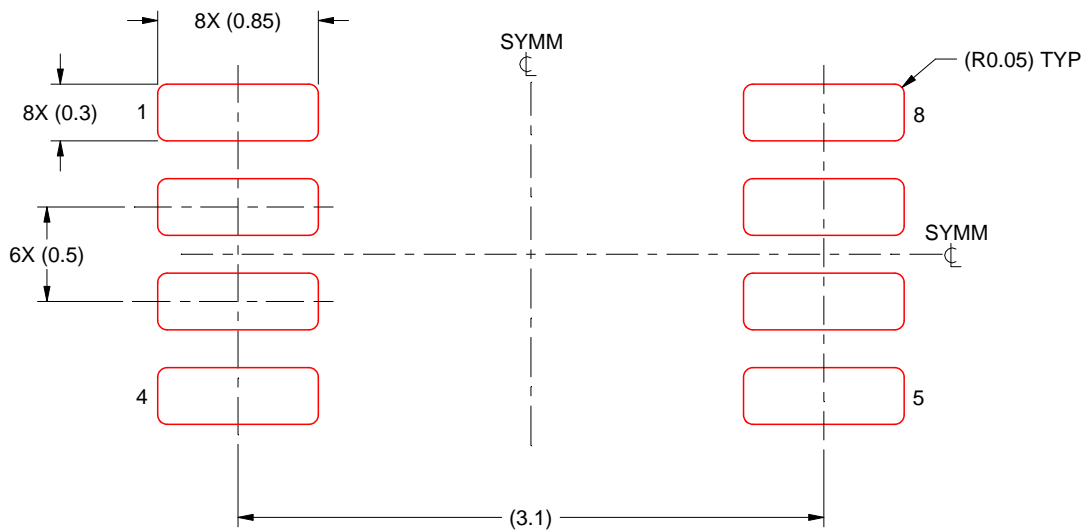
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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