

Notification Number:	20150901005	Notification Date:	12/03/2015
Title:	Datasheet update for SN65DSI85		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.

The product datasheet(s) is updated as seen in the change revision history below:



SN65DSI85

SLLSEB9E – SEPTEMBER 2012 – REVISED AUGUST 2015

www.ti.com

Changes from Revision D (September 2013) to Revision E

Page

• Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
• Changed Figure 4, note 2 for clarification.	11
• Changed item 3 of the ULPS sequence list for clarification.	13
• Changed description of the Init seq7 - Recommended Initialization Sequence for clarification.	16
• Changed description of Address 0x0A, Bit 7 in Table 8, CSR Bit Field Definitions - Reset and Clock Registers	24
• Changed Address 0x18, Bits 3 and 2 Description, Address 0x18, Bit 1 Description, and Address 0x18, Bit 0 Description in Table 10 for clarification.	27
• Changed Video STOP and Restart sequence, step 1 of the STOP sequence from "...0(CSR 0x0A.7)" to "...0(CSR 0x0D.0)" and step 3 of the Restart sequence from "Wait for the PLL_LOCK bit to be set(CSR 0x0A.7)." to "Wait for a minimum of 3 ms."	36

The datasheet number will be changing.

Device Family	Change From:	Change To:
SN65DSI85	SLLSEB9D	SLLSEB9E

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/sn65dsi85>

Reason for Change:

To more accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this Notification:

None.

Product Affected:

SN65DSI85ZQE	SN65DSI85ZQER
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For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com