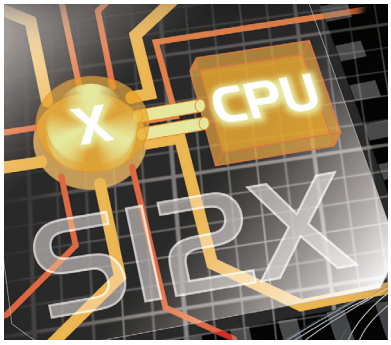
erformance 16-bit Microcontrollers

MC9S12XA512/256



Target Applications

> Industrial motor control

> Health care monitoring systems/ home health products

> Programmable logic controller

> Security-related applications and access control

> Factory automation

> HVAC/building control actuators and sensors

> Industrial control panels

16-bit Enhanced S12 CPU Core

> C-optimized CISC architecture produces extremely compact code

> Excellent 32-bit calculations and semaphore handling

> Access to large data segments independent of PPAGE

> Up to 40 MHz bus operation

> Opcode compatible with the 68HC11, 68HC12 and HCS12

> Industry-leading EMC performance

> 3V to 5.5V operation

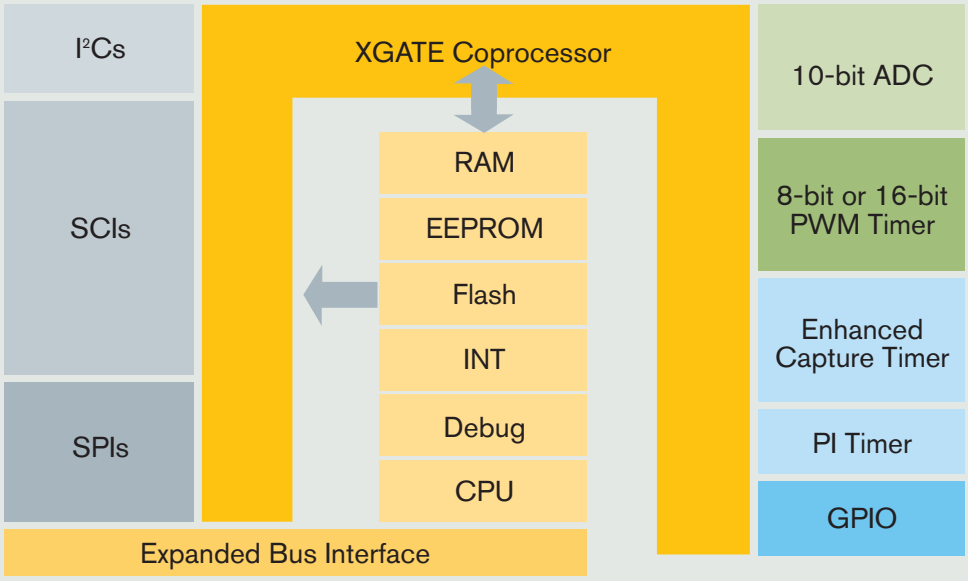
> Wide range of high-performance peripherals

Overview

Freescale Semiconductor's highly integrated MC9S12XA microcontroller family is one of the first families to use the high-performance 16-bit HCS12X core. The S12X family delivers 32-bit performance with all the advantages and efficiencies of a 16-bit MCU. Based on an enhanced HCS12 core, the S12XA family delivers two to five times the performance of a 25 MHz HCS12 while retaining code compatibility for easy migration. The family introduces the performance-boosting XGATE module, which off-loads the CPU by providing high-speed data processing and transfer between peripheral modules, RAM and I/O ports.

The family's core meets the robust requirements of the industrial markets by using Freescale's industry-leading, full automotive specification SG-Flash and further integrating static random access memory (SRAM) and electronically erasable programmable read-only memory (EEPROM) with multiple serial communication peripherals controllers, a range of timers, pulse-width modulation (PWM) channels, general I/O channels and an analog-to-digital converter (ADC). The family is available in a range of quad flat packs (QFP) and temperature variants allowing for flexibility in design.

MCS12XA FAMILY PRODUCT EXAMPLE



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XGATE Coprocessor

> Peripheral coprocessor performing complex DMA and data preprocessing features
> Easily programmable in C
> Up to 80 MHz operation
> Low level of interrupt loading on the main CPU
> Transfers data to or from peripherals, RAM and Flash without CPU intervention or CPU wait states
> Able to perform operations on data (logical, shifts, arithmetic, bit operations)

Memory

> Proven automotive Flash technology
  - 10K W/E cycles at 125°C
  - Ability to execute from one Flash block while programming/erasing another
  - No external high voltage or charge pump required
> 1 KB, 2 KB or 4 KB EEPROM
  - Minimum of 100K W/E cycles
> 4 KB, 8 KB, 12 KB, 16 KB, 20 KB or 32 KB RAM
> Security enhancement: option of locking BDM access to Flash and EEPROM
> Flash array usable for EE extension (virtual EEPROM implementation)

5V ADC Inputs and 5V I/O

Non-Multiplexed External Bus

> 23-bit address/16-bit data wide

System Integration Modules, Including Enhanced Interrupt Controller

> Windowed COP watchdog and clock monitor
> Seven levels of nested interrupt

Up to Six Serial Communications Interfaces with Hardware LIN Support

Up to Three Serial Peripheral Interfaces

Up to Two Inter-Integrated Circuit (I^2C) Interfaces

10-bit ADC

> One 8-channel and one 16-channel
> External/internal conversion trigger capability
> 7 µs, 10-bit single conversion time

Real-Time Interrupt

Enhanced Capture Timer

> Excellent 1–256 prescaler
> Eight programmable 16-bit input capture or output compare channels
> Four 8-bit or two 16-bit pulse accumulators
> Four buffered input capture channels
> 16-bit modulus down-counter

Clock Generation Module

> Phase-Lock Loop (PLL) clock frequency multiplier/divider
> Clock monitor
> Low-power Pierce oscillator using a 0.5 MHz to 16 MHz crystal or full-drive Pierce 0.5 MHz to 40 MHz crystal oscillator reference clock

Periodic Interrupt Timer

> Four 16-bit internal counters
> Two independent 8-bit prescalers

PWM Channels

> Independent period and duty cycle center-aligned outputs for motor control
> 8-bit, 8-channel; or 16-bit, 4-channel

Up to 119 Input/Output (I/O) Lines

> Programmable pull-ups/pull-downs
> Dual drive capability for EMC-optimized design

Development Support/ On-Chip Debug Interface

> Single-wire background debug mode (BDM) for debugging both S12X CPU and XGATE simultaneously while running at full speed
> On-chip hardware breakpoints with no limitation on memory address
> Read/write memory and registers while running at full speed

*C -40°C to +85°C
V -40°C to +105°C

MC9S12XA512/256 PART NUMBERS

Flash	RAM	E2	Device	XGATE	Speed	CAN	SCI	SPI	I^2C	ADC (10-bit)	PWM (8-bit)	Enhanced Capture Timer (16-bit)	Periodic Interrupt Timer (24-bit)	I/O	Package	Temp.
512 KB	32 KB	4 KB	MC9S12XA512	Yes	40 MHz	–	2	2	1	1 x 8 ch.	7	1 x 8 ch.	4	59	80 QFP (FU)	C/V*
	32 KB	4 KB	MC9S12XA512	Yes	40 MHz	–	4	3	1	2 x 8 ch.	8	1 x 8 ch.	4	91	112 LQFP (PV)	C/V*
	32 KB	4 KB	MC9S12XA512	Yes	40 MHz	–	6	3	1	1 x 8 ch., 1 x 16 ch.	8	1 x 8 ch.	4	119	144 LQFP (FV)	C/V*
256 KB	16 KB	4 KB	MC9S12XA256	Yes	40 MHz	–	2	2	1	1 x 8 ch.	7	1 x 8 ch.	4	59	80 QFP (FU)	C/V*
	16 KB	4 KB	MC9S12XA256	Yes	40 MHz	–	4	3	1	2 x 8 ch.	8	1 x 8 ch.	4	91	112 LQFP (PV)	C/V*
	16 KB	4 KB	MC9S12XA256	Yes	40 MHz	–	4	3	1	1 x 8 ch., 1 x 16 ch.	8	1 x 8 ch.	4	119	144 LQFP (FV)	C/V*

Application Notes

AN2615	HCS12 and S12X Family Compatibility
AN2685	How to Configure and Use the XGATE on S12X Devices
AN2708	An Introduction to the External Bus Interface on the HCS12X
AN2724	Using the HCS12X PIT as a 24-bit Elapsed Timer
AN2732	Using XGATE to Implement LIN Communication on HCS12X
AN2734	HCS12X Family Memory Organization

Product Documentation

Product Brief	9S12XAFAMPP
User Manual	9S12XAP512DGV2

Learn More: For more information about Freescale's MCS12X Family, please visit **www.freescale.com/S12X**.

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