

CWDM305PD**SURFACE MOUNT SILICON
DUAL P-CHANNEL
ENHANCEMENT-MODE
MOSFET****SOIC-8 CASE**www.centrasemi.com**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CWDM305PD is a dual high current P-channel enhancement-mode silicon MOSFET manufactured by the P-channel DMOS process, and is designed for high speed pulsed amplifier and driver applications. This MOSFET offers high current, low $r_{DS(ON)}$, low threshold voltage, and low gate charge.

MARKING CODE: C503**APPLICATIONS:**

- Load/Power switches
- Power supply converter circuits
- Battery powered portable equipment

FEATURES:

- Low $r_{DS(ON)}$ (83m Ω MAX @ $V_{GS}=5.0V$)
- High current ($I_D=5.3A$)

MAXIMUM RATINGS: ($T_A=25^\circ C$)

Drain-Source Voltage
Gate-Source Voltage
Continuous Drain Current (Steady State)
Maximum Pulsed Drain Current, $t_p=10\mu s$
Power Dissipation
Operating and Storage Junction Temperature
Thermal Resistance

SYMBOL		UNITS
V_{DS}	30	V
V_{GS}	16	V
I_D	5.3	A
I_{DM}	21.2	A
P_D	2.0	W
T_J, T_{stg}	-55 to +150	$^\circ C$
θ_{JA}	62.5	$^\circ C/W$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^\circ C$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=20V, V_{DS}=0$			100	nA
I_{DSS}	$V_{DS}=30V, V_{GS}=0$			1.0	μA
BV_{DSS}	$V_{GS}=0, I_D=250\mu A$	30			V
$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0		3.0	V
$r_{DS(ON)}$	$V_{GS}=10V, I_D=2.7A$		0.066	0.072	Ω
$r_{DS(ON)}$	$V_{GS}=5.0V, I_D=2.7A$		0.077	0.083	Ω
g_{FS}	$V_{DS}=5.0V, I_D=5.3A$		11		S
C_{rss}	$V_{DS}=10V, V_{GS}=0, f=1.0MHz$		50	60	pF
C_{iss}	$V_{DS}=10V, V_{GS}=0, f=1.0MHz$		500	590	pF
C_{oss}	$V_{DS}=10V, V_{GS}=0, f=1.0MHz$		60	150	pF
$Q_{g(tot)}$	$V_{DD}=15V, V_{GS}=5.0V, I_D=5.3A$		4.7	7.0	nC
Q_{gs}	$V_{DD}=15V, V_{GS}=5.0V, I_D=5.3A$		1.4	2.1	nC
Q_{gd}	$V_{DD}=15V, V_{GS}=5.0V, I_D=5.3A$		1.7	2.5	nC
t_{on}	$V_{DD}=15V, I_D=5.3A, R_G=10\Omega$		7.0		ns
t_{off}	$V_{DD}=15V, I_D=5.3A, R_G=10\Omega$		8.0		ns

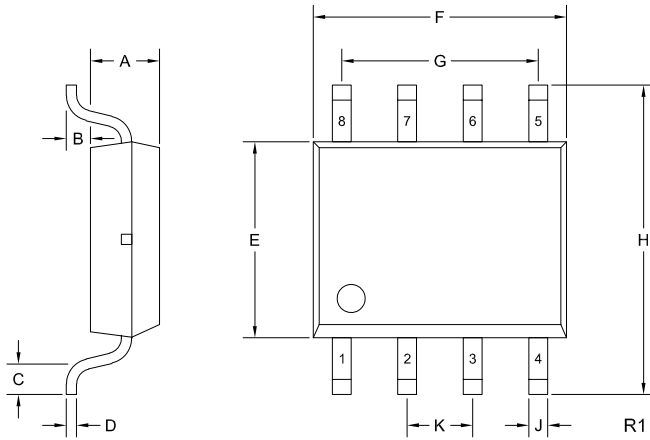
R3 (10-August 2018)

CWDM305PD

**SURFACE MOUNT SILICON
DUAL P-CHANNEL
ENHANCEMENT-MODE
MOSFET**



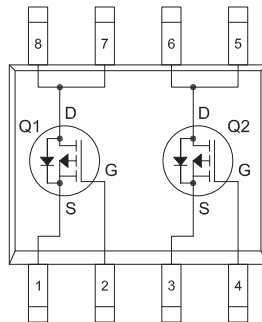
SOIC-8 CASE - MECHANICAL OUTLINE



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.061	1.392	1.554
B	0.004	0.009	0.100	0.224
C	0.016	0.035	0.40	0.90
D	0.007	0.010	0.19	0.25
E	0.145	0.157	3.80	4.00
F	0.189	0.198	4.80	5.00
G	0.150		3.81	
H	0.228	0.244	5.80	6.20
J	0.013	0.020	0.33	0.51
K	0.050		1.27	

SOIC-8 (REV: R1)

PIN CONFIGURATION



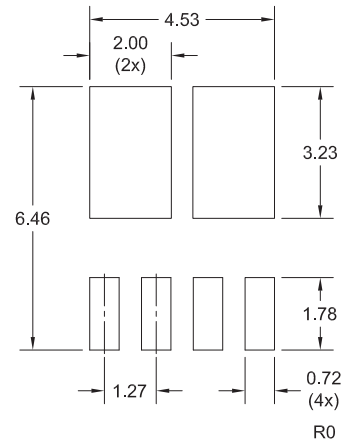
LEAD CODE:

- 1) Source Q1 5) Drain Q2
- 2) Gate Q1 6) Drain Q2
- 3) Source Q2 7) Drain Q1
- 4) Gate Q2 8) Drain Q1

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SUGGESTED MOUNTING PADS

(Dimensions in mm)



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OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

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