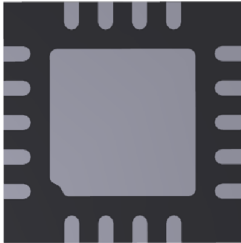


USB Type-C™ protection for source application



QFN-18L 3.5 x 3.5 x 0.55 mm

Product labels



Product status link

[TCPP02-M18](#)

Expansion board

[X-NUCLEO-SRC1M1](#)

Software example code

[X-CUBE-TCPP](#)

I2C address

0110 10x (LSB = 'x')

ST reference design

[STEVAL-2STPD01](#)

Features

- Externally programmable VBUS over current protection (OCP)
- Integrated charge pump and gate driver for external N-channel MOSFET
- VBUS current sense and amplifier with analog output
- Integrated discharge on VBUS and VCONN
- Over temperature protection
- Over voltage protection (OVP) on CC lines against short-to-V_{BUS}
- V_{CONN} OCP (100 mW max), OVP (6 V max)
- ESD protection for CC1, CC2, compliant with IEC 61000-4-2 Level 4 (±8 kV contact discharge, ±15 kV air discharge)
- Compliant with PPS (programmable power supply)
- I²C communication, with two I²C addresses available
- Junction temperature from -40 °C to 125 °C
- Compliant with USB-C power delivery standard 3.1, standard power range (SPR), up to 100 W
- ECOPACK2 compliant

Applications

- USB-C chargers, adapters, power sharing adapters, battery charger
- Wall plugs, car charger, PoE to USB-C adapter, power bank
- Desktop, monitor, docking, USB hub, dual-port charger

Description

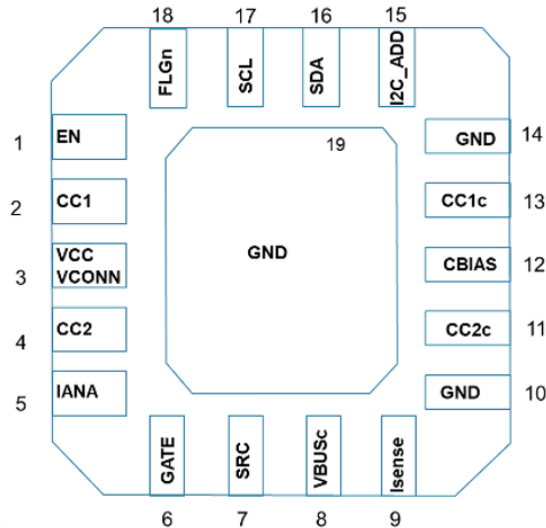
The **TCPP02-M18** is a MCU companion chip enabling cost-effective USB-C source solution. It provides protections and functionalities to safely comply with the USB-C specification.

On provider path, **TCPP02-M18** drives external N-channel MOSFET to ensure overcurrent protection on VBUS pin, as well as a discharge path. It features an analog current sense and amplifier with an output accessible for a MCU ADC, thus minimizing system cost.

The **TCPP02-M18** features 24 V tolerant ESD protection as per IEC61000-4-2 level 4 on USB Type-C™ connector communication channel pins (CC). Also, it provides overvoltage protection on CC1 and CC2 pins when these pins are subjected to short circuit with the VBUS pin that may happen when removing the USB Type-C™ cable from its receptacle.

TCPP02-M18 embeds I2C slave registers with two possible addresses, ideal for dual-port chargers or multiple port applications.

1 Pinout and functions

Figure 1. QFN-18L 3.5 x 3.5 x 0.55 mm (top view)

Table 1. Pinout and functions

Name	Pin #	Type	Description
EN	1	Input	Enable pin.
CC1	2	Input / Output	Configuration channel 1 pin on USB-C controller side.
VCC_VCONN	3	Power	Power supply for V _{CONN} power pin. Connect to 3.3 V or 5.5 V.
CC2	4	Input / Output	Configuration channel 2 pin on USB-C controller side.
I _{ANA}	5	Output	V _{BUS} current analog measurement.
GATE	6	Output	Gate driver provider: gate pin of external N-channel MOSFET.
SRC	7	Input	Gate driver provider: source pin of external N-channel MOSFET.
VBUS _c	8	Input	VBUS connector side.
I _{sense}	9	Input	VBUS current measurement.
GND	10	GND	Ground.
CC2 _c	11	Input / Output	Configuration channel 2 pin on USB-C connector side.
C _{BIAS}	12	Output	ESD capacitor.
CC1 _c	13	Input / Output	Configuration channel 1 pin on USB-C connector side.
GND	14	GND	Ground.
I2C_ADD	15	Input	Least significant bit on I2C address. Connected to GND or 1.8 V / 3.3 V.
SDA	16	Input / Output	Serial data line on I2C bus.
SCL	17	Input / Output	Serial clock line on I2C bus.
FLGn	18	Output	Open-drain output flag (active low). Floating when not connected.
GND	EP	GND	Ground exposed pad.

2 Block diagram

Figure 2. TCPP02-M18 functional block diagram

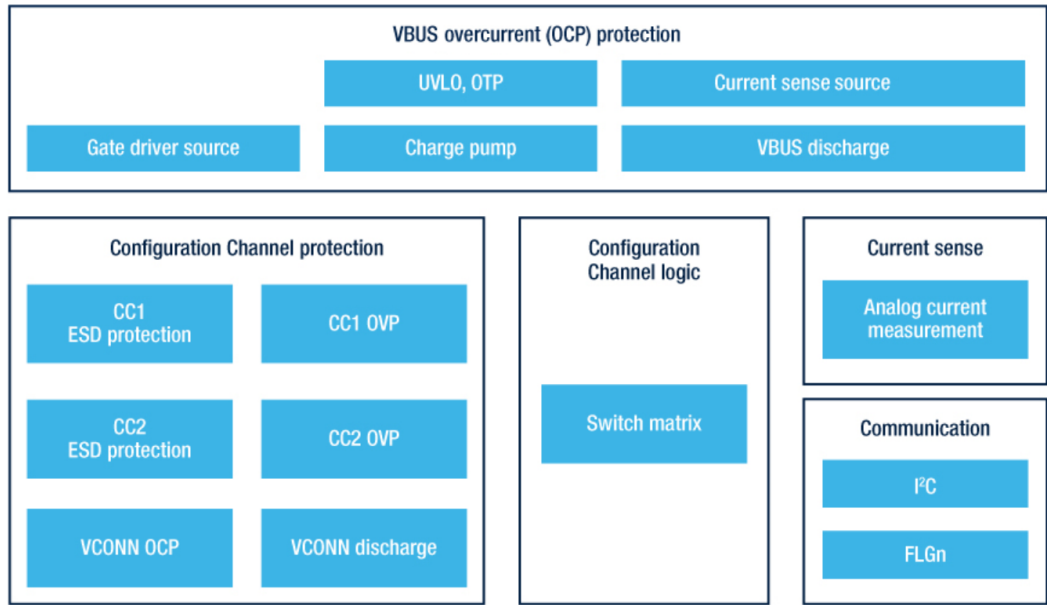
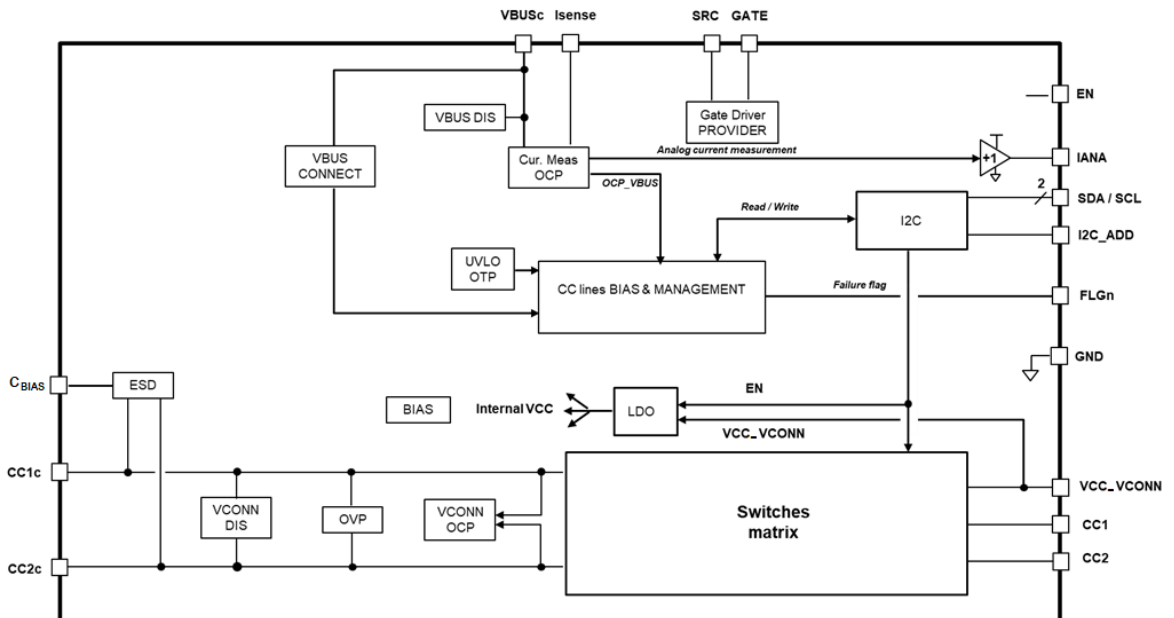
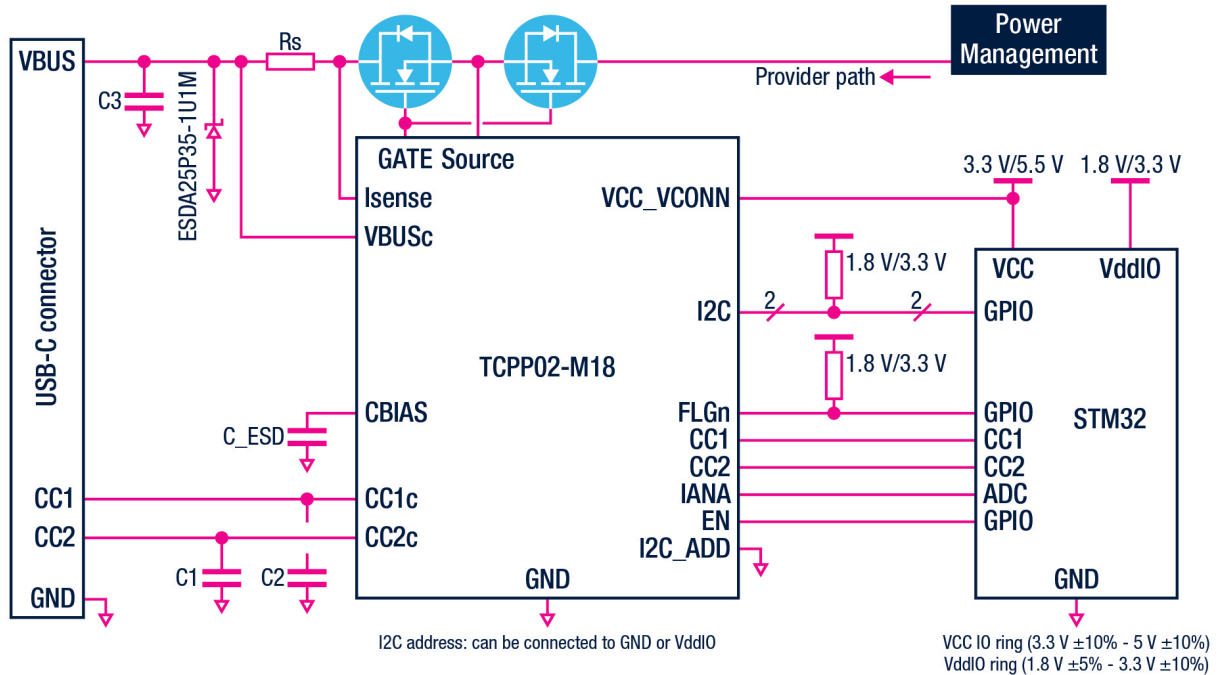


Figure 3. Internal block diagram



3 Typical USB-C source application block diagram

Figure 4. Typical application example



Please refer to [X-NUCLEO-SRC1M1](#) documentation ([databrief](#), [quick start guide](#), [user manual](#), [schematic](#) and [BOM](#)) for detailed application usage of TCPP02-M18 and selection of external components.

External components are described in External components description.

Please refer to [TA0357](#) for an overview of USB Type-C™ and power delivery technologies.

Please refer to [AN5225](#) for more informations related to USB Type-C™ power delivery using STM32xx Series MCUs and STM32xxx series MPUs.

For more information on EMI filtering and ESD protection of USB datalines, please refer to [AN4871](#): USB Type-C™ protection and filtering.

4 Electrical specification

4.1 Parameter conditions

Unless otherwise specified:

- All voltages are referenced to GND
- The minimum and maximum values are guaranteed in the worst conditions of operating temperature, supply voltage and frequencies, by tests in production on 100 % of the devices
- Typical values are given only as design guidelines and are not tested

4.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in the tables below, may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings (across junction temperature range)

Symbol	Parameter	Pin name	Value	Unit
V _{POWER}	Voltage for power pins	VCC_VCONN	7	V _{DC}
V _{IN}	Voltage for input pins	EN, I2C_ADD	7	V _{DC}
		VBUSc, I _{sense} , SRC	24	
V _{OUT}	Voltage for output pins	I _{ANA} , FLGn	7	V _{DC}
		C _{BIAS} , GATE	24	
V _{I/O}	Voltage for input, output pins	SDA,SCL, CC1,CC2	7	V _{DC}
		CC1c,CC2c	24	
R _{thj-a}	Junction to ambient thermal resistance		150	°C/W
T _J	Junction temperature range		-40 to +125	°C
T _{STG}	Storage temperature range		-55 to +150	°C

Table 3. ESD ratings (across junction temperature range)

Symbol	Description	Pins	Value	Unit
V _{ESD_c}	System level ESD robustness on USB Type-C™ connector side ⁽¹⁾			
	IEC61000-4-2 Level 4, contact discharge	CC1c, CC2c	8	kV
	IEC61000-4-2 Level 4, air discharge		15	
V _{HBM}	V _{ESD} ratings human body model (JESD22-A114D, level 2)	All pins	2	kV

1. Internal ESD protection functionality is associated with external capacitor connected on pin C_{BIAS}.

Note: for more information on IEC61000-4-2 standard testing, please refer to AN3353.

4.3 Recommended operating conditions

Table 4. Recommended operating condition, across junction temperature range

Pin name	Min.	Typ.	Max.	Unit
VCC_VCONN, CC1, CC2	2.7		5.5	V
EN, I _{ANA} , I2C_ADD, SDA, SCL, FLGn	1.7		3.6	V

Pin name	Min.	Typ.	Max.	Unit
CC1c, CC2c, VBUSc, I _{SENSE} , SRC	0		22	V

4.4 Power supply (VCC_VCONN, VBUSc)

Table 5. Electrical characteristics – Power supply (VCC_VCONN, VBUSc) across T_j

Symbol	Parameter	Test condition across T _{OP}	Value			Unit
			Min.	Typ.	Max.	
ICC_VCONN	V _{CC} supply current	Normal mode			2.7	mA
		Low power mode			1	μA
I _{enable}	Supply current of EN pin	Low power mode 1.7 V - 2.7 V			3	μA
		Low power mode 2.7 V - 3.6 V			10	μA
T _{DIS_VBUSc}	VBUSc discharge time ⁽¹⁾				220	ms

1. Equivalent discharge resistor is 2.5 kΩ typical.

4.5 VBUS OCP

Table 6. Electrical characteristics for V_{BUS} (OCP, gate driver, current monitoring) across T_j

Symbol	Parameter	Test condition across T _{OP}	Value			Unit
			Min.	Typ.	Max.	
V _{GS}	Gate to source voltage consumer VBUSc = 5 V - 20 V		4.5	5	5.5	V
V _{TH_OCP_VBUS}	VBUS OCP threshold voltage	Across sense resistor R _s	35	42	45	mV
T _{OFF_OCP_VBUS}	VBUS OCP response time			3	8	μs
I _{ana_gain}	Current sensing gain		39	42	45	V/V
V _{IANA}	IANA pin typical voltage during OCP event on VBUS line			1.7	1.95	V
T _{ON}	VBUS turn-on time			1	3	ms

4.6 CC lines OVP and ESD

Table 7. Electrical characteristics: CC lines OVP (CC refers to CC1 and CC2) across T_j

Symbol	Parameter	Test condition across T _{OP}	Value			Unit
			Min.	Typ.	Max.	
R _{ON_CC}	ON resistance of CC OVP FET	Normal mode		0.7	1.5	Ω
		Low power mode	8	17	28	
C _{ON_CC}	Equivalent ON capacitance of CCx line in normal mode	0 - 1.2 V, f = 400 kHz	40	60	100	pF
V _{TH_CC}	CC OVP threshold voltage		5.5	5.75	6	V
T _{OVP_CC}	OVP response time on the CC pins			60	100	ns
BW _{CCx}	Bandwidth on CCx pins	at -3dB and 0 - 1.2 V		10		MHz

4.7 VCONN OCP, discharge

Table 8. Electrical characteristics V_{CONN} switch (OCP, discharge) across T_j

Symbol	Parameter	Test condition across T _{OP}	Value			Unit
			Min.	Typ.	Max.	
R _{ON_VCONN}	ON resistance of VCONN FET		2.1	3	5.5	Ω
I _{VCONN}	Current thru V _{CONN} FET max operating current	VCONN = 3.0 V - 5.5 V			40	mA
R _{dis-vconn}	V _{CONN} discharge resistor		2.5	4	5	kΩ
OCP _{TH_VCONN}	OCP threshold on V _{CONN}		40	47	55	mA
T _{OCP_VCONN}	V _{CONN} OCP response time			0.9	2	μs

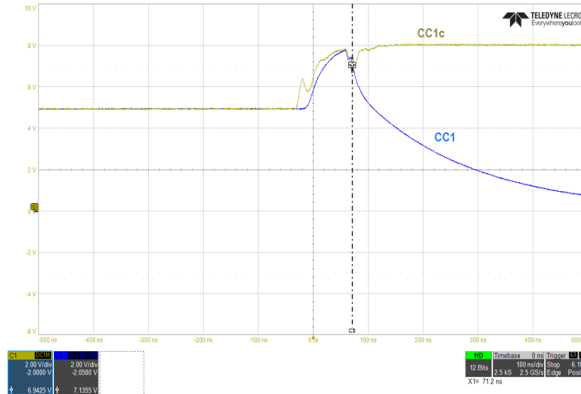
4.8 I2C slave

Table 9. Electrical characteristics I2C addressing across T_j

Symbol	Parameter	Test condition across T _{OP}	Value			Unit
			Min.	Typ.	Max.	
I2C speed					1	Mbps

5 Typical electrical characteristics curves

Figure 5. CC line (CC1 or CC2) OVP response time



Note: Test conditions for Figure 5: TCPP02-M18 in normal mode $VCC_VCONN = +5\text{ V}$, $ENABLE = 3.3\text{ V}$, $VBUS = 0\text{ V}$.

6 Functional description

6.1 Overview

The TCPP02-M18 is a cost effective solution to protect microcontrollers featuring built-in USB-C power delivery (UCPD) controller or other low voltage power delivery controller.

Please refer to [TA0357](#) for an overview of USB Type-C™ and power delivery technologies.

Please refer to [AN5225](#) for more informations related to USB Type-C™ power delivery using STM32xx Series MCUs and STM32xxx series MPUs.

6.2 Power modes

The TCPP02-M18 embeds three distinct power modes controlled by the UCPD controller via the I2C bus.

Figure 6. Power modes process

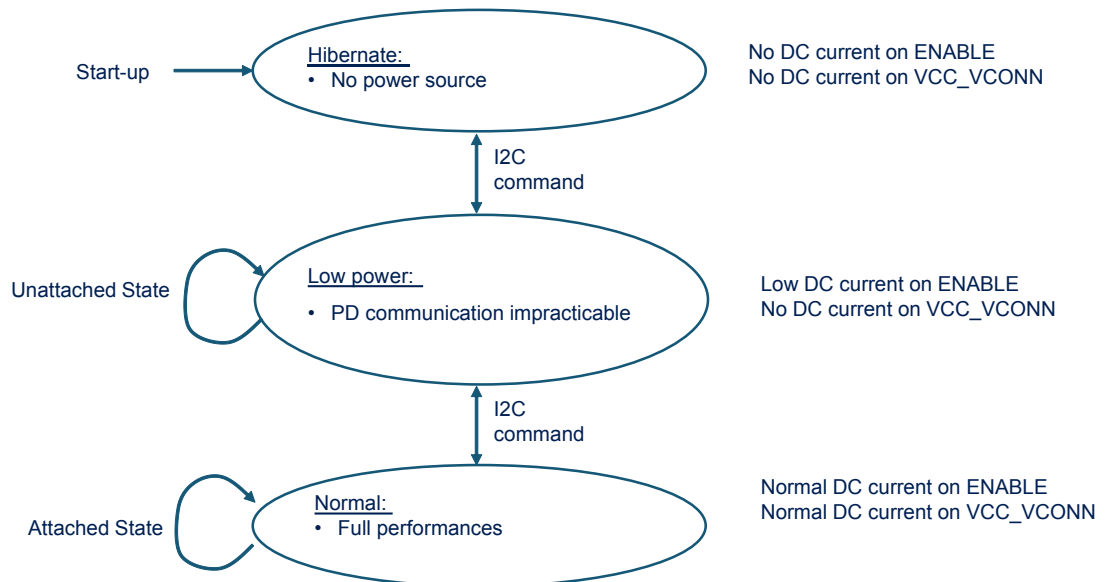


Table 10. Power mode versus power supply

VCC_VCONN	ENABLE	I _{DC} VCC_VCONN	I _{DC} ENABLE	Mode	Comments
X	0 V	0 μA ⁽²⁾	0 μA ⁽¹⁾⁽²⁾	OFF (reset)	Gate driver OFF / CC switches OFF FLGn inactive I2C inactive / I2C registers reset
X	1.8 V ±5% 3.3 V ±10%	0 μA ⁽²⁾	0 μA ⁽¹⁾⁽²⁾	Hibernate	I2C active <u>Default state at start-up</u>
X	1.8 V ±5% 3.3 V ±10%	0 μA ⁽²⁾	< 10 μA ⁽¹⁾⁽²⁾ ₍₃₎	Low power	High ohmic CC => PD communication not possible OVP protection by clamping I2C active
3.3 V ±10% 5 V ±10%	1.8 V ±5% 3.3 V ±10%	2.7 mA	< 30 μA ⁽¹⁾⁽²⁾	Normal	Full performance mode I2C active FLGn indicates failures

1. Dynamic current of I2C interface have to be added to the values indicated when the I2C bus is used.
2. ESD leakage current have to be added to the values indicated.
3. For pin EN voltage between 1.7 V and 3.6 V.

Table 11. TCPP02-M18 states versus power modes

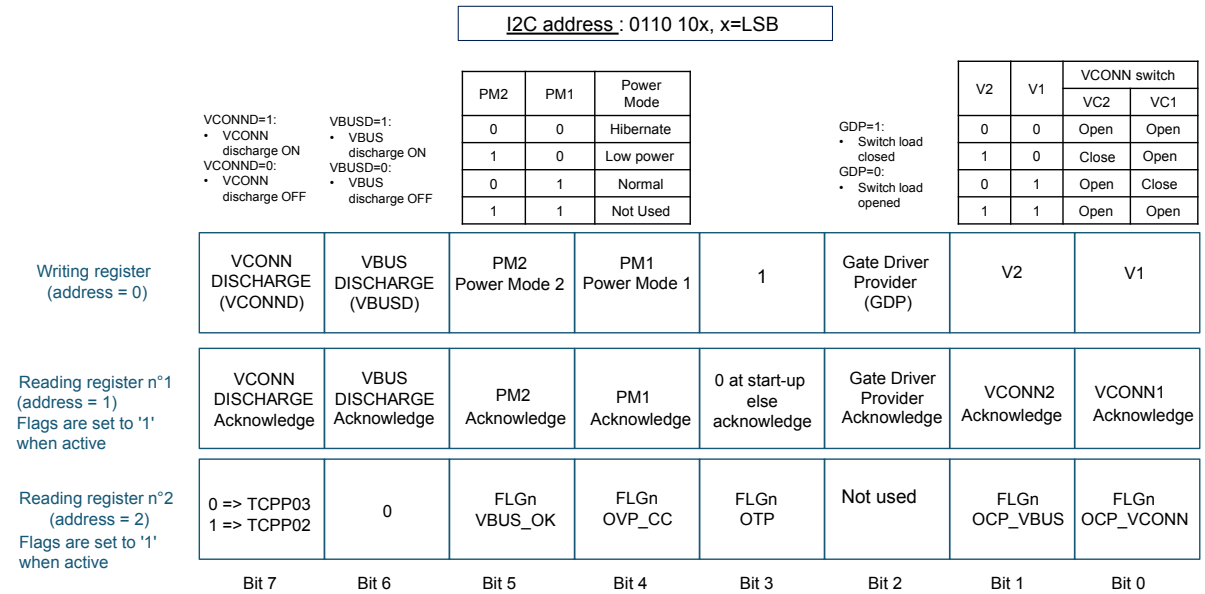
Power mode	CC switches	OVP CC	Gate driver provider	FLGn	I2C	I _{ANA}	OCP VBUS	V _{CONN} VBUS Dis.	Comment
OFF	OFF	NA	OFF	VBUS connect	OFF	OFF	OFF	OFF	TCPP not powered
Hibernate	OFF	NA	OFF	VBUS connect	ON	OFF	OFF	OFF	Default state at start-up
Low power	High ohmic	5 V clamp	OFF	VBUS connect	ON	OFF	OFF	OFF	Signaling only
Normal	Full perf.	Active OVP	Controlled by I2C	Failure flags	ON	ON	ON	Controlled by I2C	PD communication active

6.3 I2C registers

The I2C address used by TCPP02-M18 is 0110 10x, with LSB = 'x'.

The LSB bit of the I2C address is set when connecting TCPP02-M18 pin I2C_ADD to GND (for LSB = '0') or to 1.8 V or 3.3 V (for LSB = '1').

Figure 7. I2C registers



7 Protection features

TCPP02-M18 embeds protection features for source applications, as required by:

- USB-C specification
- USB power delivery specification 3.1
- International electrotechnical commission (IEC)

7.1 FLGn pin description

FLGn pin is an open-drain output flag in steady state, it must be left floating when not connected.

In normal mode, FLGn indicates an error (OVP, OCP or OTP): I2C registers must be read to identify the error. Recovery for each error type is described in each section of below paragraphs.

7.2 How to protect against ESD (electrostatic discharge) applied on the USB Type-C™ connector?

Electrostatic discharges can be conducted by the USB Type-C™ connector and damage the electronic circuitry of the application.

The international electrotechnical commission modelize the ESD surge waveform in the specification [IEC61000-4-2](#).

The **TCPP02-M18** integrates ESD protection for CC1 and CC2 lines up to +8 kV contact discharge, associated with an external 100 nF - 50 V capacitor on C_{BIAS} pin.

Please refer to [AN4871](#) USB Type-C™ protection and filtering to apply a required protection to comply with the [IEC61000-4-2](#) specification.

For more information on IEC61000-4-2 standard testing, please refer to the STMicroelectronics application note [AN3353](#).

7.3 VBUS management

Until now, it was common to find the protection circuit inside a controller dedicated to USB-C power delivery. However, by supporting USB-C PD with an embedded module inside an MCU and a companion Type-C port protection device, you can lower your bill of material and facilitate the transition, without requiring an expensive USB-C PD ASIC controller. One of the reasons the MCU and **TCPP02-M18** bundle is such a compelling financial proposition is that the latter device integrates the VBUS gate drivers, which enables the use of cheaper and smaller N-MOSFETs, instead of the P-MOSFETs usually used by ASIC controllers.

7.4 VBUS current sense (I_{ANA} pin)

The I_{ANA} output pin is active only in normal mode.

The I_{ANA} output can be connected directly to the STM32 ADC input because it is internally biased by EN pin.

The I_{ANA} output voltage level is about 1.7 V at the OCP tripping level allowing connection to 1.8 V MCU I/O pin.

7.5 V_{BUS} analog current measurement and OCP

VBUS OCP threshold is set by external serial resistor on VBUS. The gain for the analog reading is set to 42 V/V. The OCP threshold is set to 0.042 V across R_s.

The OCP VBUS is biased by VCC_VCONN and works only in normal mode.

Equivalent block diagram in TCP02-M18 for V_{BUS} analog current measurement and OCP is given here after:

Figure 8. Equivalent block diagram in TCP02-M18

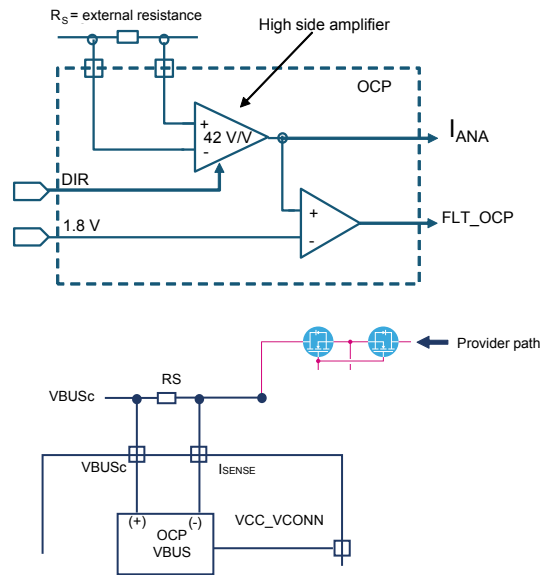


Table 12. Recommended values

Typical current	VBUS OCP threshold	R _s - Sense resistor (normalized values)
0.5 A	0.9 A	47 mΩ
1.5 A	1.9 A	22 mΩ
3.0 A	4.2 A	10 mΩ
5.0 A	6.0 A	7 mΩ

The OCP is biased continuously: inrush current magnitude is controlled by the user through an external capacitor. Please refer to the X-NUCLEO-SRC1M1 user manual for more informations on external capacitor to control the inrush current magnitude.

If an OCP event occurs:

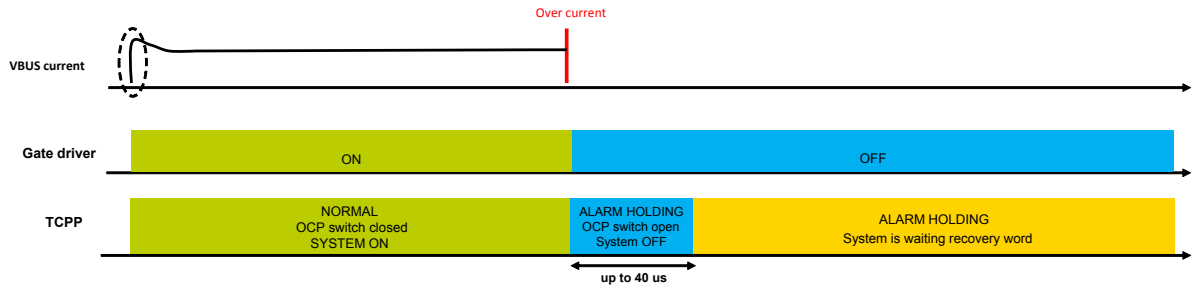
- V_{CONN} switches, CC switches and gate drivers are shutting down
- During up to 40 μs typ., this OCP alarm is held (no recovery is possible)
- After this delay, CC switches are turned ON but V_{CONN} switches and gate drivers are held OFF

The system can be restarted only with a recovery word send by the MCU via the I2C bus.

- The FLGn signal stays low while the recovery word has not been sent

The recovery word is described in next paragraph

Figure 9. Typical chronograms of TCPP02-M18 VBUS OCP



Note:

- In case of VBUS OCP event, the TCPP02-M18 switches OFF all active functions except CC switches:
 - V_{CONN} switches
 - VBUS gate driver
 - V_{CONN} and V_{BUS} discharge paths are activated
- It is signaled to the user by several ways:
 - I2C corresponding state bits are cleared (i.e. $V_{CONN1_ACK} = 0$, $V_{CONN2_ACK} = 0...$)
 - I2C relevant OCP flag is set ($FLGn_OCP_VBUS$ is the OCP event coming from VBUS switch for example)
 - Failure flag pin ($FLGn$) is active (i.e. in LowZ state)
- After a delay of up to 40 μs, to recover, the below bit sequence has to be written and after recovery, the user can resume a start-up procedure:

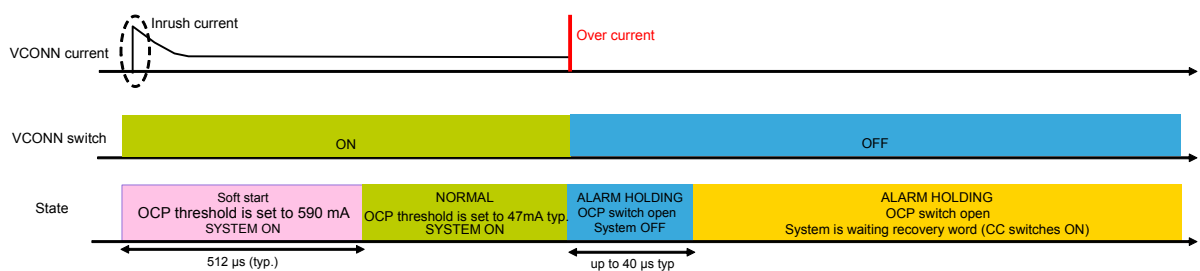
Table 13. VBUS OCP recovery bit sequence table

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	PM2	PM1	1	0	0	0

7.6 VCONN OCP

- At start-up, a soft start sets the tripping current to about 590 mA during 512 μ s min. (1ms max.)
- After this delay, the soft start is ended and the normal OCP threshold occurs (50 mA).
- If an OCP event occurs:
 - VCONN switches, CC switches and gate drivers are shutting down
 - During up to 40 μ s typical, this OCP alarm is held (no recovery is possible)
 - After this delay, CC switches are turned ON but VCONN switches and gate drivers are held OFF. The system can be restarted only with a recovery word send by the MCU via the I2C bus.
 - The FLGn signal stays low as long as the recovery word has not been sent

Figure 10. VCONN OCP chronograms



To recover, the below bit sequence has to be written and after recovery, the user can resume a start-up procedure:

Table 14. VBUS OCP recovery bit sequence table

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	PM2	PM1	1	0	0	0

7.7 VCONN CC line OVP

7.7.1 CC lines short to VBUS

USB Type-C™ standard specifies a pitch of 0.5 mm between connector pins (see figure 3-1 USB Type-C™ receptacle interface dimensions in [USB Type-C cable and connector specification](#)).

VBUS pin being adjacent to the CC pins, when removing the USB Type-C™ plug from the connector, VBUS can be shorted to CC lines and apply a voltage higher than specified for CC lines.

Over voltage protection is needed on the CC lines because VBUS typical voltage can be as high as 20 V when CC pins are usually 5 V tolerant I/Os on low voltage USB-PHY controllers.

TCPP02-M18 integrate this protection against CC lines short to VBUS thanks to an overvoltage protection (integrated FET).

When the voltage on the CC line goes above V_{TH_CC} , the OVP on CC line turns-on in less than 60ns (T_{OVP_CC} typical value) and FLGn pin goes to '0' state.

When the OVP event disappears, the OVP on the CC line is turned-off and the FLGn pin goes back to 'Hi-Z' state.

7.8 VBUS discharge

VBUS discharge is activated via I2C bus and controlled via firmware by the USB-C power delivery controller. The VBUS discharge feature integrated in TCPP02-M18 allows to discharge 10 μF in less than 220 ms ($T_{\text{DIS_VBUS}}$).

This discharge time is in line with USB-C specification, extracted below for VBUS discharge:

Table 15. Common source electrical parameters from USB-C specification

Parameter	Description	Min.	Typ.	Max.	Units
tSafe0V	Time to reach vSafe0V max.	-	-	650	ms
tSafe5V	Time to reach vSafe5V max.	-	-	275	ms

7.9 V_{CONN} discharge

V_{CONN} discharge is activated via I2C bus and controlled via firmware by the USB-C power delivery controller.

The V_{CONN} discharge feature integrated in TCPP02-M18 allows to discharge V_{CONN} in $R_{\text{DIS_VCONN}} < 5.5 \text{ k}\Omega$, as per USB-C specification table extracted below:

Table 16. V_{CONN} source characteristics from USB-C power delivery specification

	Minimum	Maximum	Notes
R _{dch}	30 Ω	6120 Ω	Discharge resistance applied in UnattachedWait.SRC between the CC pin being discharged and GND.

Note:

- V_{CONN} discharge is activated and stopped via I2C commands from USB-PD controller
- To avoid short-circuit, V_{CONN} discharge cannot be activated if V_{CONN} switch are closed
- The CCxc pin discharged is the last one acting as V_{CONN}

7.10 OTP (over temperature protection)

Above 150°C typ., the OTP triggers the FLGn pin.

OVP and OCP on VCONN, CC lines, VBUS are shut down.

Auto recovery is ensured when the temperature goes back below OTP threshold.

8 Application example

8.1 X-NUCLEO-SRC1M1

The X-NUCLEO-SRC1M1 expansion board allows evaluating the features of the TCPP02-M18 for the USB Type-C™ and the protections for VBUS and CC lines suitable for source applications.

Please refer to X-NUCLEO-SRC1M1 documentation ([databrief](#), [quick start guide](#), [user manual](#), [schematic](#) and [BOM](#)) for detailed application usage of TCPP02-M18 and selection of external components.

8.2 STEVAL-2STPD01

The STEVAL-2STPD01 is an evaluation kit composed of an expansion board containing two Type-C ports and integrating two STPD01PUR programmable buck converters for USB Power Delivery, and the NUCLEO-G071RB STM32 Nucleo-64 development board.

The expansion board has been specifically developed to be stacked on the NUCLEO-G071RB development board using the capability of its microcontroller to manage two UCPD peripherals at the same time. It also embeds the TCPP02-M18 USB Type-C port protection for Source applications and the L7983PU50R synchronous step-down switching regulator.

Please refer to STEVAL-2STPD01 documentation ([databrief](#), [quick start guide](#), [user manual](#), [schematic](#)) for detailed USB-C PD with power sharing using TCPP02-M18.

8.3 PCB routing

When routing the TCPP02-M18, please respect the following recommendation:

- Place the circuit as close as possible to the USB-C connector in order to maximize the efficiency of the ESD protection for CC lines
- Place the ESD capacitor as close as possible to the TCPP02-M18

9 USB Type-C™ port protection (TCPP) comparison table

Table 17. Device comparison table

Part number	Expansion board	SW expansion board	USB Type-C™ application	Package
TCPP01-M12	X-NUCLEO-SNK1M1	X-CUBE-TCPP	Sink, UFP, consumer	QFN-12L
TCPP02-M18	X-NUCLEO-SRC1M1		Source, DFP, provider	QFN-18L
TCPP03-M20	X-NUCLEO-DRP1M1		DRP, dual role power DRD, dual role data Sink requiring current sense and OCP	QFN-20L

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 QFN18L 3.5x3.5 mm package information

Figure 11. QFN18L 3.5x3.5 mm package outline

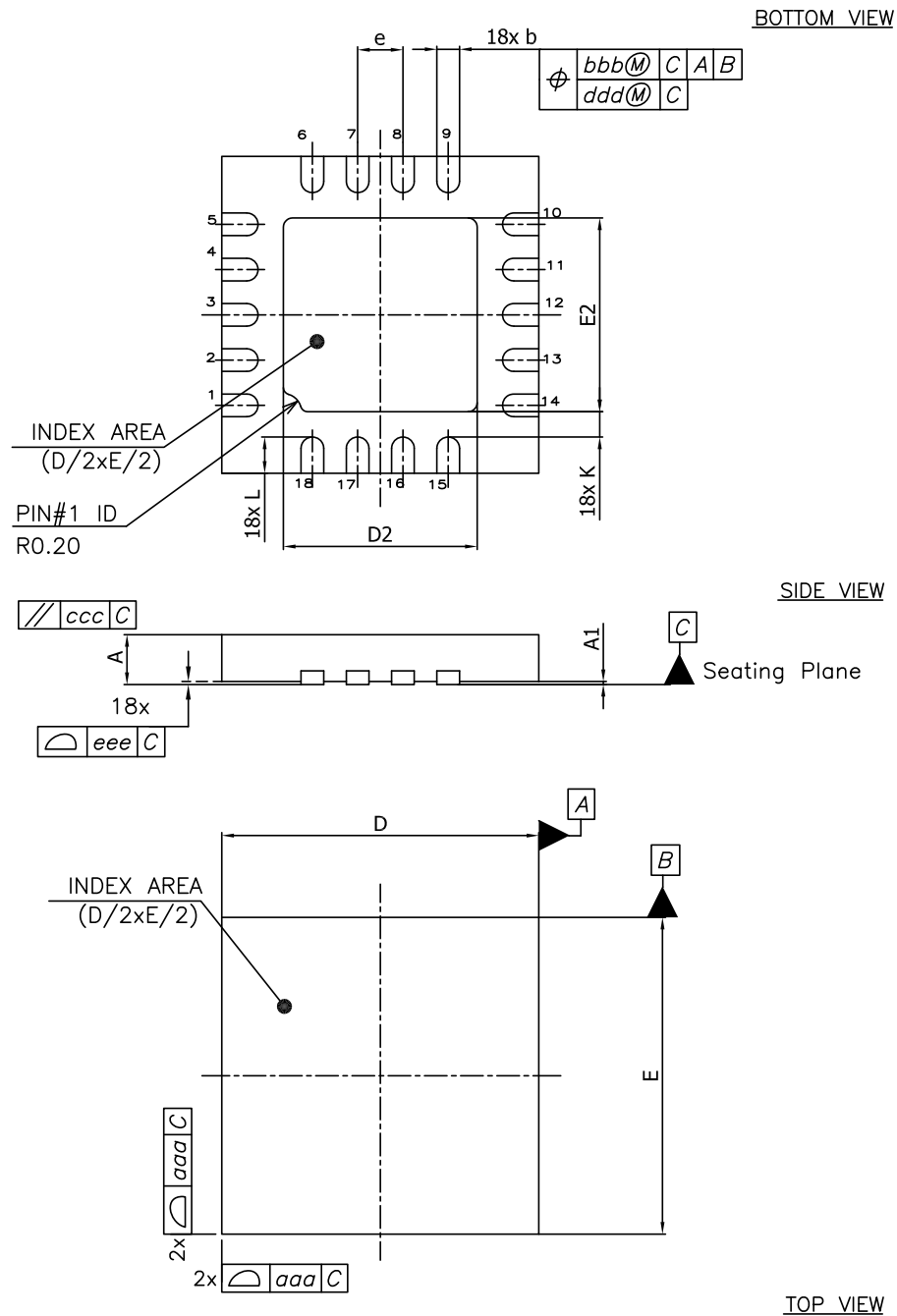


Table 18. QFN18L 3.5x3.5 mm mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.51	0.55	0.60
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		3.50	
D2	1.99	2.14	2.24
E		3.50	
E2	1.99	2.14	2.24
e		0.50	
L	0.30	0.40	0.50
K	0.20		
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 12. recommended footprint (dimensions are in mm)

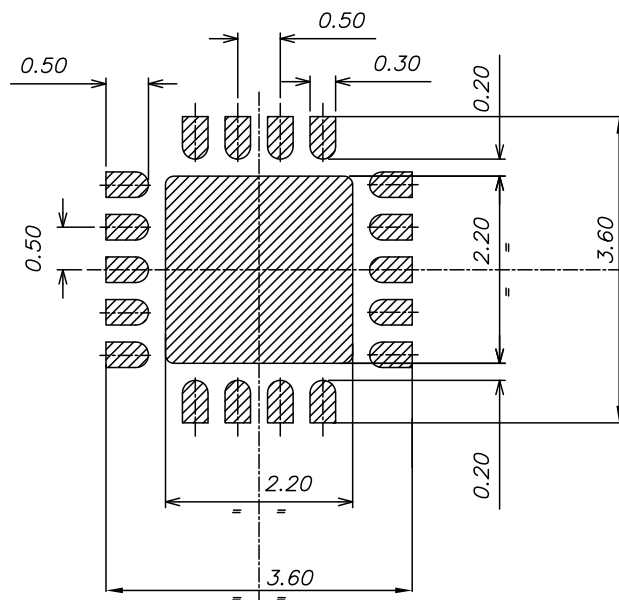


Figure 13. Tape and reel outline

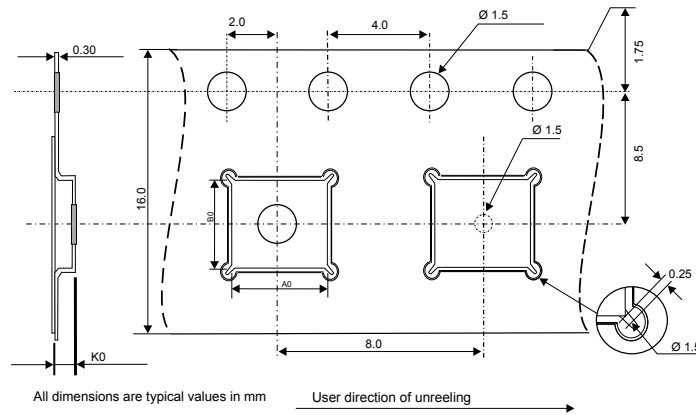
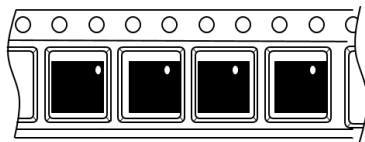


Table 19. Tape and reel mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A0	3.76	3.81	3.86
B0	3.76	3.81	3.86
K0	0.71	0.76	0.81

Figure 14. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Figure 15. Tape and reel orientation

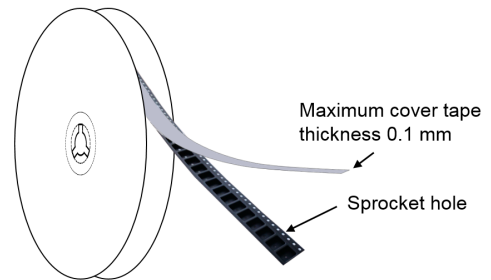


Figure 16. Reel dimensions (mm)

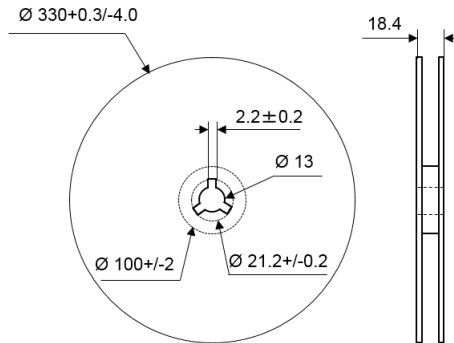


Figure 17. Inner box dimensions (mm)

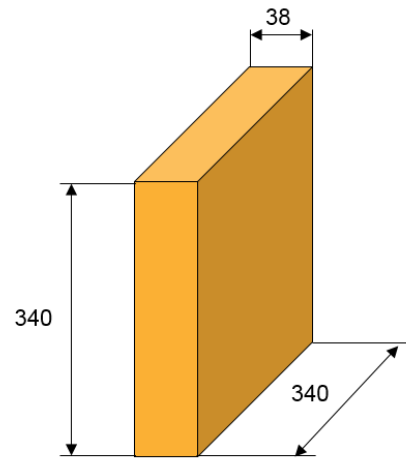
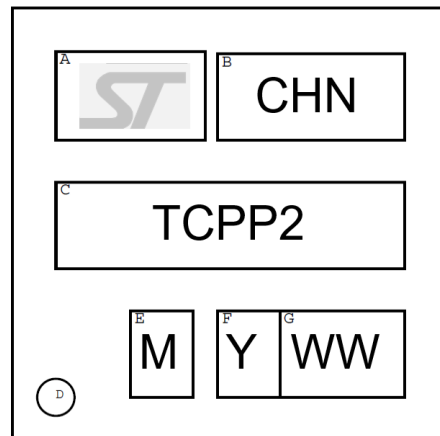


Figure 18. Marking

PACKAGE FACE : TOP



LEGEND

- Unmarkable Surface
- Marking Composition Field
- A - STANDARD ST LOGO
- B - COUNTRY OF ORIGIN
- C - MARKING AREA
- D - DOT
- E - Assy Plant (P)
- F - Assy Year (Y)
- G - Assy Week (WW)

11 Ordering information

Table 20. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TCPP02-M18	TCPP2	QFN-18L 3.5 x 3.5 x 0.55 mm	21.7 mg	3000	Tape and reel

Revision history

Table 21. Document revision history

Date	Revision	Changes
30-Aug-2021	1	Initial release.
04-Oct-2021	2	Updated Features, Table 6 , Table 7 and Table 20 .
09-May-2022	3	Added Section 8.1 and Section 8.2 . Updated Figure 4 .
17-May-2022	4	Updated cover image and added Figure 18 .

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