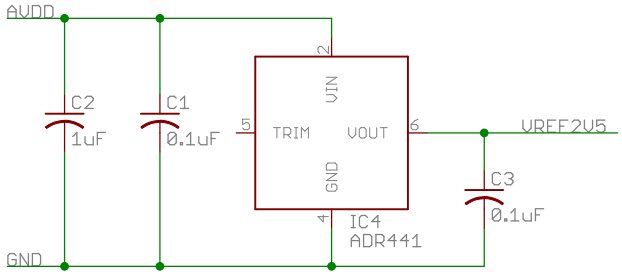

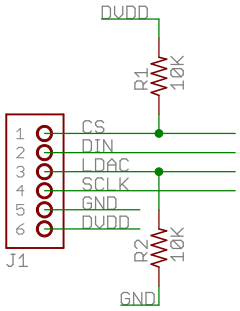

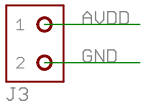

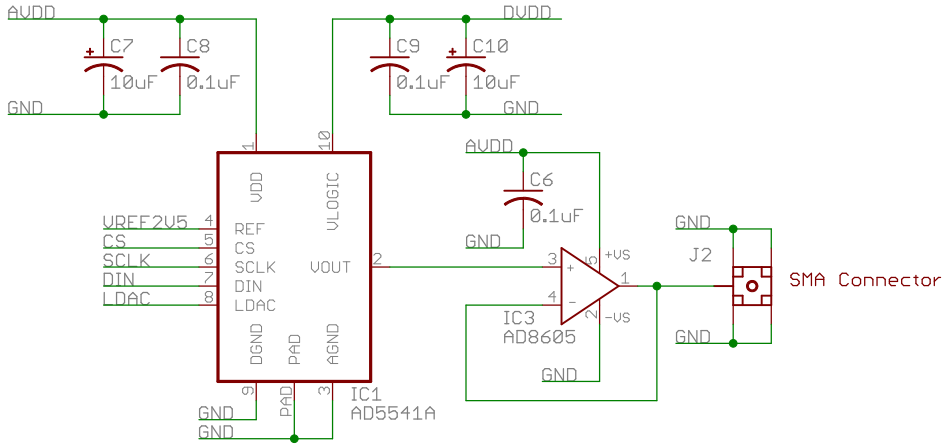

Note: Any external voltage applied to AVDD must be kept between 3.0V and 5.5V in order to avoid damaging the parts used in this circuit.

For more information on the parts used in this design, please refer to:
www.analog.com/AD5541A - 2.7V to 5.5V, Serial-Input, Voltage Output, Unbuffered 16-Bit DAC
www.analog.com/AD8605 - Precision, Low Noise, CMOS, Rail-to-Rail, Input/Output Operational Amplifier
www.analog.com/ADR441 - Ultralow Noise, LDO XFET Voltage Reference with Current Sink and Source

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SHEET:		Author: PJA
TITLE: PmodDA3		Rev: B.0
Doc#: 500-241	Date: 07/31/2012	Sheet: 1/1