To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8211TK

SiGe LOW NOISE AMPLIFIER FOR GPS/MOBILE COMMUNICATIONS

DESCRIPTION

The μPC8211TK is a silicon germanium (SiGe) monolithic integrated circuit designed as low noise amplifier for GPS and mobile communications.

The package is 6-pin lead-less minimold, suitable for surface mount.

This IC is manufactured using our 50 GHz f_{max} UHS2 (Ultra High Speed Process) SiGe bipolar process.

★ FEATURES

- Low noise : NF = 1.3 dB TYP. @ V_{CC} = 3.0 V
- High gain : G_P = 18.5 dB TYP. @ V_{CC} = 3.0 V
- Low current consumption : I_{CC} = 3.5 mA TYP. @ V_{CC} = 3.0 V
- Gain 1 dB compression output power : $P_{o\ (1\ dB)}$ = –6.0 dBm @ V_{CC} = 3.0 V
- Built-in power-save function
- High-density surface mounting : 6-pin lead-less minimold package (1.5 × 1.3 × 0.55 mm)

APPLICATION

- Low noise amplifier for GPS and mobile communications

ORDERING INFORMATION

Part Number	Order Number	Package	Marking	Supplying Form
μPC8211TK-E2	μPC8211TK-E2-A	6-pin lead-less minimold (1511 PKG) (Pb-Free) Note	6G	• Embossed tape 8 mm wide • Pin 1, 6 face the perforation side of the tape • Qty 5 kpcs/reel

Note With regards to terminal solder (the solder contains lead) plated products (conventionally plated), contact your nearby sales office.

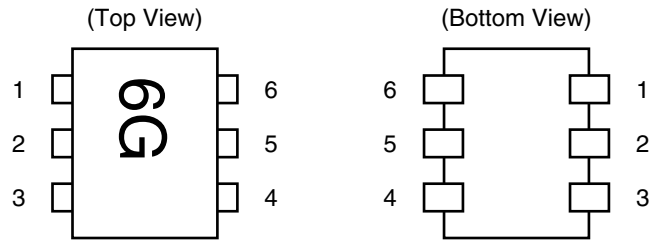
Remark To order evaluation samples, contact your nearby sales office.
Part number for sample order: μPC8211TK

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

Document No. PU10426EJ04V0DS (4th edition)
Date Published January 2006 CP(K)
Printed in Japan

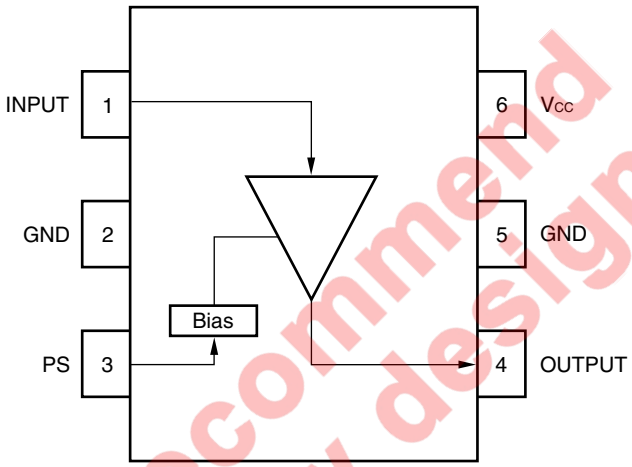
The mark ★ shows major revised points.

PIN CONNECTIONS



Pin No.	Pin Name
1	INPUT
2	GND
3	PS
4	OUTPUT
5	GND
6	V_{CC}

INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Ratings	Unit
Supply Voltage	V_{CC}	T_A = +25°C	4.0	V
Power-Saving Voltage	V_{PS}		–0.3 to V_{CC} +0.3	V
Power Dissipation of Package	P_D	T_A = +85°C **Note**	232	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C
Input Power	P_{in}		+10	dBm

Note Mounted on double-side copper-clad 50 × 50 × 1.6 mm epoxy glass PWB

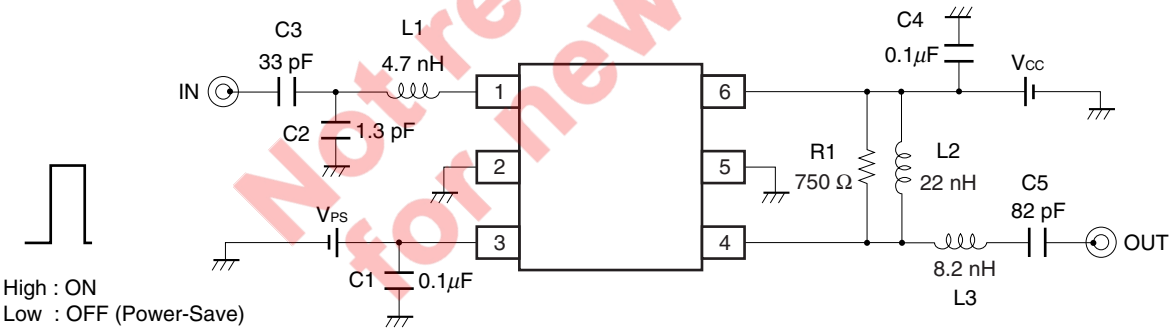
RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.3	V
Operating Ambient Temperature	T_A	–25	+25	+85	°C
Operating Frequency Range	f_{in}	–	1 575	–	MHz

★ ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.0 V, V_{PS} = 3.0 V, f_{in} = 1 575 MHz, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No Signal	2.5	3.5	4.5	mA
		At Power-Saving Mode	–	–	1	μA
Power Gain	G_P		15.5	18.5	21.5	dB
Noise Figure	NF		–	1.3	1.5	dB
Input 3rd Order Distortion Intercept Point	IIP_3		–	–12	–	dBm
Input Return Loss	RL_{in}		6.0	7.5	–	dB
Output Return Loss	RL_{out}		10	14.5	–	dB
Isolation	ISL		–	33.5	–	dB
Rising Voltage From Power-Saving Mode	V_{PSon}		2.2	–	–	V
Falling Voltage From Power-Saving Mode	V_{PSoff}		–	–	0.8	V
Gain Flatness	Flat	f_{RF} = ± 2.5 MHz	–	–	0.5	dB
Gain 1 dB Compression Output Power	$P_{O\ (1\ dB)}$		–	–6.0	–	dBm
Output Power	P_O	P_{in} = –10 dBm	–1.5	+2.0	–	dBm

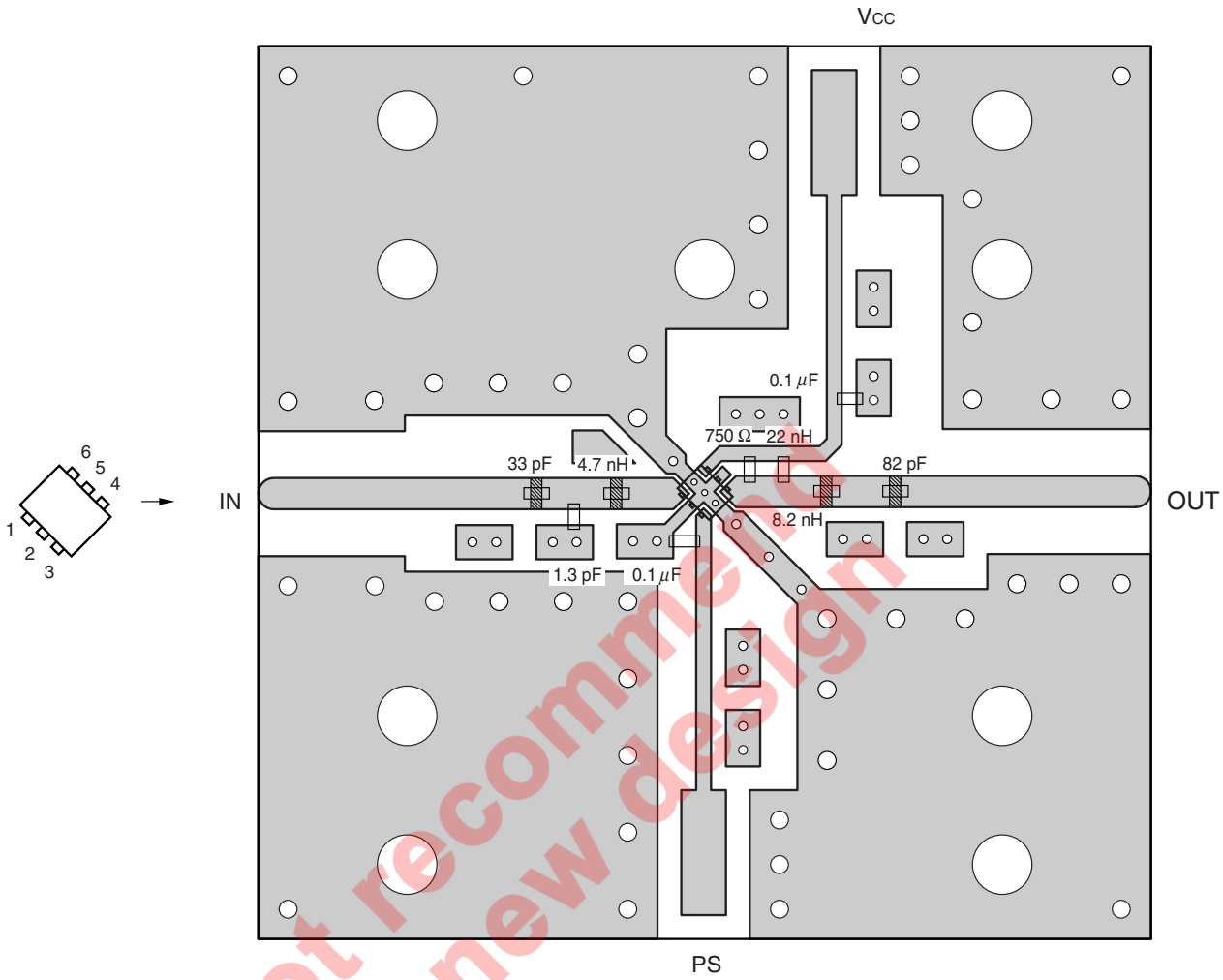
★ TEST CIRCUIT



COMPONENTS OF TEST CIRCUIT FOR MEASURING ELECTRICAL CHARACTERISTICS

Symbol	Form	Rating	Part Number	Maker
C_1, C_4	Chip Capacitor	0.1 μF	GRM36	Murata
C_2	Chip Capacitor	1.3 pF	GRM36	Murata
C_3	Chip Capacitor	33 pF	GRM36	Murata
C_5	Chip Capacitor	82 pF	GRM36	Murata
R_1	Resistor	750 Ω	RR0816	Susumu
L_1	Inductor	4.7 nH	TFL0510	Susumu
L_2	Inductor	22 nH	TFL0816 or TFL0510	Susumu
L_3	Inductor	8.2 nH	TFL0510	Susumu

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD

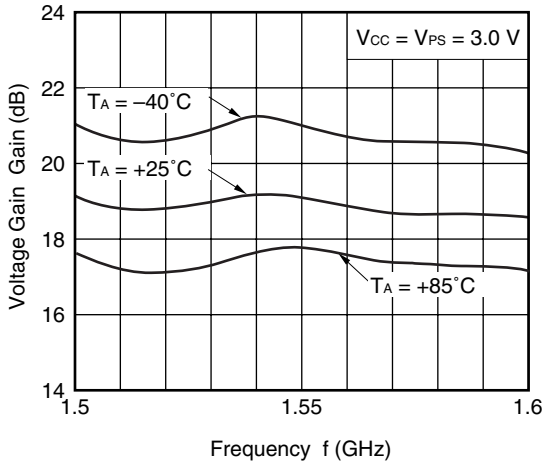


Notes

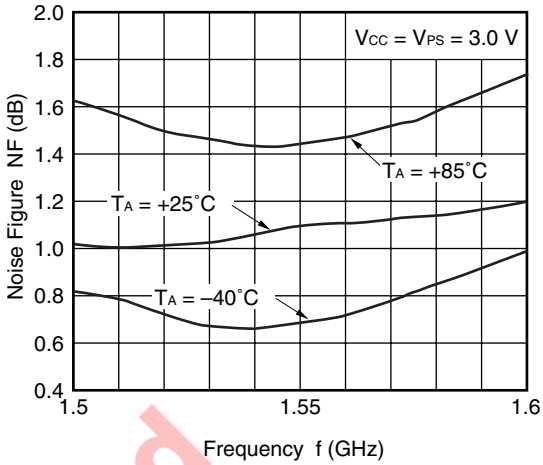
1. 30 × 30 × 0.51 mm double-side copper-clad hydrocarbon ceramic woven glass PWB (Rogers: R04003, εr = 3.38).
2. Back side: GND pattern
3. Au plated on pattern
4. ▨ represents cutout
5. ○: Through holes

TYPICAL CHARACTERISTICS (T_A = +25°C, unless otherwise specified)

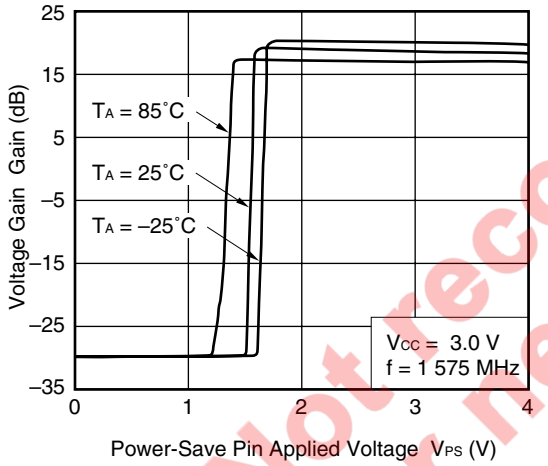
VOLTAGE GAIN vs. FREQUENCY



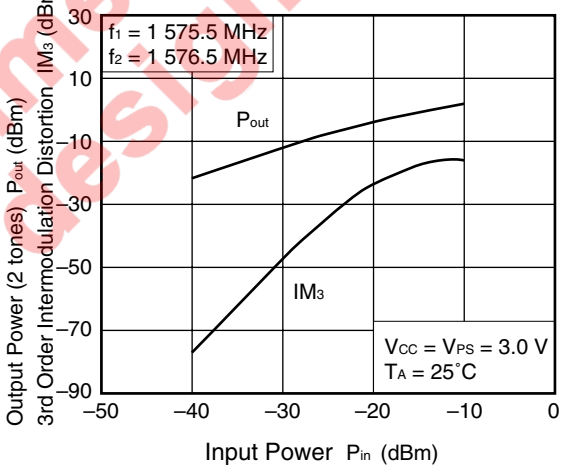
NOISE FIGURE vs. FREQUENCY



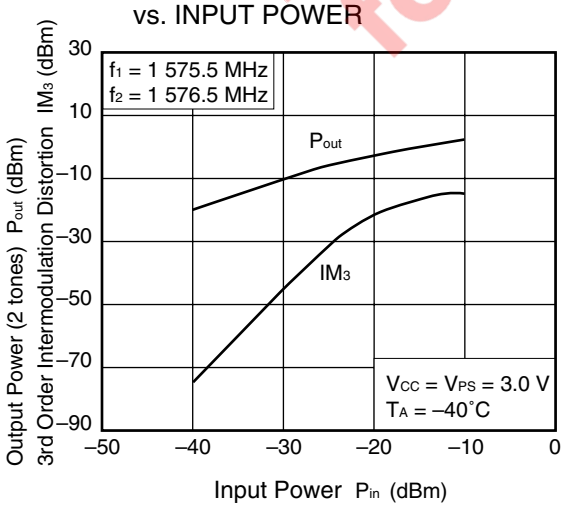
VOLTAGE GAIN vs. POWER-SAVE PIN APPLIED VOLTAGE



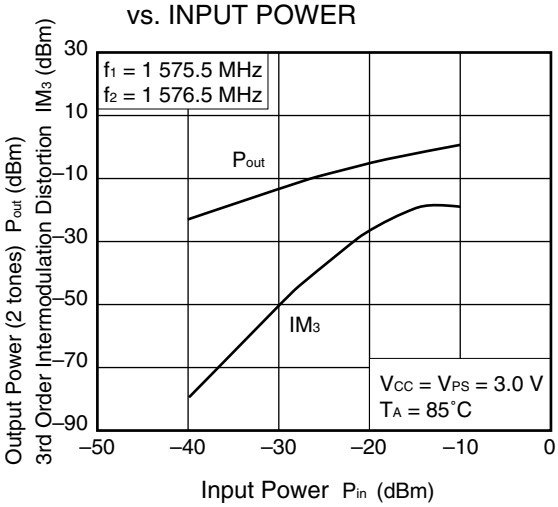
OUTPUT POWER (2 tones), IM3 vs. INPUT POWER



OUTPUT POWER (2 tones), IM3 vs. INPUT POWER



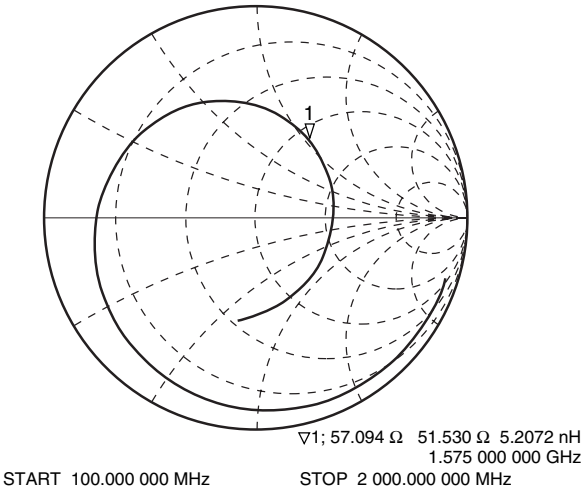
OUTPUT POWER (2 tones), IM3 vs. INPUT POWER



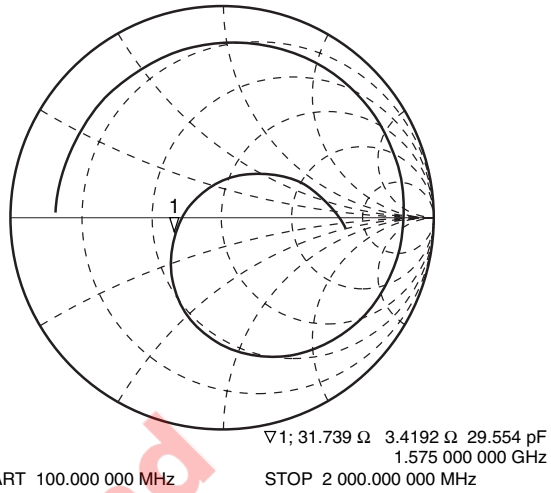
Remark The graphs indicate nominal characteristics.

S-PARAMETERS (T_A = +25°C, V_{CC} = V_{PS} = 3.0 V, monitored at connector on board)

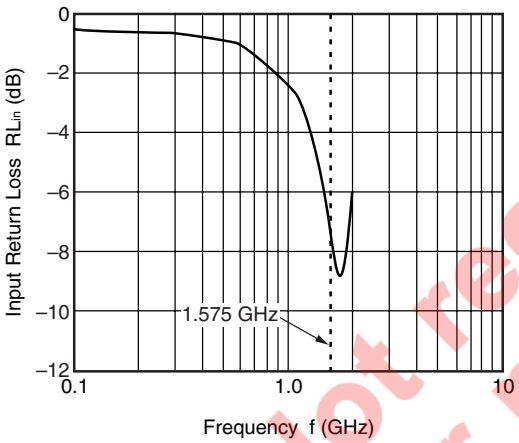
S_{11}-FREQUENCY



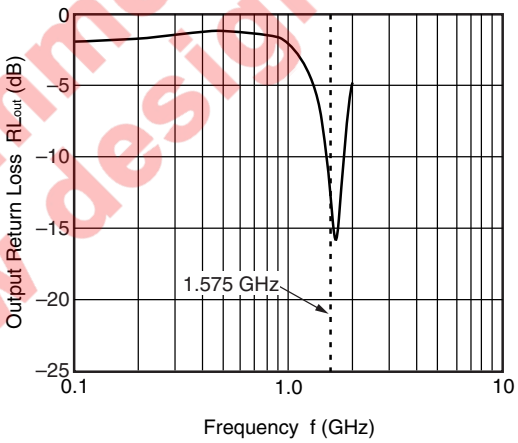
S_{22}-FREQUENCY



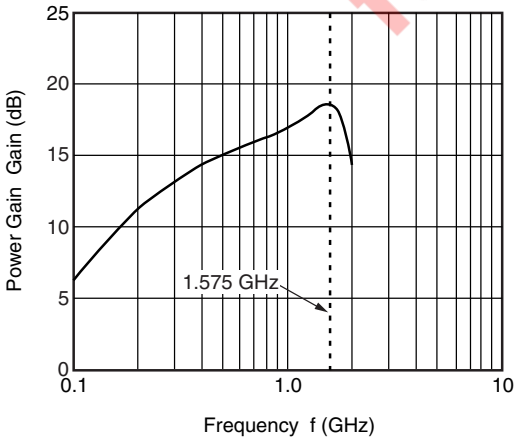
INPUT RETURN LOSS vs. FREQUENCY



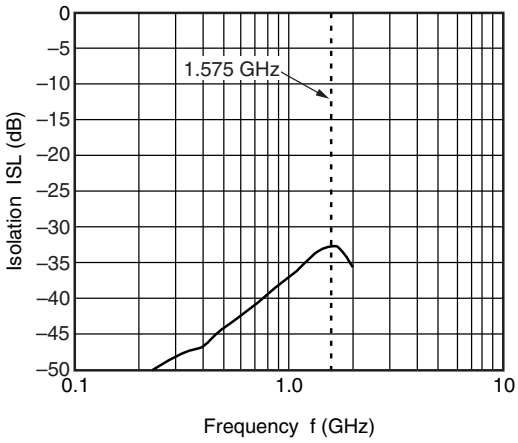
OUTPUT RETURN LOSS vs. FREQUENCY



POWER GAIN vs. FREQUENCY



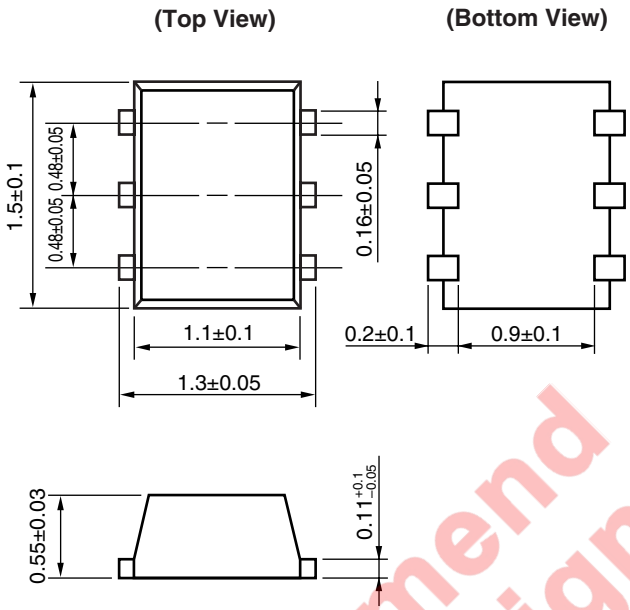
ISOLATION vs. FREQUENCY



Remark The graphs indicate nominal characteristics.

PACKAGE DIMENSIONS

6-PIN LEAD-LESS MINIMOLD (1511 PKG) (UNIT: mm)



Remark ( ) : Reference value

NOTES ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.

(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation). All the ground terminals must be connected together with wide ground pattern to decrease impedance difference.

(3) The bypass capacitor should be attached to V_{CC} line.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2%(Wt.) or below	IR260
Wave Soldering	Peak temperature (molten solder temperature) Time at peak temperature Preheating temperature (package surface temperature) Maximum number of flow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 120°C or below : 1 time : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (terminal temperature) Soldering time (per side of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	HS350

Caution Do not use different soldering methods together (except for partial heating).

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