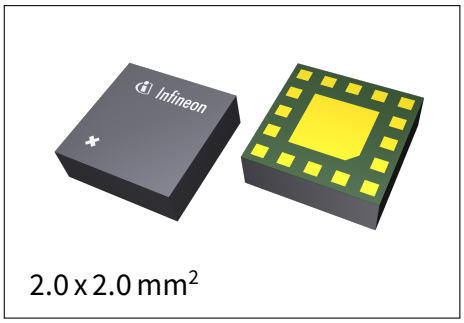
BGSX24MU16

DP4T Antenna Cross Switch with MIPI RFFE Control Interface

Features

- High linearity up to 36.5 dBm input power
- Low insertion loss and high port-to-port isolation up to 5.0 GHz
- Low current consumption
- MIPI RFFE 2.1 compliant control interface
- Software and hardware programmable USID
- Ultra low profile leadless plastic package
- RoHS and WEEE compliant package



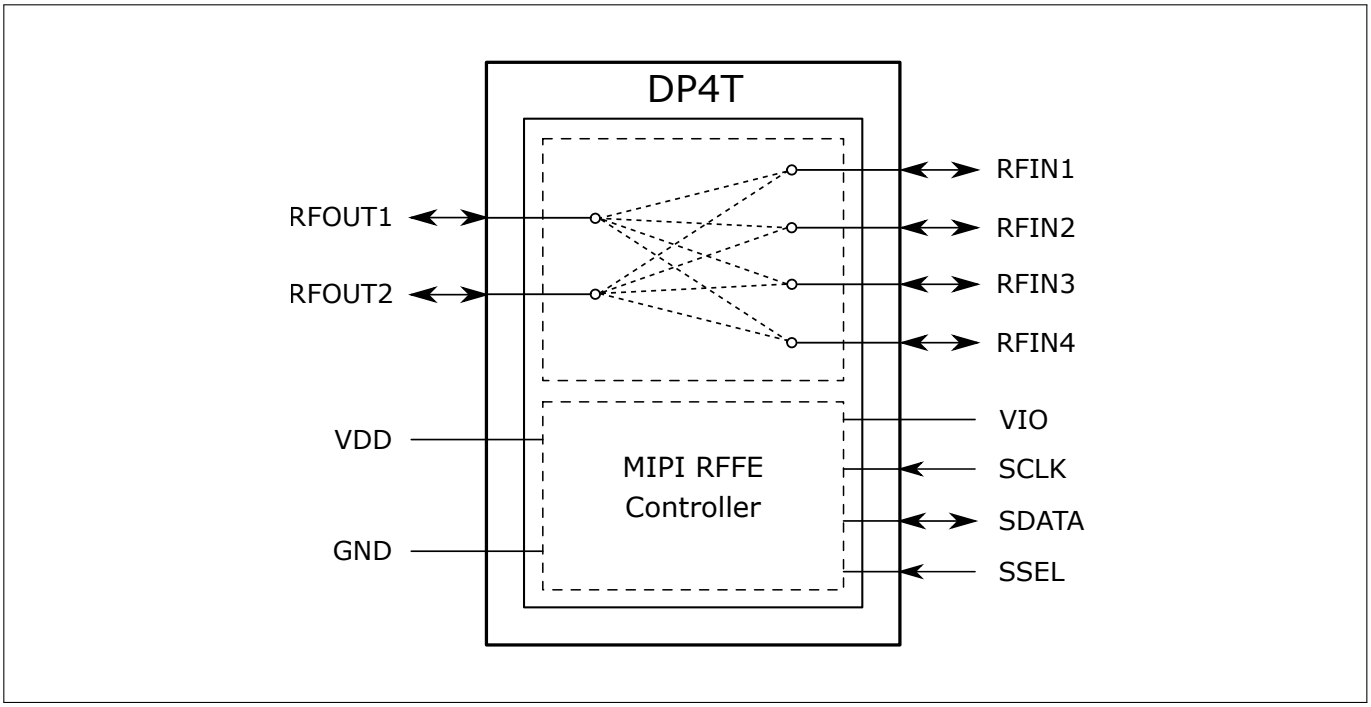
Potential Applications

DP4T antenna routing/swapping for cellular mobile devices. GSM/WCDMA/LTE post PA power level routing switch.

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block Diagram



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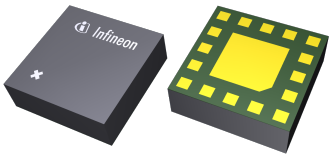
1 Features



- RF CMOS DP4T antenna cross switch with power handling capability of up to 36.5 dBm
- Suitable for multi-mode LTE and WCDMA quadruple antenna applications
- Low insertion loss and harmonics generation
- 0.1 to 5.0 GHz coverage
- High port-to-port-isolation
- No blocking capacitors required if no DC applied on RF lines
- Integrated MIPI RFFE interface operating in 1.65 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- Leadless and halogen free package PG-ULGA-16-1 with lateral size of 2.0 mm x 2.0 mm and thickness of 0.59 mm
- No power supply decoupling required
- High EMI robustness
- RoHS and WEEE compliant package

RoHS Halogen-Free Lead-Free Green

2 Product Description

The BGSX24MU16 RF CMOS switch is specifically designed for LTE and WCDMA quadruple antenna applications. This DP4T offers low insertion loss and low harmonic generation.

The switch is controlled via a MIPI RFFE controller. The on-chip controller allows power-supply voltages from 1.65 to 1.95 V. The switch features direct-connect-to-battery functionality and DC-free RF ports. Unlike GaAs technology, external DC blocking capacitors at the RF Ports are only required if DC voltage is applied externally. The BGSX24MU16 RF Switch is manufactured in Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherent higher ESD robustness. The device has a very small size of only 2.0 x 2.0 mm^2 and a maximum thickness of 0.59 mm.

Table 1: Ordering Information

Type	Package	Marking
BGSX24MU16	PG-ULGA-16-1	891

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range [1]	f	0.1	–	5.0	GHz	
Supply voltage	V_{DD}	-0.5	–	3.9	V	–
RF input power	P_{RF}	–	–	38	dBm	VSWR = 1:1, 12.5 % duty cycle
ESD robustness, CDM [2]	$V_{ESD,CDM}$	-1	–	+1	kV	
ESD robustness, HBM [3]	$V_{ESD,HBM}$	-1	–	+1	kV	
ESD robustness RF ports, SLT[4]	$V_{ESD,RF}$	-8	–	+8	kV	RF versus GND, with 27 nH shunt inductor
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0 V.
[2] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[3] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).
[4] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF ports and RF ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF ports
RFFE supply voltage	V_{IO}	-0.5	–	2.5	V	–
RFFE control voltage levels	V_{SCLK}, V_{SDATA}, V_{SSEL}	-0.7	–	V_{IO} + 0.7 (max. 2.5)	V	–

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.65	2.8	3.4	V	–
Supply current	I_{DD}	–	70	250	µA	Operating State
Supply current in standby mode	$I_{DD,sb}$	–	0.5	1	µA	VIO = low or MIPI low-power mode
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1)]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1)]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1)]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1)]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE supply current	I_{IO}	–	2	10	µA	Idle State
Ambient temperature	T_A	-40	25	85	°C	–

[1)] SCLK and SDATA

Table 5: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF input power	P_{RF}	–	–	36.5	dBm	VSWR = 1:1

5 RF Characteristics

Table 6: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, V_{DD}= 1.65 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1] at 25°C						
All RFOUT/RFIN ports	*IL*	–	0.40	0.50	dB	617–960 MHz
		–	0.45	0.60	dB	1425–2200 MHz
		–	0.55	0.70	dB	2300–2690 MHz
		–	0.75	1.10	dB	3300–3800 MHz
		–	1.00	1.90	dB	3800–5000 MHz
Insertion Loss[1]						
All RFOUT/RFIN ports	*IL*	–	0.40	0.60	dB	617–960 MHz
		–	0.45	0.70	dB	1425–2200 MHz
		–	0.55	0.80	dB	2300–2690 MHz
		–	0.75	1.30	dB	3300–3800 MHz
		–	1.00	2.10	dB	3800–5000 MHz
Return Loss[1]						
All RFOUT/RFIN ports	*RL*	23	30	–	dB	617–960 MHz
		19	28	–	dB	1425–2200 MHz
		17	26	–	dB	2300–2690 MHz
		11	20	–	dB	3300–3800 MHz
		7	16	–	dB	3800–5000 MHz

[1] Measured on application board, without any matching components.

Table 7: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, V_{DD}= 1.65 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Isolation On-On[1]						
RFOUT to RFOUT ports	*ISO*	41	49	–	dB	617–960 MHz
		36	43	–	dB	1425–2200 MHz
		35	42	–	dB	2300–2690 MHz
		34	41	–	dB	3300–3800 MHz
		30	40	–	dB	3800–5000 MHz
RFIN to RFIN ports	*ISO*	40	49	–	dB	617–960 MHz
		34	42	–	dB	1425–2200 MHz
		32	40	–	dB	2300–2690 MHz
		29	36	–	dB	3300–3800 MHz
		25	34	–	dB	3800–5000 MHz
RFIN to RFOUT ports	*ISO*	40	49	–	dB	617–960 MHz
		34	43	–	dB	1425–2200 MHz
		32	41	–	dB	2300–2690 MHz
		31	40	–	dB	3300–3800 MHz
		28	38	–	dB	3800–5000 MHz
Isolation On-Off[1]						
RFOUT to RFOUT ports	*ISO*	47	52	–	dB	617–960 MHz
		43	48	–	dB	1425–2200 MHz
		42	47	–	dB	2300–2690 MHz
		37	46	–	dB	3300–3800 MHz
		28	39	–	dB	3800–5000 MHz
RFIN to RFIN ports	*ISO*	39	48	–	dB	617–960 MHz
		32	41	–	dB	1425–2200 MHz
		31	40	–	dB	2300–2690 MHz
		29	38	–	dB	3300–3800 MHz
		26	36	–	dB	3800–5000 MHz
RFIN to RFOUT ports	*ISO*	39	49	–	dB	617–960 MHz
		33	42	–	dB	1425–2200 MHz
		32	40	–	dB	2300–2690 MHz
		30	39	–	dB	3300–3800 MHz
		26	38	–	dB	3800–5000 MHz

[1] Measured on application board without any external matching components.

Table 8: RF Characteristics at T_A = −40 °C...85 °C, V_{DD}= 1.65 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic Generation[1] at VSWR 1:1, 12.5 % duty cycle						
H2, GSM LB	P_{H2}	–	-67	-56	dBm	36 dBm, 600–915 MHz
H2, GSM HB		–	-63	-55	dBm	34 dBm, 1447–1980 MHz
H2		–	-83	-70	dBm	26 dBm, 600–915 MHz, CW
		–	-79	-70	dBm	26 dBm, 1447–1980 MHz, CW
		–	-76	-68	dBm	26 dBm, 2300–2690 MHz, CW
		–	-70	-62	dBm	29 dBm, 2300–2690 MHz, CW
		–	-70	-60	dBm	26 dBm, 3300–3800 MHz, CW
		–	-65	-50	dBm	26 dBm, 3800–5000 MHz, CW
H3, GSM LB	P_{H3}	–	-53	-48	dBm	36 dBm, 600–915 MHz
H3, GSM HB		–	-53	-47	dBm	34 dBm, 1447–1980 MHz
H3		–	-81	-72	dBm	26 dBm, 600–915 MHz, CW
		–	-77	-70	dBm	26 dBm, 1447–1980 MHz, CW
		–	-75	-68	dBm	26 dBm, 2300–2690 MHz, CW
		–	-66	-61	dBm	29 dBm, 2300–2690 MHz, CW
		–	-75	-65	dBm	26 dBm, 3300–3800 MHz, CW
		–	-75	-65	dBm	26 dBm, 3800–5000 MHz, CW
Intermodulation Distortion[1]						
IIP2	*IIP*2	100	120	–	dBm	IIP2 conditions, see Tab. 9
IIP3	*IIP*3	70	77	–	dBm	IIP3 conditions, see Tab. 10

[1] On application board without any matching components.
[2] Test condition outside of specified operation range.

Table 9: IMD2 Testcases

Band	Symbol	In-Band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD2,low}$	2140	1950	24	190	-10
	$B1_{IMD2,high}$	2140	1950	24	4090	-10
Band 5	$B5_{IMD2,high}$	880	835	24	1715	-10
Band 7	$B7_{IMD2,low}$	2655	2535	24	120	-10
	$B7_{IMD2,high}$	2655	2535	24	5190	-10

Table 10: IMD3 Testcases

Band	Symbol	In-Band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD3,low}$	2140	1950	24	95	-10
	$B1_{IMD3,mid}$	2140	1950	24	1760	-10
	$B1_{IMD3,high}$	2140	1950	24	6040	-10
Band 5	$B5_{IMD3,low}$	880	835	24	22.5	-10
	$B5_{IMD3,mid}$	880	835	24	790	-10
	$B5_{IMD3,high}$	880	835	24	2550	-10
Band 7	$B7_{IMD3,low}$	2655	2535	24	60	-10
	$B7_{IMD3,mid}$	2655	2535	24	2415	-10
	$B7_{IMD3,high}$	2655	2535	24	7725	-10

Table 11: Switching Times at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, V_{DD}= 1.65 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Times[1)]						
Power Up Settling Time	t_{PUP}	–	10	20	µs	Time from Power Up plus Switch command, 50 % last SCLK falling edge to 90 % RF signal
Switching Time	t_{ST}	–	1.2	2.0	µs	Time to switch between RF states, 50 % last SCLK falling edge to 90 % RF signal

[1)] Measured on application board without any external matching components.

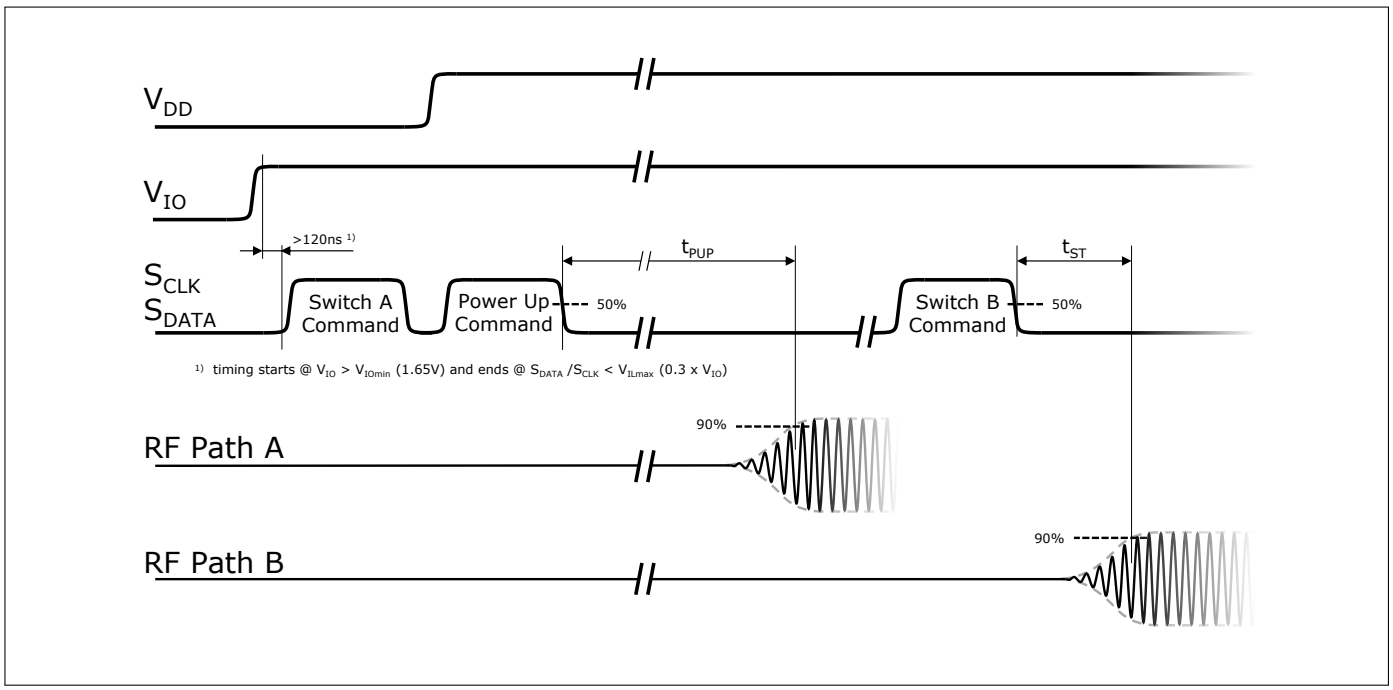


Figure 1: MIPI Timing Diagram

6 MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017' as well as the 'Qualcomm RFFE Vendor specification 80-N7876-1 Rev. W'.

Table 12: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	Up to 80 pF
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	External pin for changing USID: SSEL = 0 → 1011 SSEL = 1 → 1010
USID selection via SDATA / SCLK swap feature	No	

Table 13: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 14: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	REGISTER_0	7:1	RESERVED	Reserved for future use	0000000	No	Yes Trigger 0-10	R/W MW
		0	MODE_CTRL	Switch control	0			
0x01	REGISTER_1	7:0	MODE_CTRL	Switch control	00000000	No	Yes Trigger 0-10	R/W MW
0x1C	PM_TRIG	7	PWR_MODE(1) Operation Mode	0: Normal operation (ACTIVE) 1: Low Power Mode (LOW POWER)	1	Yes	No	R/W MW
		6	PWR_MODE(0) State Bit Vector	0: No action (ACTIVE) 1: Powered Reset (STARTUP to ACTIVE to LOW POWER)	0			
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0	No		
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		2	TRIGGER_2	0: No action (data held in shadow REG) 1: Data transferred to active REG	0	Yes		
		1	TRIGGER_1	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
		0	TRIGGER_0	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	11101001	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	0001			R
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Tab. 12	No	No	R/W

Table 15: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID		00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION		1101	No	No	R
		3:0	SUB_REVISION		0001			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:3	RESERVED	Reserved for future use	0x0	No	No	R/W
		2:0	BUS_LD[2:0]	Program the drive strength of the SDATA driver in readback modes. 0x0 to 0x3: Reserved for future use 0x4: 50pF (default) 0x5: 60pF 0x6: 80pF 0x7: 80pF	0x4			
0x2D	EXT_TRIG_MASK	7	TRIGGER_MASK_10	0: Data masked (held in shadow REG)	0	No	No	R/W MW
				1: Data not masked (ready for transfer to active REG)				
		6	TRIGGER_MASK_9	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		5	TRIGGER_MASK_8	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_7	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_6	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_MASK_5	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		1	TRIGGER_MASK_4	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		0	TRIGGER_MASK_3	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				

Table 16: Register Mapping, Table III

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2E	EXT_TRIG	7	TRIGGER_10	0: No action (data held in shadow REG)	0	Yes	No	R/W MW
				1: Data transferred to active REG				
		6	TRIGGER_9	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		5	TRIGGER_8	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		4	TRIGGER_7	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		3	TRIGGER_6	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		2	TRIGGER_5	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		1	TRIGGER_4	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_3	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				

Table 17: Modes of Operation (Truth Table)

		REGISTER_0 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
A	DP4T Direct (enables States 1-21)	x	x	x	x	x	x	x	0
B	DP4T Cross (enables States 22-42)	x	x	x	x	x	x	x	1
		REGISTER_1 Bits (DP4T Direct Mode)							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	Isolation	x	x	0	0	0	0	0	0
2	RFIN1-RFOUT1; RFOUT2-Isolation	x	x	0	0	0	0	0	1
3	RFIN1-RFOUT1; RFIN2-RFOUT2	x	x	0	1	0	0	1	1
4	RFIN1-RFOUT1; RFIN3-RFOUT2	x	x	0	1	0	1	0	1
5	RFIN1-RFOUT1; RFIN4-RFOUT2	x	x	0	1	1	0	0	1
6	RFIN2-RFOUT1; RFOUT2-Isolation	x	x	0	0	0	0	1	0
7	RFIN2-RFOUT1; RFIN1-RFOUT2	x	x	1	0	0	0	1	1
8	RFIN2-RFOUT1; RFIN3-RFOUT2	x	x	0	1	0	1	1	0
9	RFIN2-RFOUT1; RFIN4-RFOUT2	x	x	0	1	1	0	1	0
10	RFIN3-RFOUT1; RFOUT2-Isolation	x	x	0	0	0	1	0	0
11	RFIN3-RFOUT1; RFIN1-RFOUT2	x	x	1	0	0	1	0	1
12	RFIN3-RFOUT1; RFIN2-RFOUT2	x	x	1	0	0	1	1	0
13	RFIN3-RFOUT1; RFIN4-RFOUT2	x	x	0	1	1	1	0	0
14	RFIN4-RFOUT1; RFOUT2-Isolation	x	x	0	0	1	0	0	0
15	RFIN4-RFOUT1; RFIN1-RFOUT2	x	x	1	0	1	0	0	1
16	RFIN4-RFOUT1; RFIN2-RFOUT2	x	x	1	0	1	0	1	0
17	RFIN4-RFOUT1; RFIN3-RFOUT2	x	x	1	0	1	1	0	0
18	RFIN1-RFOUT2; RFOUT1-Isolation	x	x	1	1	0	0	0	1
19	RFIN2-RFOUT2; RFOUT1-Isolation	x	x	1	1	0	0	1	0
20	RFIN3-RFOUT2; RFOUT1-Isolation	x	x	1	1	0	1	0	0
21	RFIN4-RFOUT2; RFOUT1-Isolation	x	x	1	1	1	0	0	0
		REGISTER_1 Bits (DP4T Cross Mode)							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
22	Isolation	x	x	0	0	0	0	0	0
23	RFIN1-RFOUT2; RFOUT1-Isolation	x	x	0	0	0	0	0	1
24	RFIN1-RFOUT2; RFIN2-RFOUT1	x	x	0	1	0	0	1	1
25	RFIN1-RFOUT2; RFIN3-RFOUT1	x	x	0	1	0	1	0	1
26	RFIN1-RFOUT2; RFIN4-RFOUT1	x	x	0	1	1	0	0	1
27	RFIN2-RFOUT2; RFOUT1-Isolation	x	x	0	0	0	0	1	0
28	RFIN2-RFOUT2; RFIN1-RFOUT1	x	x	1	0	0	0	1	1
29	RFIN2-RFOUT2; RFIN3-RFOUT1	x	x	0	1	0	1	1	0
30	RFIN2-RFOUT2; RFIN4-RFOUT1	x	x	0	1	1	0	1	0
31	RFIN3-RFOUT2; RFOUT1-Isolation	x	x	0	0	0	1	0	0
32	RFIN3-RFOUT2; RFIN1-RFOUT1	x	x	1	0	0	1	0	1
33	RFIN3-RFOUT2; RFIN2-RFOUT1	x	x	1	0	0	1	1	0
34	RFIN3-RFOUT2; RFIN4-RFOUT1	x	x	0	1	1	1	0	0
35	RFIN4-RFOUT2; RFOUT1-Isolation	x	x	0	0	1	0	0	0
36	RFIN4-RFOUT2; RFIN1-RFOUT1	x	x	1	0	1	0	0	1
37	RFIN4-RFOUT2; RFIN2-RFOUT1	x	x	1	0	1	0	1	0
38	RFIN4-RFOUT2; RFIN3-RFOUT1	x	x	1	0	1	1	0	0
39	RFIN1-RFOUT1; RFOUT2-Isolation	x	x	1	1	0	0	0	1
40	RFIN2-RFOUT1; RFOUT2-Isolation	x	x	1	1	0	0	1	0
41	RFIN3-RFOUT1; RFOUT2-Isolation	x	x	1	1	0	1	0	0
42	RFIN4-RFOUT1; RFOUT2-Isolation	x	x	1	1	1	0	0	0

7 Package Information

The switch has a package size of 2000 µm in X-dimension and 2000 µm in Y-dimension with a maximum deviation of ±50 µm in each dimension. Fig. 2 shows the footprint from top view. The pin definitions are listed in Tab. 19.

Table 18: Mechanical Data

Parameter	Symbol	Value	Unit
Package X-dimension	*X*	2000 ± 50	µm
Package Y-dimension	*Y*	2000 ± 50	µm
Package height	*H*	590 ± 50	µm

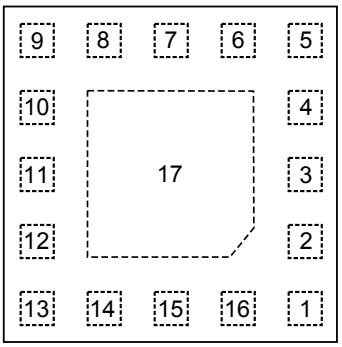


Figure 2: Footprint (top view)

Table 19: Pin Definition and Function

Pin No.	Name	Function
1	RFIN1	RF input port 1
2	GND	RF ground
3	RFOUT1	RF output port 1
4	GND	RF ground
5	SSEL	MIPI USID select port (to be connected to VIO or GND)
6	VIO	MIPI RFFE power supply
7	SCLK	MIPI RFFE clock
8	SDATA	MIPI RFFE data
9	VDD	Power supply
10	GND	RF ground
11	RFOUT2	RF output port 2
12	GND	RF ground
13	RFIN4	RF input port 4
14	RFIN3	RF input port 3
15	GND	RF ground
16	RFIN2	RF input port 2
17	GND	RF ground

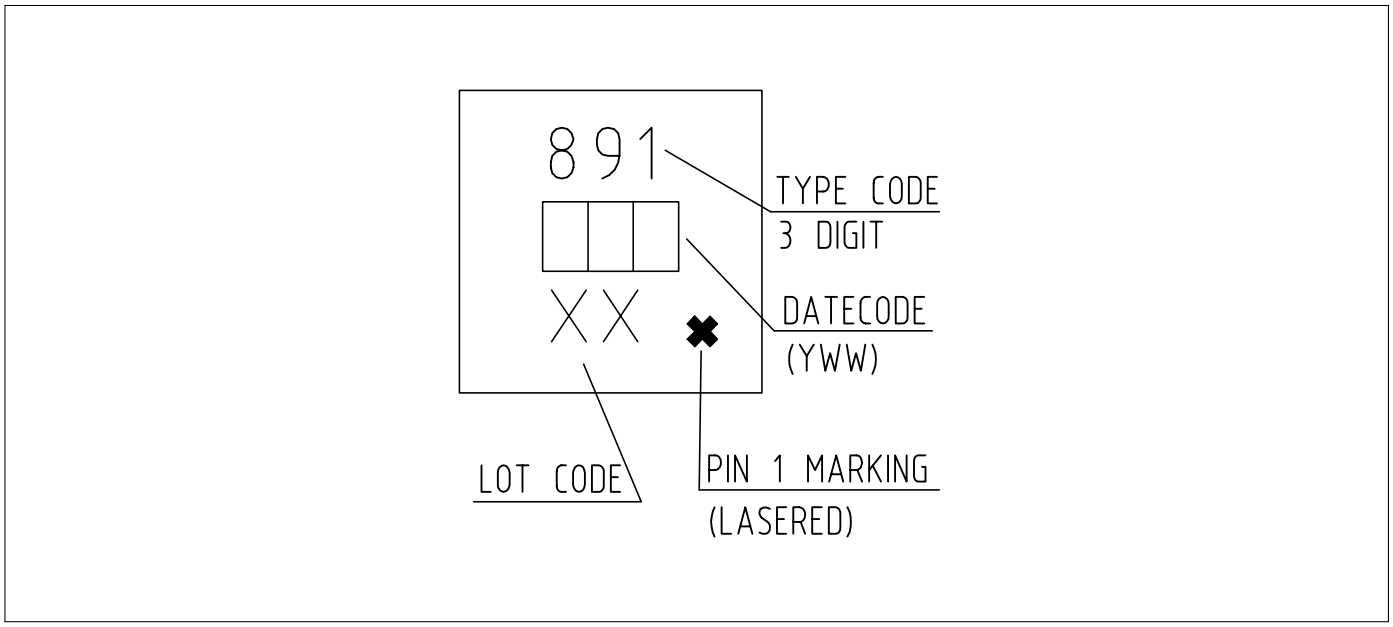


Figure 3: Marking Specification (top view)

Table 20: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"
2010	0	2020	0
2011	1	2021	1
2012	2	2022	2
2013	3	2023	3
2014	4	2024	4
2015	5	2025	5
2016	6	2026	6
2017	7	2027	7
2018	8	2028	8
2019	9	2029	9

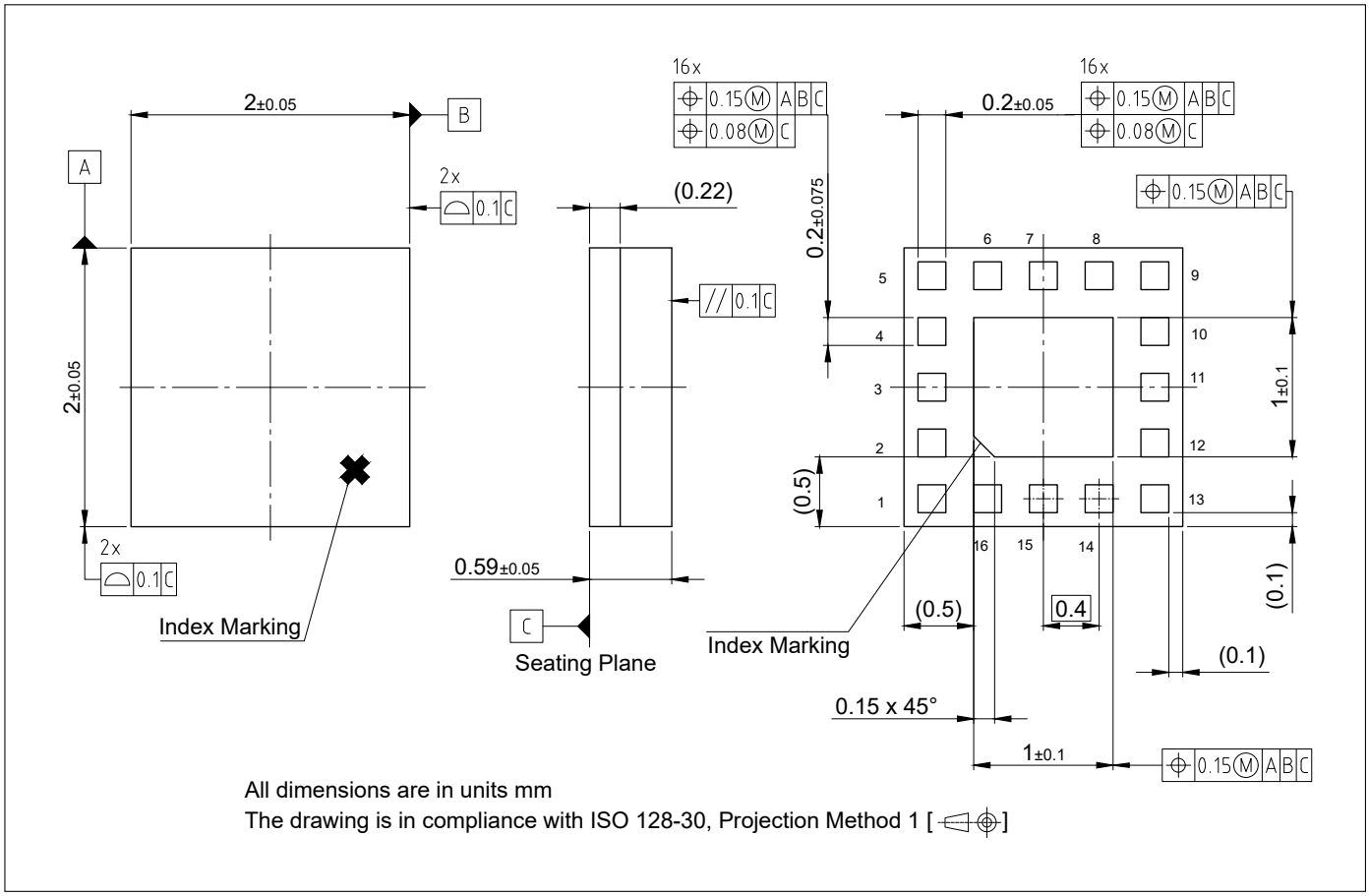


Figure 4: Package Outline Drawing (top, side and bottom views)

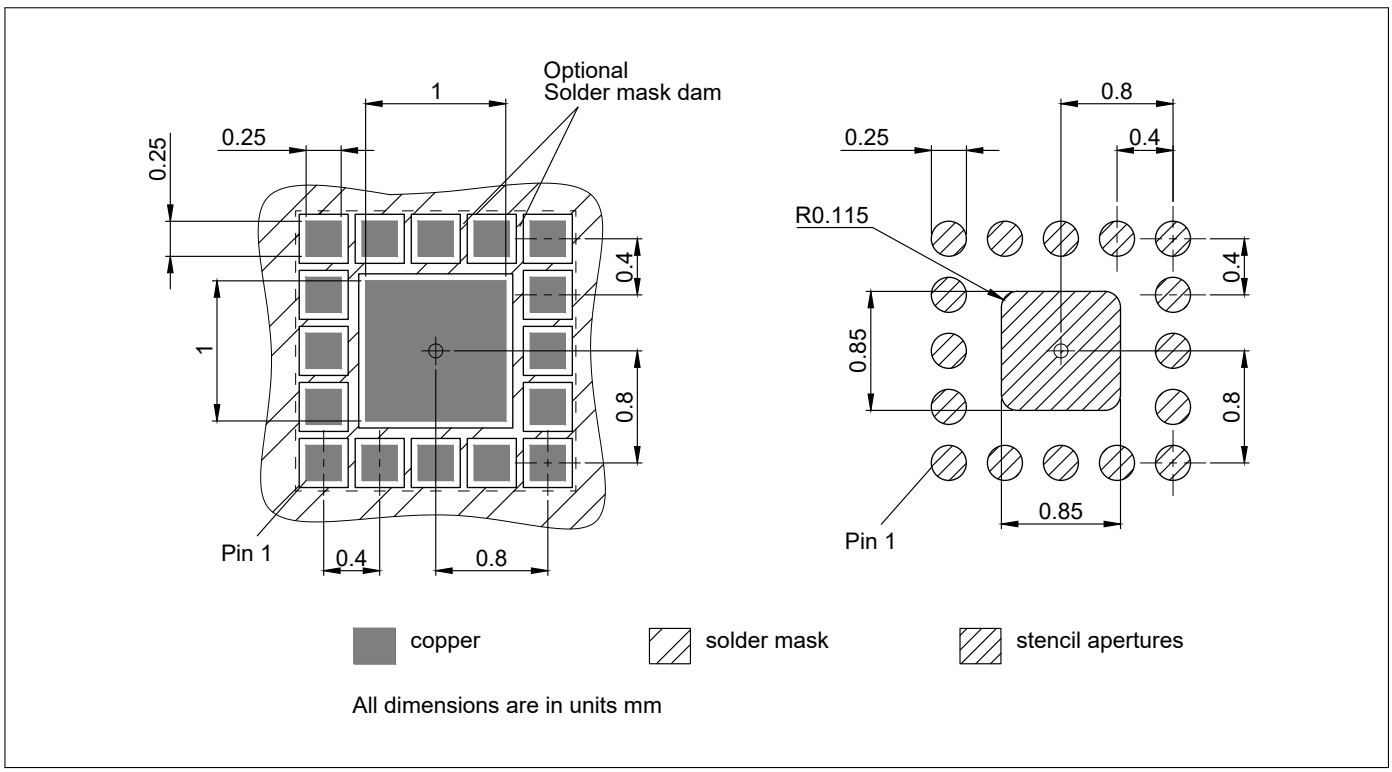


Figure 5: Footprint Recommendation

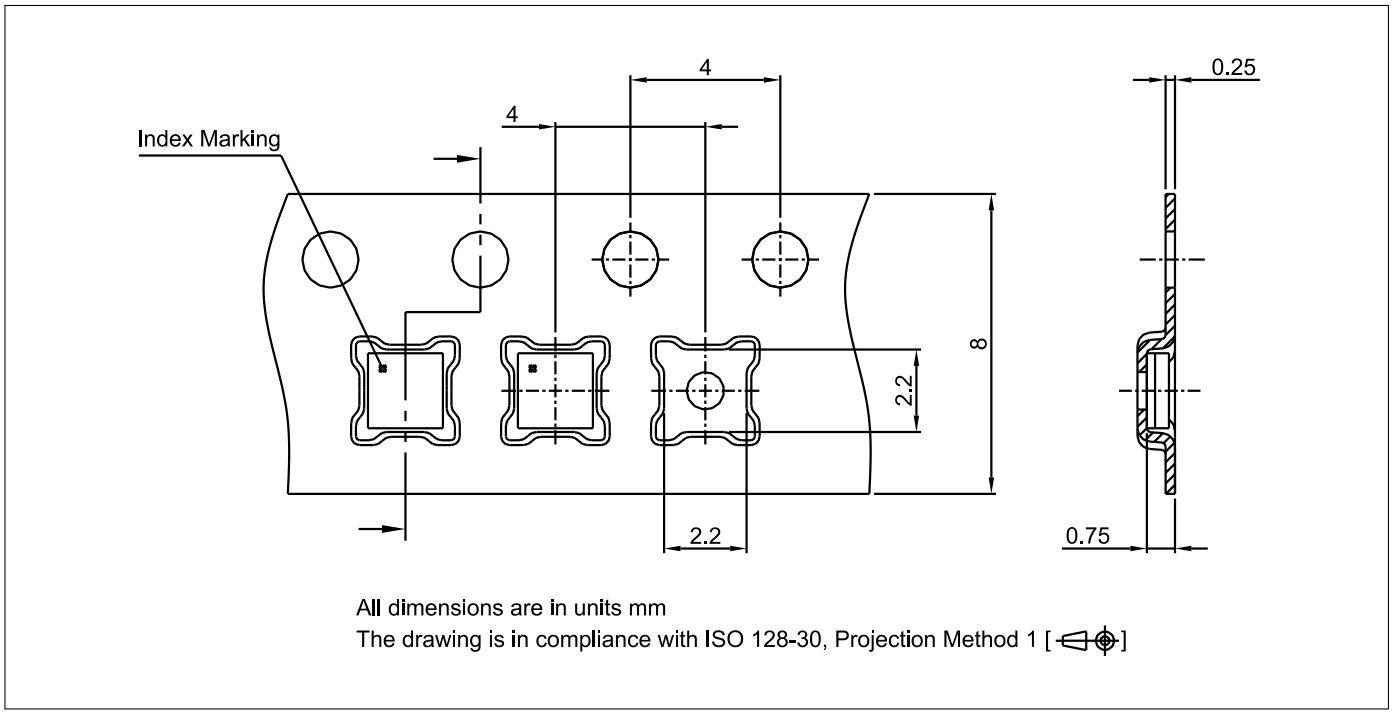


Figure 6: Carrier Tape Drawing (top and side views)

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.1 - 2020-08-31	
8	Switching time characteristics updated in Table 11
Revision 2.2, 2020-09-15	
11	REV_ID default value updated in Table 15

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Edition 2020-09-15
Published by
Infineon Technologies AG
81726 Munich, Germany

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