LSF0108-Q1 Automotive 8-Channel Multi-Voltage Level Translator

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device HBM ESD classification level 2000-V
  - Device CDM ESD classification level 1000-V
- Provides bidirectional voltage translation with no direction pin
- Supports up to 100 MHz up translation and greater than 100 MHz down translation at ≤ 30-pF capacitive load and up to 40 MHz up or down translation at 50-pF capacitive load
- Supports hot insertion
- Allow bidirectional voltage level translation between
  - 0.95 V ↔ 1.8 V, 2.5 V, 3.3 V, 5 V
  - 1.2 V ↔ 1.8 V, 2.5 V, 3.3 V, 5 V
  - 1.8 V ↔ 2.5 V, 3.3 V, 5 V
  - 2.5 V ↔ 3.3 V, 5 V
  - 3.3 V ↔ 5 V
- Low standby current
- 5-V tolerance I/O port to support TTL
- Low r_{on} provides less signal distortion
- High-impedance I/O pins for EN = low
- Flow-through pinout for easy PCB trace routing
- Latch-up performance exceeds 100 mA per JESD 17
- –40°C to +125°C operating temperature range

2 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I^2C, and other interfaces in telecom infrastructure
- Infotainment and cluster
- Body electronics and lighting
- Hybrid, electric and powertrain systems
- Passive safety
- ADAS

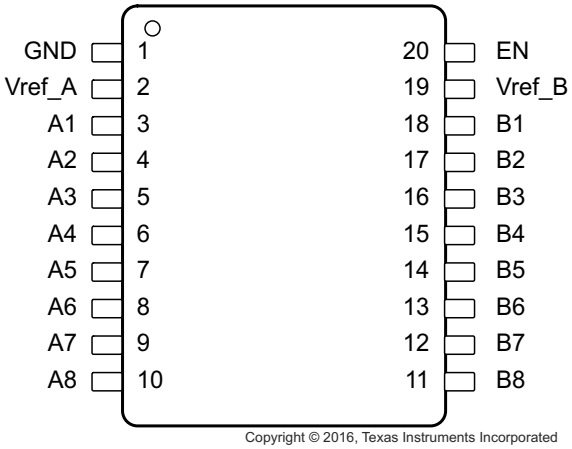
3 Description

- Supports up to 100 MHz up translation and greater than 100 MHz down translation at <= 30 pF cap load and up to 40 MHz up/down translation at 50 pF cap load:
  - Allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO).
- Bidirectional voltage translation without DIR pin:
  - Minimizes system effort to develop voltage translation for bidirectional interface (PMBus, I^2C, or SMbus).
- 5 V tolerance on IO port and 125°C support:
  - With 5 V tolerance and 125°C support, the LSF family is flexible and compliant with TTL levels in industrial and telecom applications.
- Channel specific translation:
  - The LSF family is able to set up different voltage translation levels on each channel.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LSF0108-Q1	TSSOP (20)	4.40 mm × 6.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Device Pinout Drawing

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Updated the *Bidirectional Translsation* section to include inclusive terminology....11

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- Changed *Thermal Information* values....4

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- Deleted ESD Performance Tested Per JESD 22 from *Features*....1
- Updated *Features* and *Applications*....1
- Added *Receiving Notification of Documentation Updates* section....1
- Deleted $R_{\theta JA}$ from *Absolute Maximum Ratings* table....4
- Changed ANSI/ESDA/JEDEC JS-001 to AEC-Q100 - 002 and JEDEC specification JESD22- V C101 to AEC-100-011 in *ESD Ratings*....4
- Updated *Short Trace Layout* image....15

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5 Pin Configuration and Functions

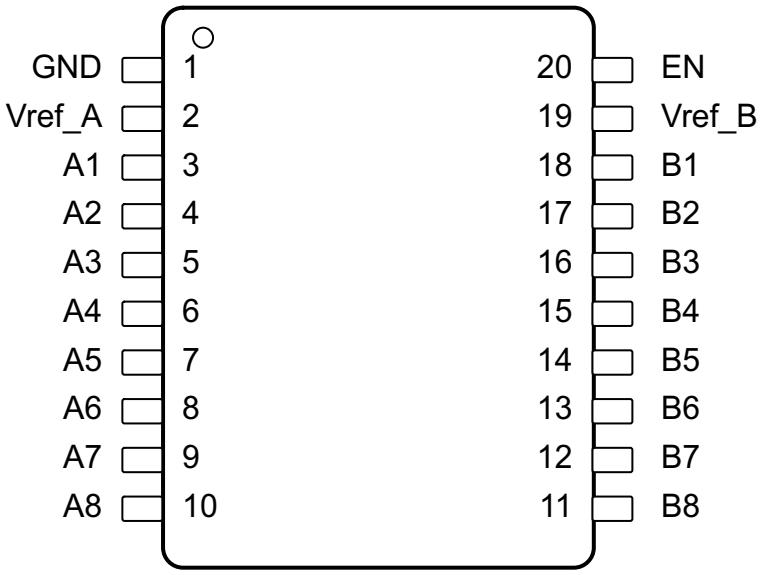


Figure 5-1. PW Package
20-Pin TSSOP
Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	3	I/O	Data port
A2	4	I/O	Data port
A3	5	I/O	Data port
A4	6	I/O	Data port
A5	7	I/O	Data port
A6	8	I/O	Data port
A7	9	I/O	Data port
A8	10	I/O	Data port
B1	18	I/O	Data port
B2	17	I/O	Data port
B3	16	I/O	Data port
B4	15	I/O	Data port
B5	14	I/O	Data port
B6	13	I/O	Data port
B7	12	I/O	Data port
B8	11	I/O	Data port
EN	20	I	Switch enable input; connect to Vref_B and pull-up through a high resistor (200 kΩ).
GND	1	—	Ground
Vref_A	2	—	Reference supply voltage A; see
Vref_B	19	—	Reference supply voltage B; see

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage(2)		–0.5	7	V
$V_{I/O}$	Input/output voltage(2)		–0.5	7	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
T_J	Max Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5	V
$V_{ref\_A/B/EN}$	Reference voltage	0	5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LSF0108-Q1 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	I_I = –18 mA,	V_{EN} = 0				–1.2	V
I_{IH}	V_I = 5 V	V_{EN} = 0				5	µA
I_{CC}	V_{ref_B} = V_{EN} = 5.5 V, V_{ref_A} = 4.5 V, I_O = 0, V_I = V_{CC} or GND				6		µA
$C_{I(ref\_A/B/EN)}$	V_I = 3 V or 0				11		pF
$C_{io(off)}$	V_O = 3 V or 0,	V_{EN} = 0			4	6	pF
$C_{io(on)}$	V_O = 3 V or 0,	V_{EN} = 3 V			10.5	12.5	pF
r_{on} (2)	V_I = 0,	I_O = 64 mA	V_{ref_A} = 3.3 V; V_{ref_B} = V_{EN} = 5 V		8		Ω
			V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 5 V		9		
			V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 5 V		10		
	V_I = 0,	I_O = 32 mA	V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 5 V		10		Ω
			V_{ref_A} = 2.5 V; V_{ref_B} = V_{EN} = 5 V		15		
	V_I = 1.8 V,	I_O = 15 mA	V_{ref_A} = 3.3 V; V_{ref_B} = V_{EN} = 5 V		9		Ω
	V_I = 1.0 V,	I_O = 10 mA	V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 3.3 V		18		Ω
	V_I = 0 V,	I_O = 10 mA	V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 3.3 V		20		Ω
	V_I = 0 V,	I_O = 10 mA	V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 1.8 V		30		Ω

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

6.6 Switching Characteristics (Translating Down), V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	1.9		1.4		0.75		ns
t_{PHL}			2		1.5		0.85		

6.7 Switching Characteristics (Translating Down), V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	2		1.45		0.8		ns
t_{PHL}			2.1		1.55		0.9		

6.8 Switching Characteristics (Translating Up), V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V and R_L = 300 (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	2.1		1.55		0.9		ns
t_{PHL}			2.2		1.65		1		

6.9 Switching Characteristics (Translating Up), V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V and R_L = 300 (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	1.8		1.35		0.8		ns
t_{PHL}			1.9		1.45		0.9		

6.10 Typical Characteristics

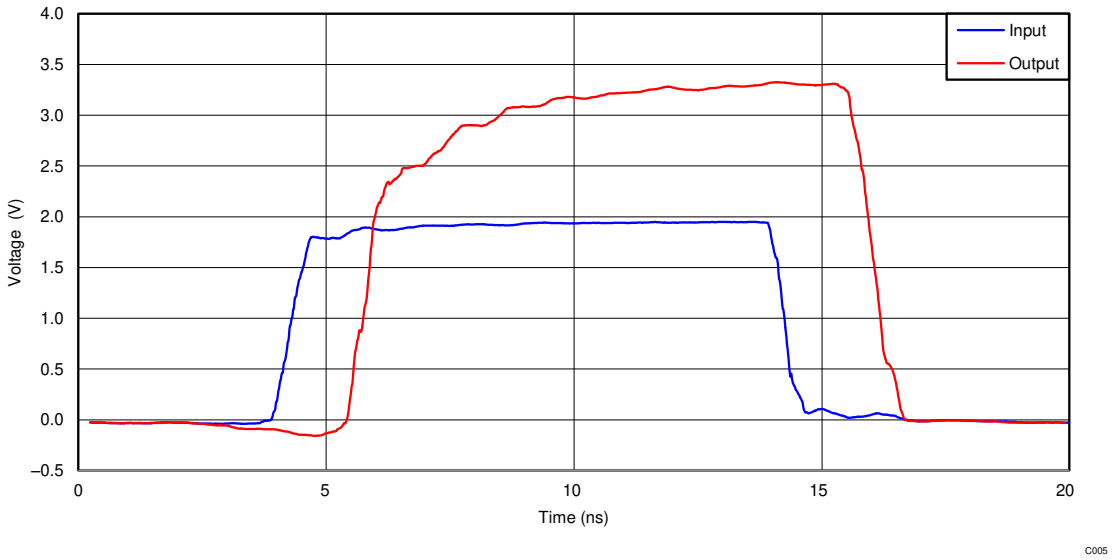
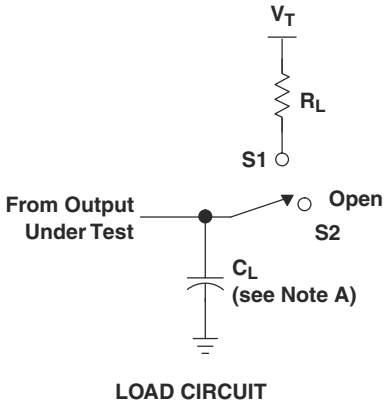
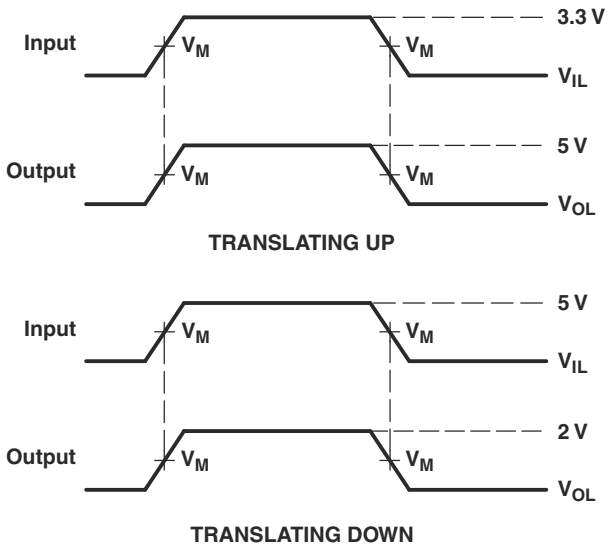


Figure 6-1. Signal Integrity (1.8 to 3.3 V Translation Up at 50 MHz)

Parameter Measurement Information



USAGE	SWITCH
Translating up	S1
Translating down	S2



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

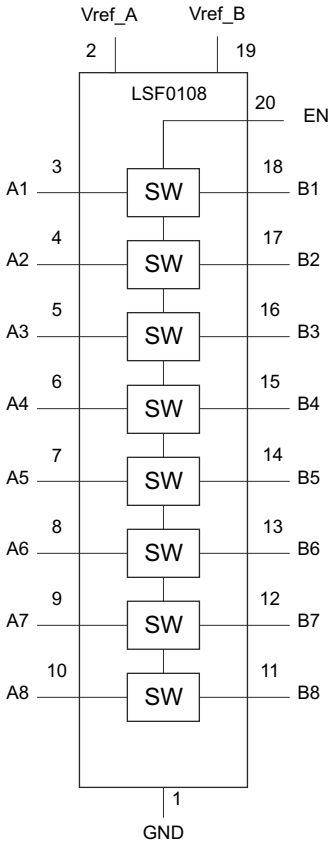
Figure 7-1. Load Circuit for Outputs

7 Detailed Description

7.1 Overview

The LSF0108-Q1 may be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The LSF0108-Q1 is ideal for use in applications where an open-drain driver is connected to the data I/Os. LSF0108-Q1 can achieve 100 MHz with appropriate pull-up resistors and layout. The LSF0108-Q1 may also be used in applications where a push-pull driver is connected to the data I/Os.

7.2 Functional Block Diagram



7.3 Feature Description

The LSF0108-Q1 are bidirectional voltage level translators operational from 0.95 to 4.5 V (Vref_A) and 1.8 to 5.5 V (Vref_B). This allows bidirectional voltage translations between 1 V and 5 V without the need for a direction pin in open-drain or push-pull applications. LSF0108-Q1 supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30-pF capacitance and 250-Ω pullup resistor.

When the An or Bn port is LOW, the switch is in the ON-state and a low resistance connection exists between the An and Bn ports. The low R_{on} of the switch allows connections to be made with minimal propagation delay and signal distortion. The voltage on the An port is limited to the voltage set by Vref_A, assuming the higher voltage is on the Bn port when the Bn port is HIGH. When the An port is HIGH, the Bn port is pulled to the drain pull-up supply voltage ($V_{pu\#}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

The supply voltage (Vpu#) for each channel can be individually set up with a pull-up resistor. For example, CH1 can be used in up-translation mode (1.2 V ↔ 3.3 V) and CH2 in down-translation mode (2.5 V ↔ 1.8 V).

When EN is HIGH, the translator switch is on and the An I/O is connected to the Bn I/O, respectively. This connection allows bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by Vref_B. EN must be LOW to ensure the high-impedance state during power-up or power-down.

7.4 Device Functional Modes

Table 7-1 shows the functional modes of the LSF devices.

Table 7-1. Function Table

INPUT EN(1) PIN	FUNCTION
H	An = Bn
L	H-Z

(1) EN is controlled by V_{ref_B} logic levels and should be at least 1 V higher than V_{ref_A} for best translator.

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LSF0108-Q1 device are able to perform voltage translation for open-drain or push-pull interface. Table 8-1 provides some consumer/telecom interfaces as reference to the different channel numbers that are supported by the LSF0108-Q1.

Table 8-1. Voltage Translator for Consumer/Telecom Interface

Part Name	Channel Number	Interface
LSF0108-Q1	8	GPIO, MDIO, SDIO, SVID, UART, SMBus, PMBus, I²C, SPI

8.2 Typical Application

8.2.1 I²C PMBus, SMBus, GPIO

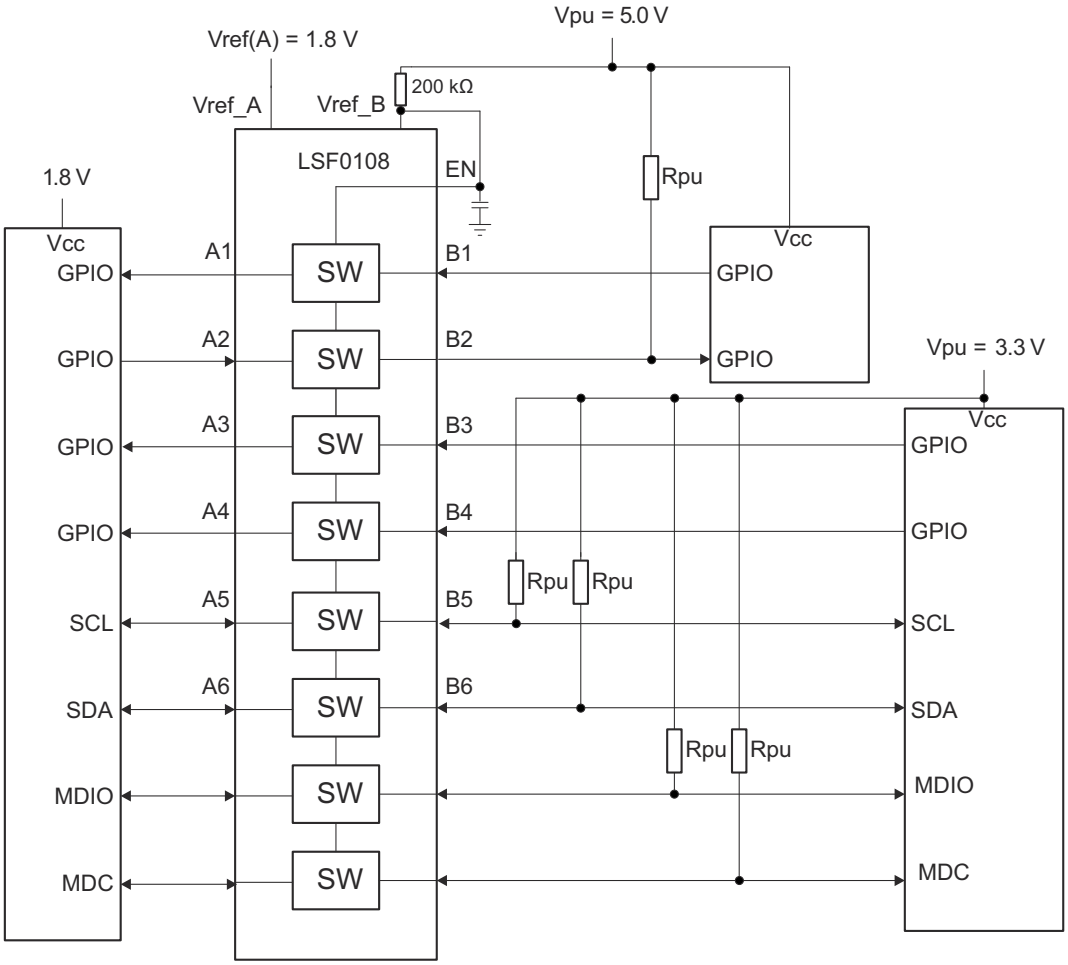


Figure 8-1. Bidirectional Translation to Multiple Voltage Levels

8.2.1.1 Design Requirements

8.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

The LSF0108-Q1 has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. The power consumption is very low because LSF0108-Q1 is a switch-type voltage translator. It is recommended to always enable LSF0108-Q1 for bidirectional application (I^2C, SMBus, PMBus, or MDIO).

Table 8-2. Application Operating Condition

PARAMETER		MIN	TYP	MAX	UNIT
Vref_A(1)	reference voltage (A)	0.95		4.5	V
Vref_B	reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	Vref_A + 0.8		5.5	V
Vpu	pull-up supply voltage	0		Vref_B	V

(1) Vref_A have to be the lowest voltage level across all of inputs and outputs.

The 200 kΩ, pull-up resistor is required to allow Vref_B to regulate the EN input. A filter capacitor on Vref_B is recommended. Also Vref_B and $V_{I(EN)}$ are recommended to be at 1.0 V higher than Vref_A for best signal integrity.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to Vref_B and both pins pulled to HIGH side Vpu through a pull-up resistor (typically 200 kΩ). This allows Vref_B to regulate the EN input. A filter capacitor on Vref_B is recommended. The controller output driver can be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

If either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

In Figure 8-1, the reference supply voltage (Vref_A) is connected to the processor core power supply voltage. When Vref_B is connected through a 200 kΩ resistor to a 3.3 V Vpu power supply, and Vref_A is set 1 V. The output of A3 and B4 has a maximum output voltage equal to Vref_A, and the bidirectional interface (Ch1/2, MDIO) has a maximum output voltage equal to Vpu.

8.2.1.2.2 Pull-Up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, to calculate the pull-up resistor value use Equation 1:

$$Rpu = (Vpu – 0.35\ V) / 0.015\ A \quad (1)$$

Table 8-3 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF0108-Q1 device at 0.175 V, although the 15 mA applies only to current flowing through the LSF0108-Q1 device.

Table 8-3. Pull-up Resistor Values

V_{DPU}	15 mA		10 mA		3 mA	
	NOMINAL (Ω)	+10%(1) (Ω)	NOMINAL (Ω)	+10%(1) (Ω)	NOMINAL (Ω)	+10%(1) (Ω)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) +10% to compensate for V_{DD} range and resistor tolerance

8.2.1.2.3 LSF0108-Q1 Bandwidth

The maximum frequency of the LSF0108-Q1 is dependent on the application. The device can operate at speeds of >100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application. The LSF0108-Q1 behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

Figure 8-2 shows a bandwidth measurement of the LSF0108-Q1 using a two-port network analyzer.

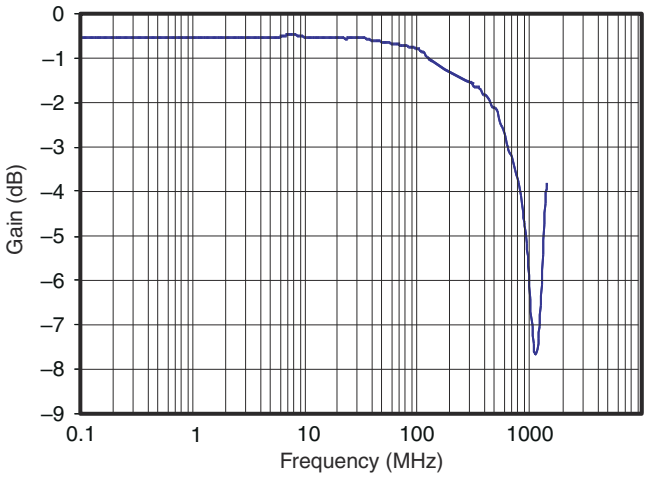


Figure 8-2. 3-dB Bandwidth

The 3-dB point of the LSF0108-Q1 is ≈ 600 MHz; however, this measurement is an analog type of measurement. For digital applications the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the LSF0108-Q1, a digital clock frequency of greater than 100 MHz can be achieved.

The LSF0108-Q1 does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pull-up resistor is needed on the host side (3.3 V) if the LSF0108-Q1 is being driven by standard CMOS totem pole output driver. Ideally, it is best to minimize the trace length from the LSF0108-Q1 on the sink side (1.8 V) to minimize signal degradation.

All fast edges have an infinite spectrum of frequency components; however, there is an inflection (or knee) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate the maximum practical frequency component, or the knee frequency (f_{knee}), use Equation 2 and Equation 3:

$$f_{knee} = 0.5 / RT\ (10 – 80\%) \quad (2)$$

$$f_{knee} = 0.4 / RT\ (20 – 80\%) \quad (3)$$

For signals with rise time characteristics based on 10% to 90% thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20% to 80% thresholds, which is very common in many of today's device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the LSF0108-Q1 close to the I^2C output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pull-up resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

8.2.1.3 Application Curves

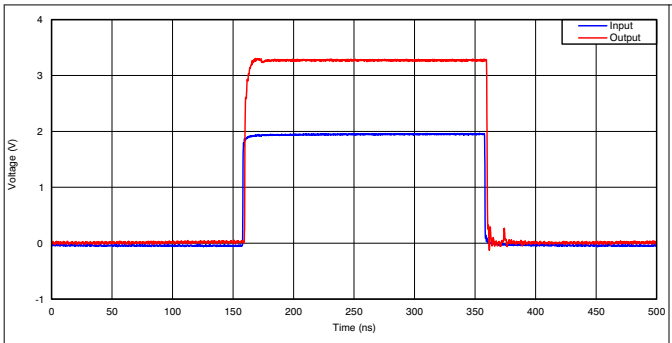


Figure 8-3. Captured Waveform From Above I^2C Set-Up (1.8 V to 3.3 V at 2.5 MHz)

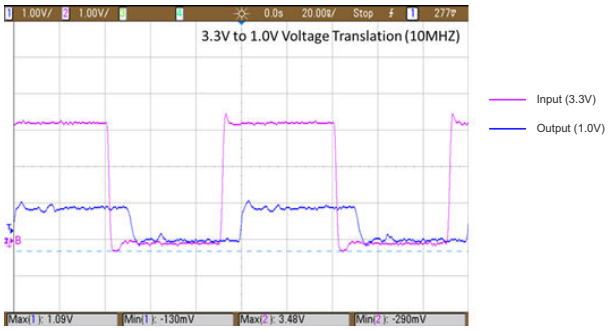
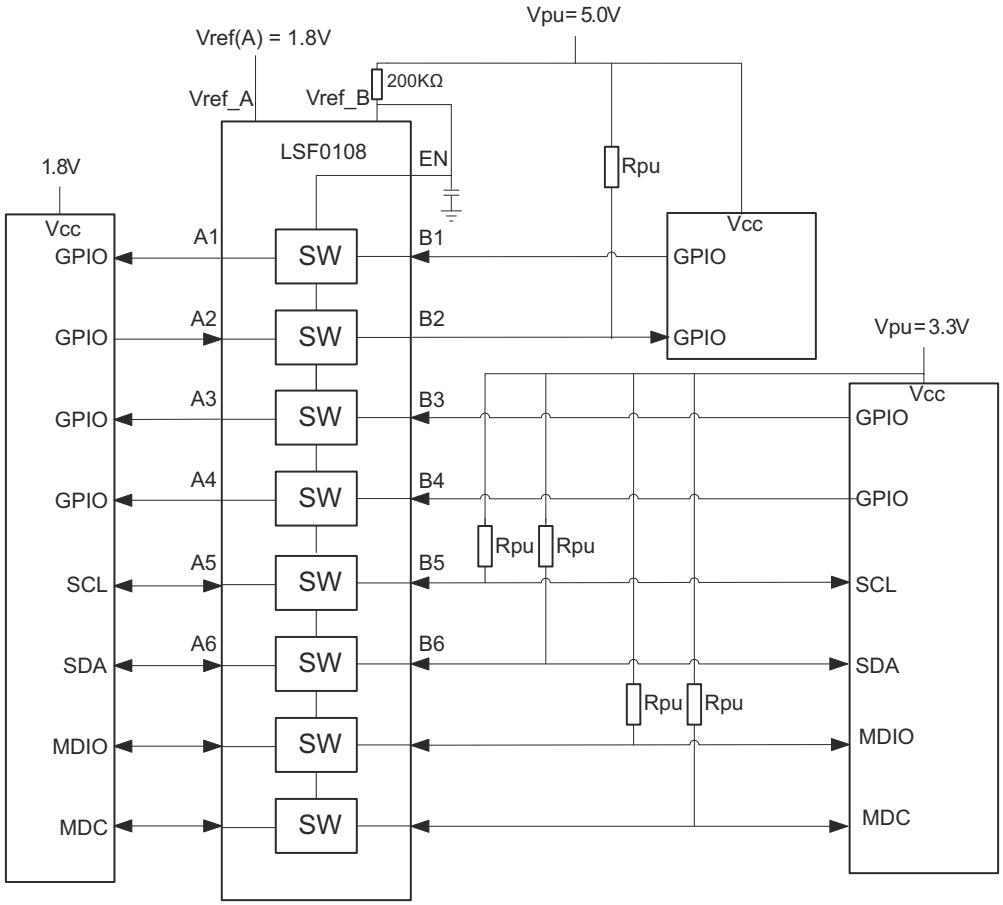


Figure 8-4. Captured Waveform From Above MDIO Setup

8.2.2 Multiple Voltage Translation in Single Device



8.2.2.1 Design Requirements

Refer to *Section 8.2.1.1*.

8.2.2.2 Detailed Design Procedure

Refer to *Section 8.2.1.2*.

8.2.2.3 Application Curve

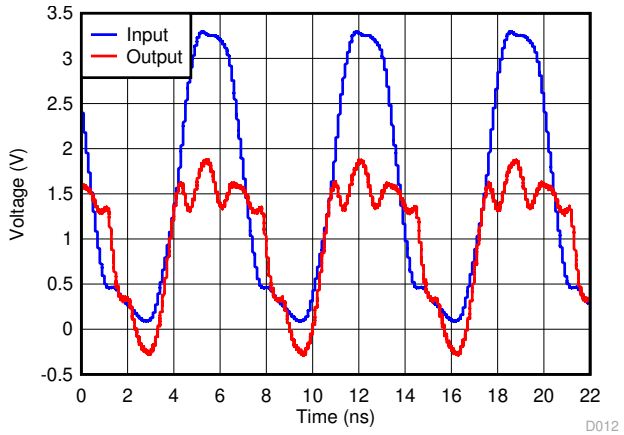


Figure 8-5. Translation Down (3.3 to 1.8 V) at 150 MHz

9 Power Supply Recommendations

There are no power sequence requirements for the LSF0108-Q1. For enable and reference voltage guidelines, please refer to the *Section 8.2.1.1.1*.

10 Layout

10.1 Layout Guidelines

Because the LSF0108-Q1 is a switch-type level translator, the signal integrity is highly related with a pull-up resistor and PCB capacitance condition.

- Short signal trace as possible to reduce capacitance and minimize stub from pull-up resistor.
- Place LSF close to high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of transmitter.

10.2 Layout Example

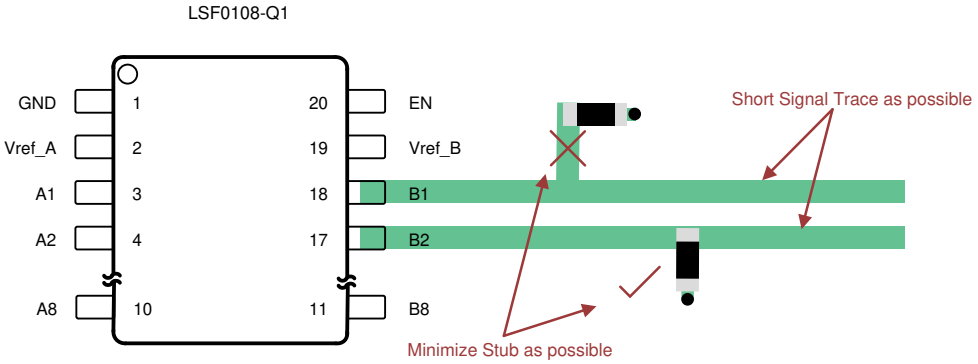


Figure 10-1. Short Trace Layout

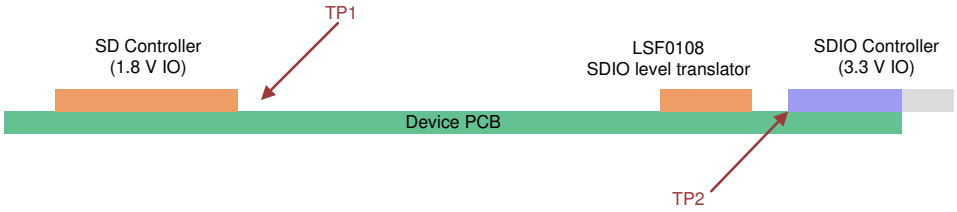


Figure 10-2. Device Placement

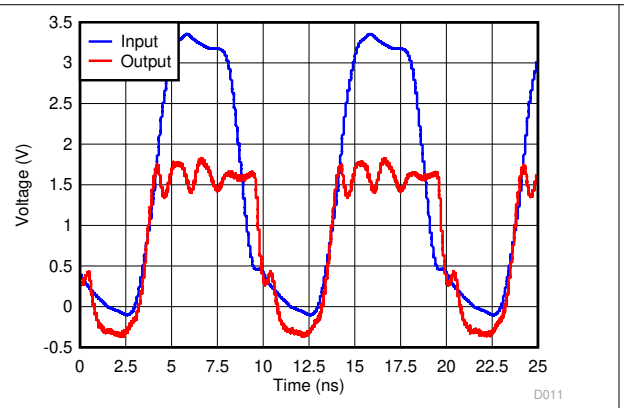


Figure 10-3. Waveform From TP1 (Pull-Up Resistor: 160-Ω and 50-pF Capacitance 3.3 V to 1.8 V at 100 MHz)

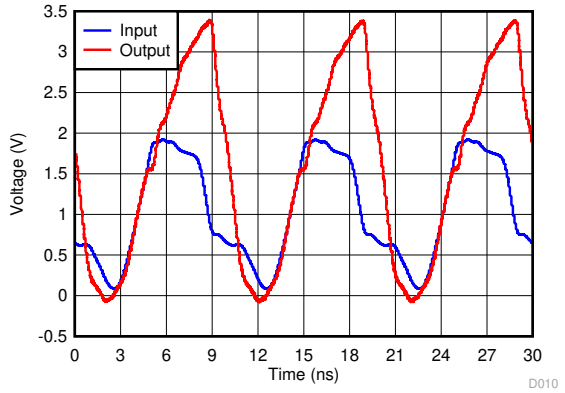


Figure 10-4. Waveform From TP2 (Pull-Up Resistor: 160-Ω and 50-pF Capacitance 1.8 V to 3.3 V at 100 MHz)

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0108QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LSF0108Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LSF0108-Q1 :

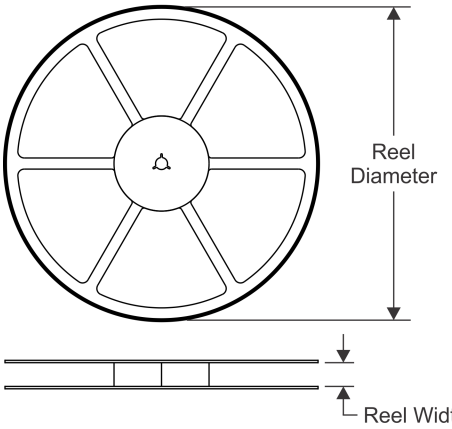
- Catalog : LSF0108

NOTE: Qualified Version Definitions:

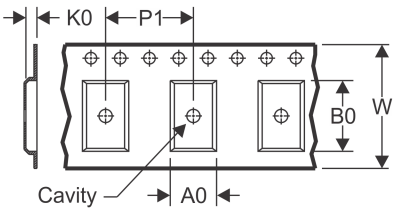
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

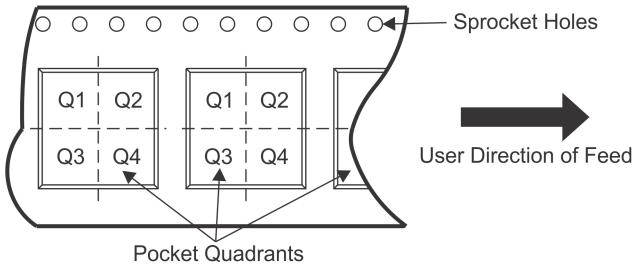


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

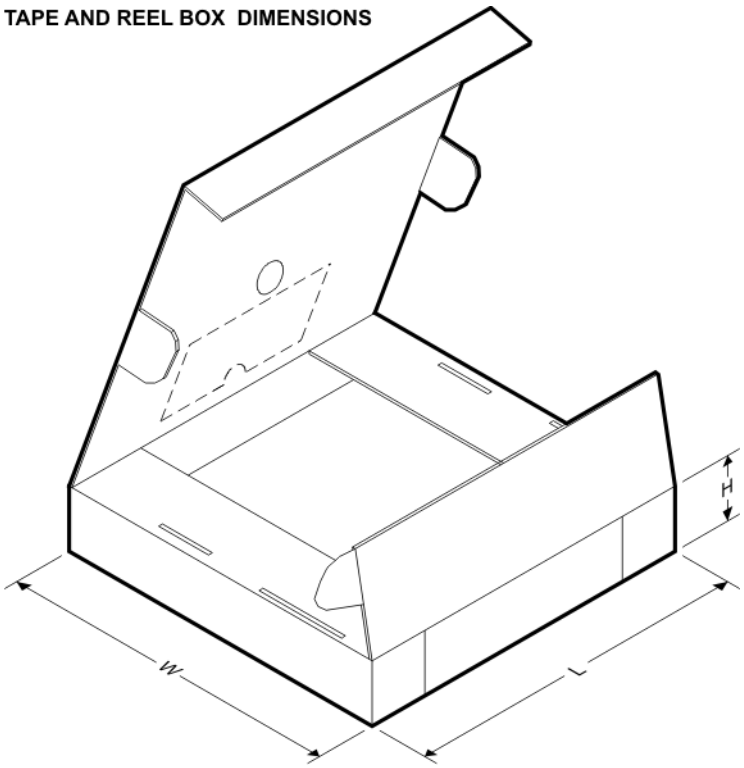
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LSF0108QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

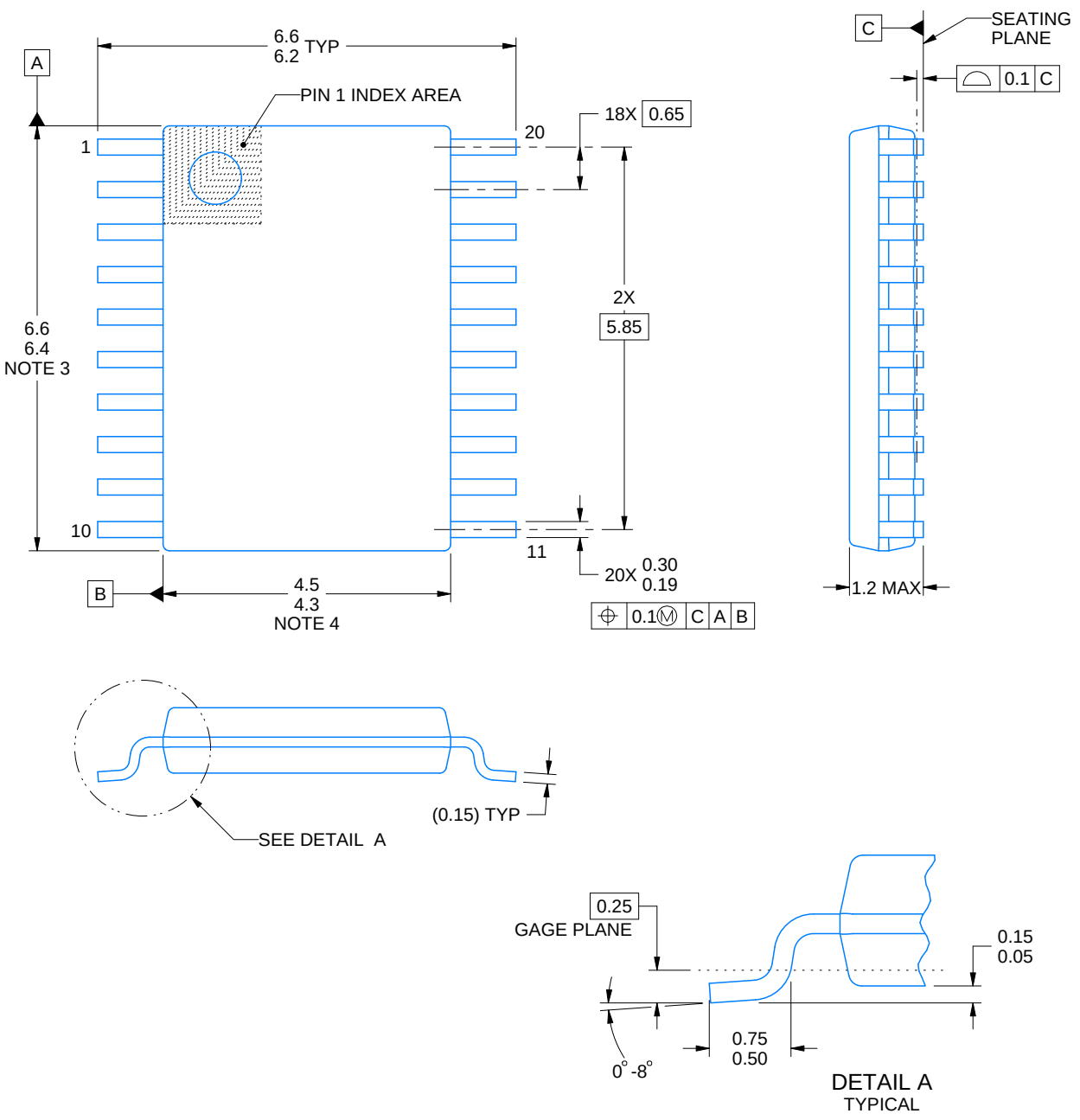
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LSF0108QPWRQ1	TSSOP	PW	20	2000	364.0	364.0	27.0

PACKAGE OUTLINE

PW0020A

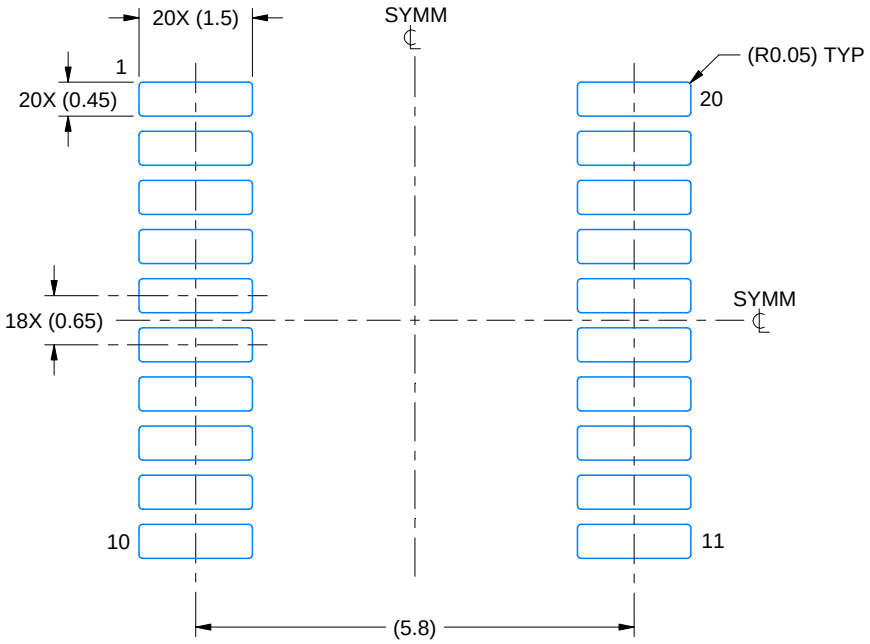
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



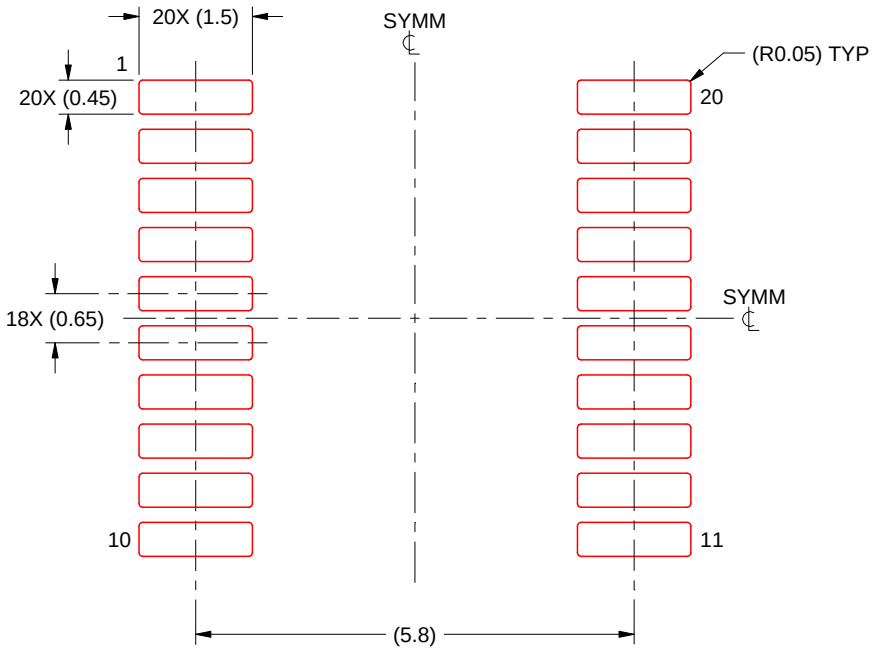
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



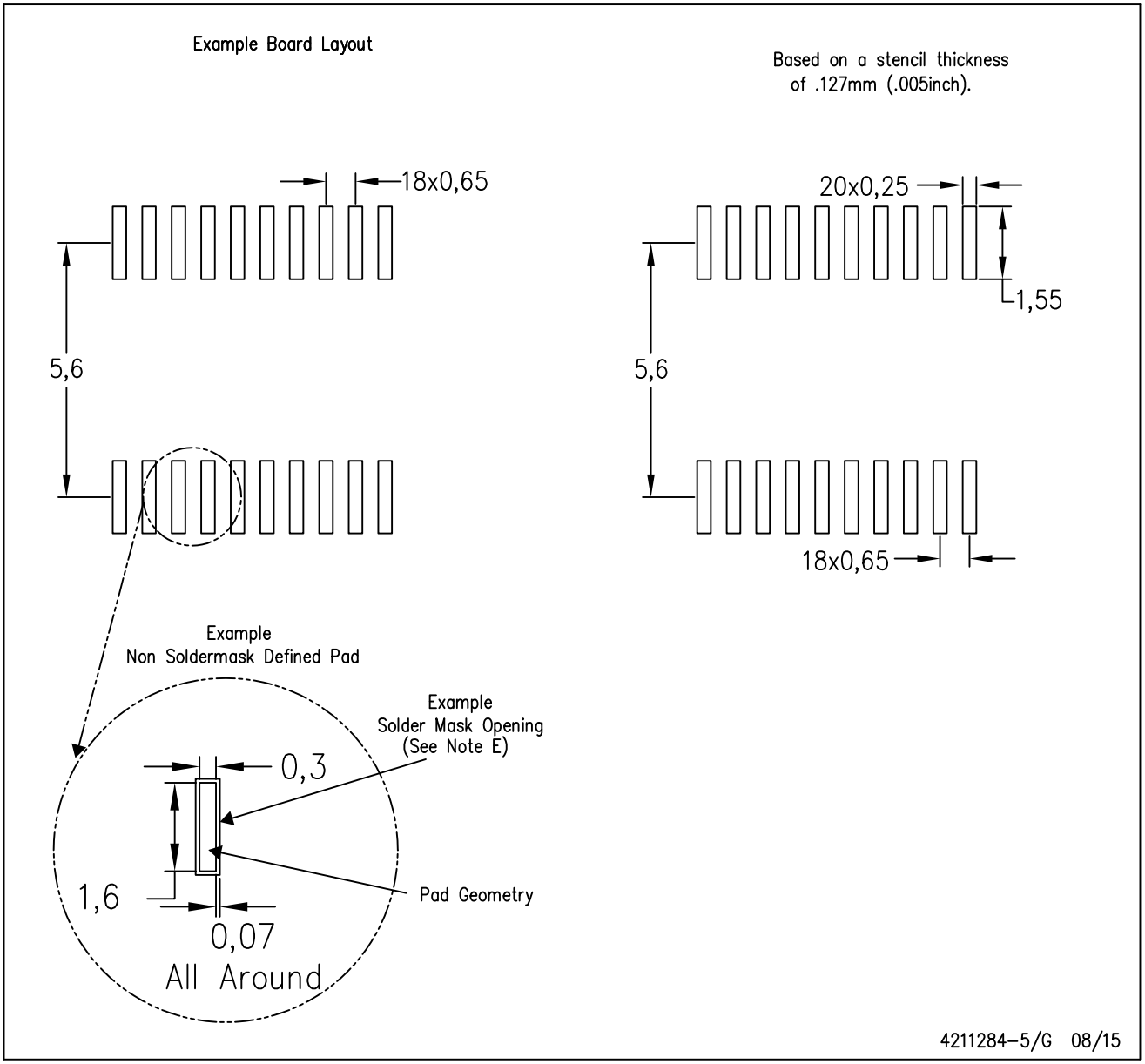
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265