

# ICL5102 PFC + Resonant Half-Bridge Controller for LED Drivers

## 2nd Generation

### Datasheet

Rev 1.31

### Features

- Integrated two stage combination controller allows for reduced number of external components, optimizes Bill of Materials (BOM) and form factor.
- PFC controller with Critical Conduction Mode (CrCM) + Discontinuous Conduction Mode (DCM)
- Resonant Half-Bridge (HB) controller with fixed or variable switching frequency control
- Maximum 500 KHz HB switching frequency and soft-start frequency up to 1.3 MHz
- Resonant HB Burst Mode (BM) ensures power limitation and low standby power < 300mW.
- Supports universal AC input voltage (90 to 305 V<sub>rms</sub>) nominal
- Excellent system efficiency up to 94%
- THD optimization ensures Low harmonic distortion (Total Harmonic Distortion (THD) < 5%) down to 30% nominal load.
- Integrated High Side MOSFET driver
- Small DSO-16 package

Comprehensive set of protection features with auto-restart reaction:

- Input brown-out protection
- PFC bus over-voltage protection
- PFC over-current protection
- Output over-voltage protection (OVP)
- Output over-current/short circuit protection (OCP)
- Output over-power/over-load protection (OPP)
- Capacitive mode protection
- External over-temperature protection (OTP)

### Potential applications

- Offline LED Drivers for commercial and industrial lighting up to 350 W
- High density AC/DC power supply

### Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Product Type	Package
ICL5102	PG-DSO-16

**Description**

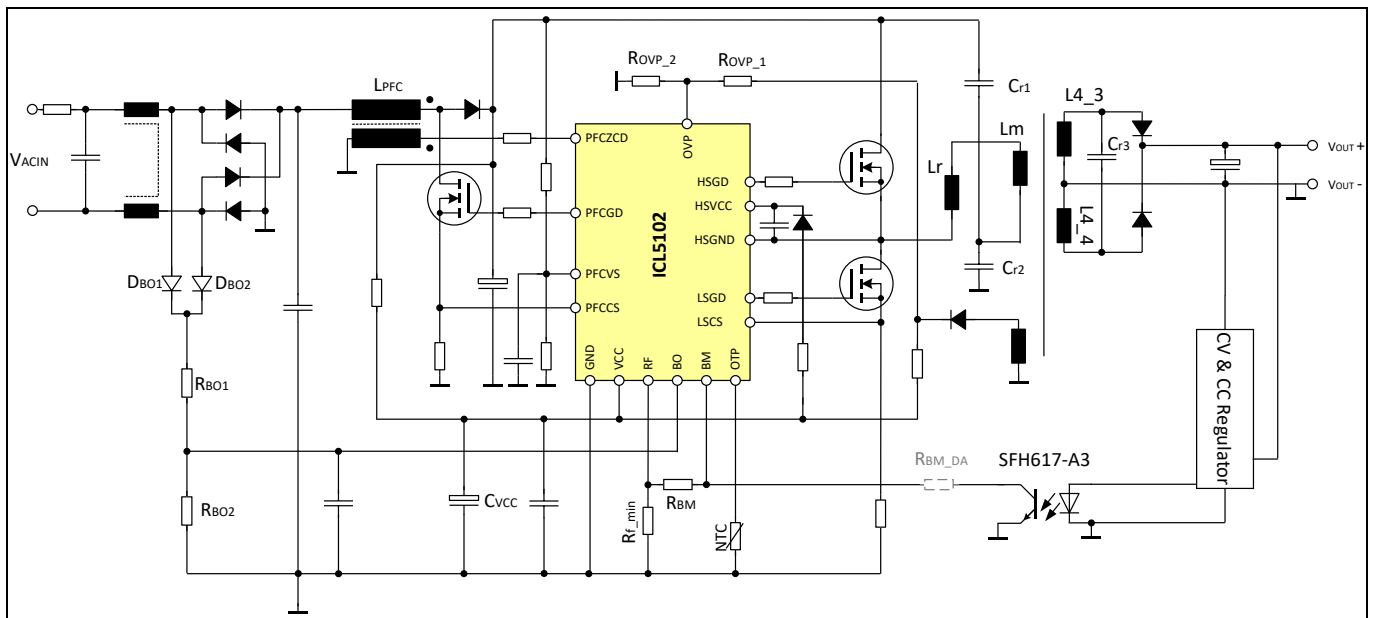
The ICL5102 is a highly integrated multi-mode (CrCM and DCM) PFC and resonant HB combination controller. The integration of PFC and HB into a single controller enables reduction of external components and optimizes performance by harmonized operation of the two stages.

The two-stage approach divides the PFC responsibilities from the output current regulations functions. This ensures low variation in the output voltage and current and allows for low THD, high power factor and a greater ability to withstand AC line perturbations. The multi-mode operation of PFC converter provides excellent efficiency over the whole load range.

Resonant HB converter supports both LLC and LCC topologies with fixed or variable switching frequency control for highest efficiency and the BM enables the low standby power consumption.

A comprehensive set of protection features with auto-restart ensures the highest safety and reliability of the components and overall system.

The following Figure shows a typical LED driver application using ICL5102 with PFC+LCC topology:



**Figure 1 ICL5102 Typical Application with PFC+LCC Topology**

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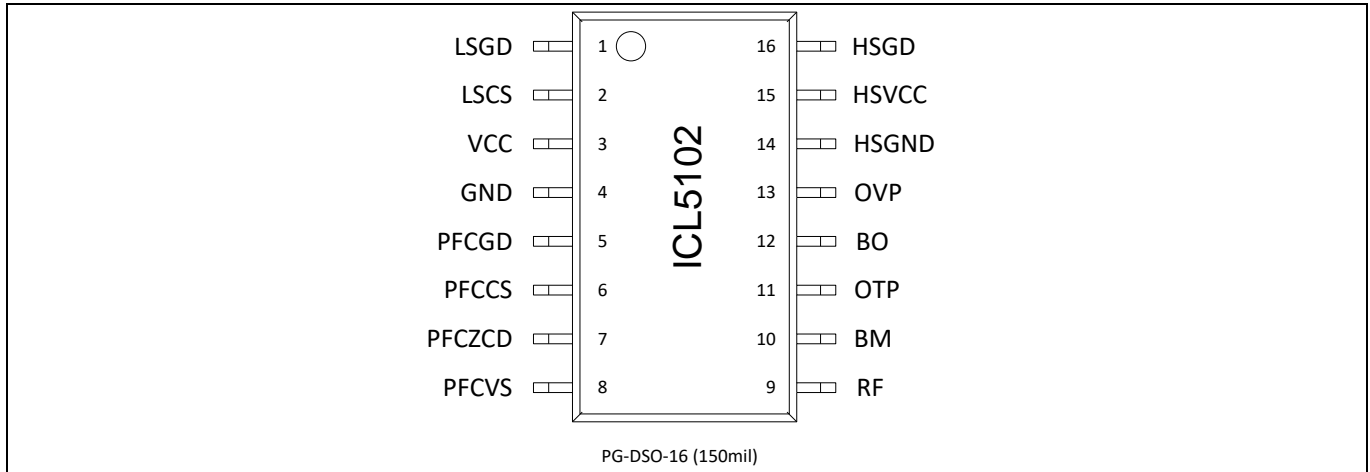
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## 1 Pin Configuration and Description

ICL5102 pin assignments and basic pin description are shown below in the [Figure 2](#) and [Table 1](#).



**Figure 2 Pinning of ICL5102**

**Table 1 Pin Definitions and Functions**

Name	Pin	Type	Function
LSGD	1	O	<b>HB low side gate driver</b> Output for directly driving the HB low side MOSFET via a resistor
LSCS	2	I	<b>HB current sense</b> Connected to an external shunt resistor and the source of the HB low side MOSFET
VCC	3	I	<b>Positive power supply</b> IC power supply
GND	4	-	<b>Ground</b> IC Ground
PFCGD	5	O	<b>PFC gate driver</b> Output for directly driving the PFC MOSFET via a resistor
PFCCS	6	I	<b>PFC current sense</b> Connected to an external shunt resistor and the source of the PFC MOSFET
PFCZCD	7	I	<b>PFC zero-crossing detection</b> Connected to the PFC auxiliary winding via a resistor for PFC inductor current zero-crossing detection
PFCVS	8	I	<b>PFC bus voltage sense</b> Connected to a high impedance resistor divider from the PFC controller output for bus voltage sensing
RF	9	I	<b>HB minimum switching frequency setting</b> Connected via an external resistor to GND for HB minimum switching frequency setting
BM	10	I	<b>Burst Mode (BM) enter/exit switching frequency setting</b> Connected to an opto-coupler and to the RF pin with an external resistor for BM enter/exit setting

# ICL5102 PFC + Resonant Half-Bridge Controller

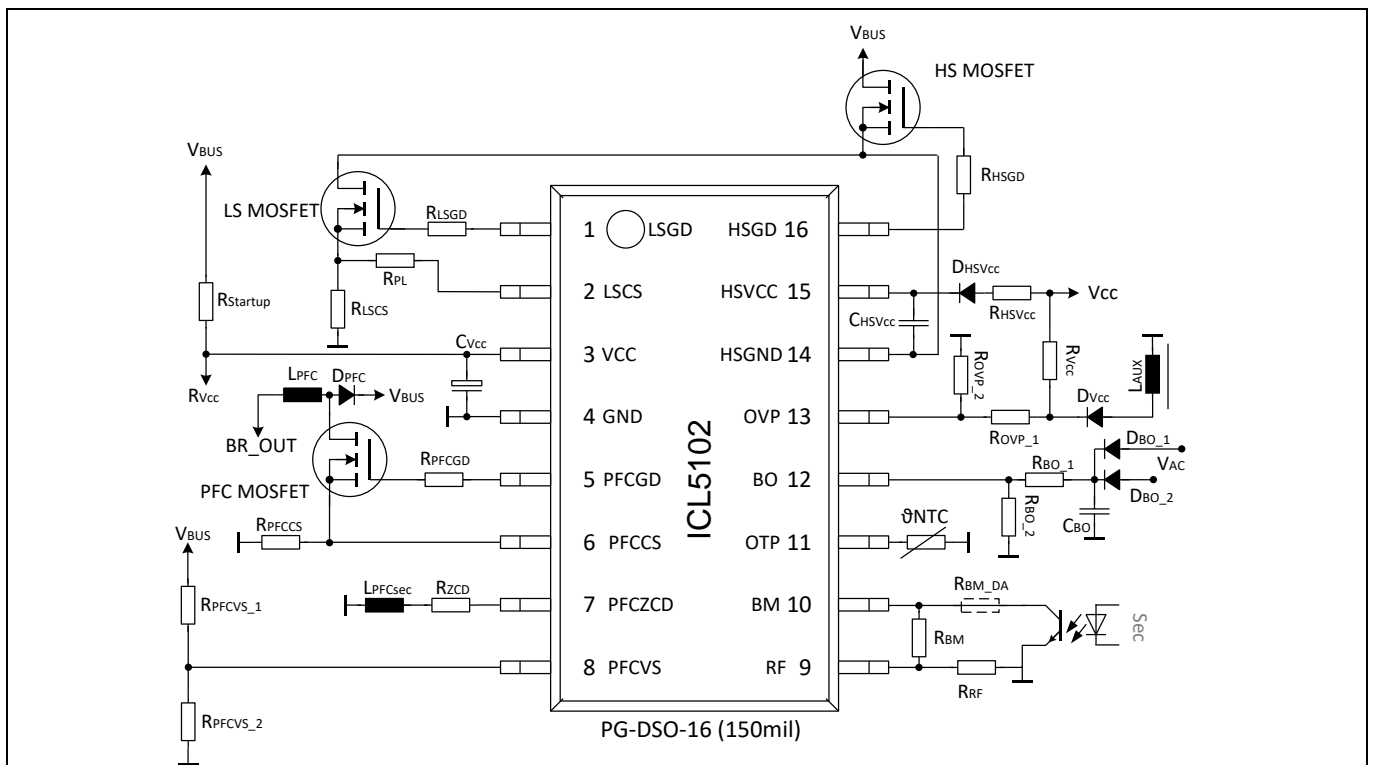
## 2nd Generation



### Pin Configuration and Description

Name	Pin	Type	Function
OTP	11	I	<b>Over Temperature Protection (OTP)</b> Connected to an external Negative Temperature Coefficient thermistor (NTC) for external over temperature protection
BO	12	I	<b>Brown in/out detection</b> Connected to the rectified input voltage via an external resistor for input brown in/out detection
OVP	13	I	<b>Output Over Voltage Protection (OVP)</b> Connected to the HB auxiliary winding via a resistor divider and diode for OVP of the secondary output voltage
HSGND	14	-	<b>High side ground</b> Ground for floating high side driver of HB
HSVCC	15	I	<b>High side VCC power supply</b> Power supply of the high side floating driver of HB, supplied via bootstrap circuit
HSGD	16	O	<b>High side floating gate driver</b> Output for directly driving the HB floating high side MOSFET via a resistor.

The ICL5102 pin connection schematic is shown in the following **Figure 3**:



**Figure 3 ICL5102 Pin Connection**

## 2 Functional Block Diagram

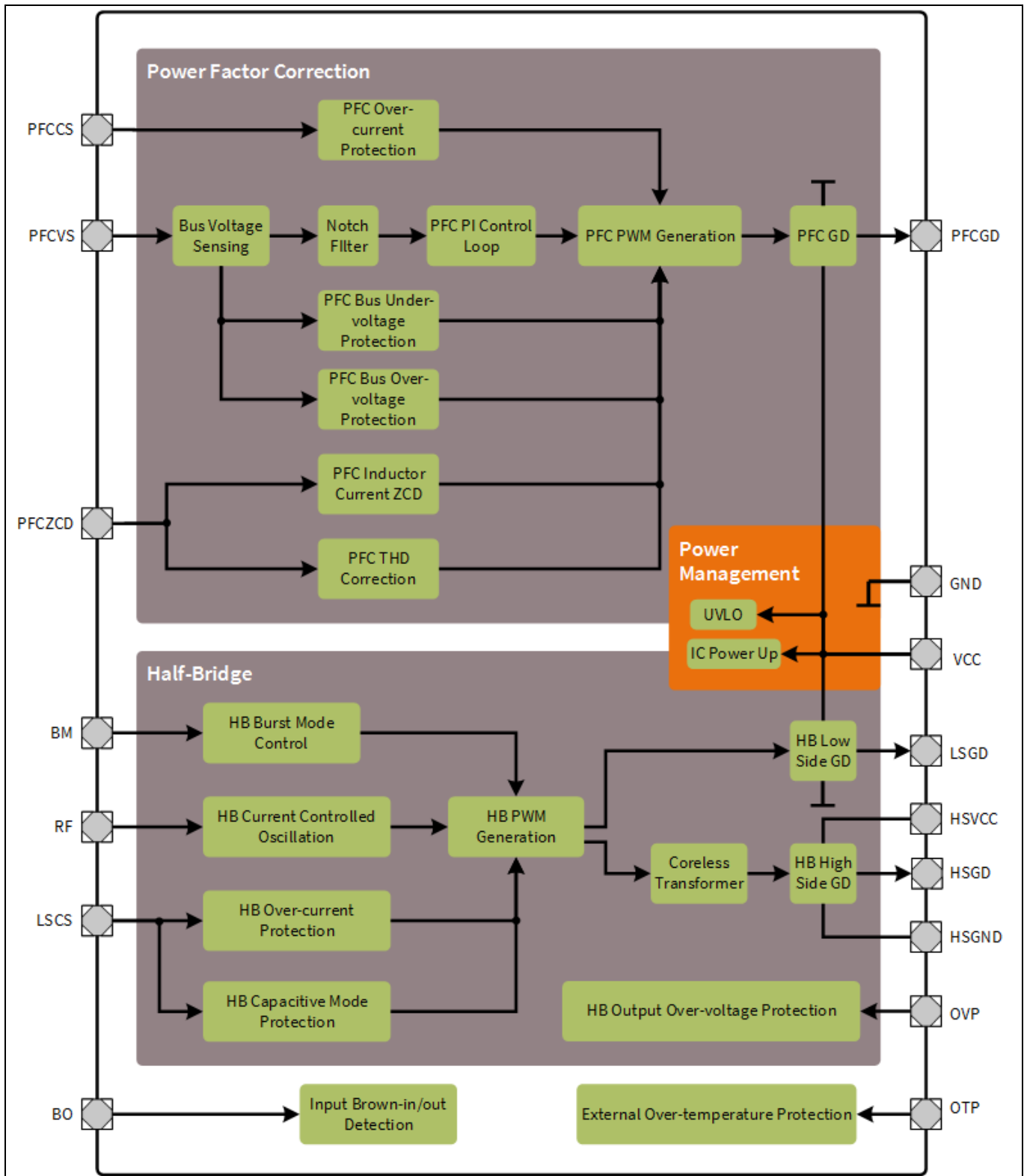


Figure 4 ICL5102 Functional Block Diagram

## 3 Functional Description

Functional description section provides an overview of the integrated functions. It includes:

- ICL5102 power up
- Multi-mode PFC controller
- Resonant HB controller

The parameters and equations are based on typical values at  $T_A = 25\text{ °C}$ . The correlated minimum and maximum values are shown in the electrical characteristics in chapter 5.

### 3.1 IC Power Up

ICL5102 has four power supply pins: VCC, GND, HSVCC and HSGND:

- Normal start-up operation of ICL5102 requires a positive voltage at pin VCC higher than the turn-on threshold  $V_{CC\_on}$ . After the ICL5102 is active, the Vcc voltage should remain between the  $V_{CC\_on}$  and  $V_{CC\_off}$ . Once the voltage drops below  $V_{CC\_off}$ , under-voltage lock out (UVLO) will occur and IC operation is disabled.
- HSVCC and HSGND power pins are the power supply for the integrated floating high side driver, usually derived using an external boot strap circuit. The high side driver is active after the voltage between pin HSVCC and HSGND is higher than the turn-on threshold  $V_{HSVCC\_on}$ . Once this voltage drops below  $V_{HSVCC\_off}$  in the normal operation, the high side driver is disabled.

### 3.2 Multi-Mode PFC Controller

The PFC controller ensures high power quality by maximizing the power factor (PF) and minimizing Total Harmonic Distortion (THD). It is designed in a boost topology to provide a constant high DC voltage for the HB controller.

#### 3.2.1 Control Scheme

During normal to heavy load conditions, PFC bus voltage regulation is achieved using CrCM with a constant on-time control. The PFC MOSFET on-time is proportional to the PFC output power and determined by the PFC choke inductance  $L_{PFC}$ , the input voltage  $V_{in\_rms}$ , the applied PFC load  $P_{O\_PFC}$  and the PFC converter efficiency  $\eta_{PFC}$ . This is given by:

$$t_{on\_PFC} = \frac{2 * P_{O\_PFC} * L_{PFC}}{V_{in\_rms}^2 * \eta_{PFC}}$$

ICL5102 PFC controller has an integrated PI compensator which calculates the PFC on-time according to the error between the value at PFCVS pin and the reference value  $V_{PFC\_ref} = 2.5\text{ V}$ . A notch filter before the compensator filters out the double AC line frequency ripple in the bus voltage and stabilizes the controller loop.

To support light load condition, DCM is implemented for efficient operation.

#### 3.2.1.1 PFC Soft-start

After the voltage at pin VCC is higher than the threshold  $V_{CC\_on}$ , PFC controller will initiate a soft-start to minimize the stress on the input filter, PFC MOSFET, PFC choke and diode when the following conditions are fulfilled:

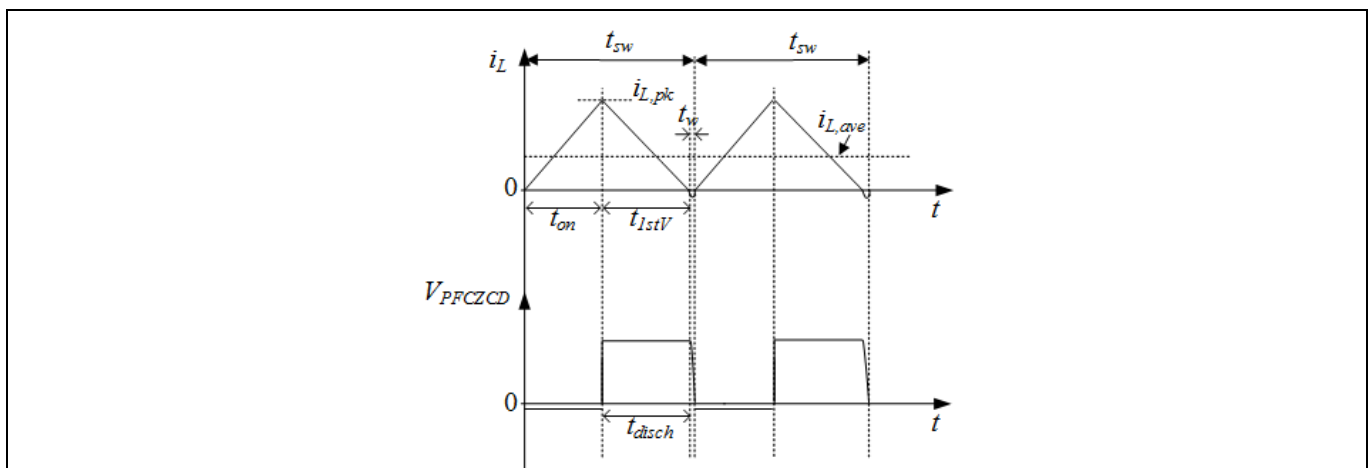
### Functional Description

- Brown-in: the voltage at Brown-Out pin (BO) must be higher than  $V_{BO\_in} = 1.4 \text{ V}$
- PFC open-loop not detected: the voltage at pin PFCVS must be higher than  $V_{PFCVSUV2} = 12.5\% \cdot V_{PFC\_ref} = 0.31 \text{ V}$
- PFC output over-voltage not detected: the voltage at pin PFCVS must be lower than  $V_{PFCVSUV2} = 105\% \cdot V_{PFC\_ref} = 2.63 \text{ V}$
- Other protections (e.g. OTP or OVP) not present

ICL5102 PFC soft-start is implemented by increasing PFC MOSFET on-time from  $t_{PFC\_on\_initial}$  to  $t_{PFC\_on\_max} = 22 \text{ us}$  every 280 us. The initial PFC on-time  $t_{PFC\_on\_initial}$  is dependent on the input voltage sensed at the BO pin. Once the voltage at pin PFCVS reaches the threshold  $V_{PFC\_UV2} = 95\% \cdot V_{PFC\_ref} = 2.375 \text{ V}$ , soft-start is completed. At this time normal operation on-time control takes place via the integrated PI compensator.

### 3.2.1.2 PFC Multi-Mode Control

During CrCM operation of the PFC, the PFC MOSFET is turned on with a constant on-time throughout the complete AC half cycle and the off-time is varying depending on the instantaneous value of the input AC voltage amplitude. Therefore, the switching frequency is changing within each AC half cycle with the lowest switching frequency at the peak of the AC input voltage and the highest switching frequency near the zero-crossings. As shown in the **Figure 5**, a new switching cycle starts with a tiny delay after the inductor current reaches zero.

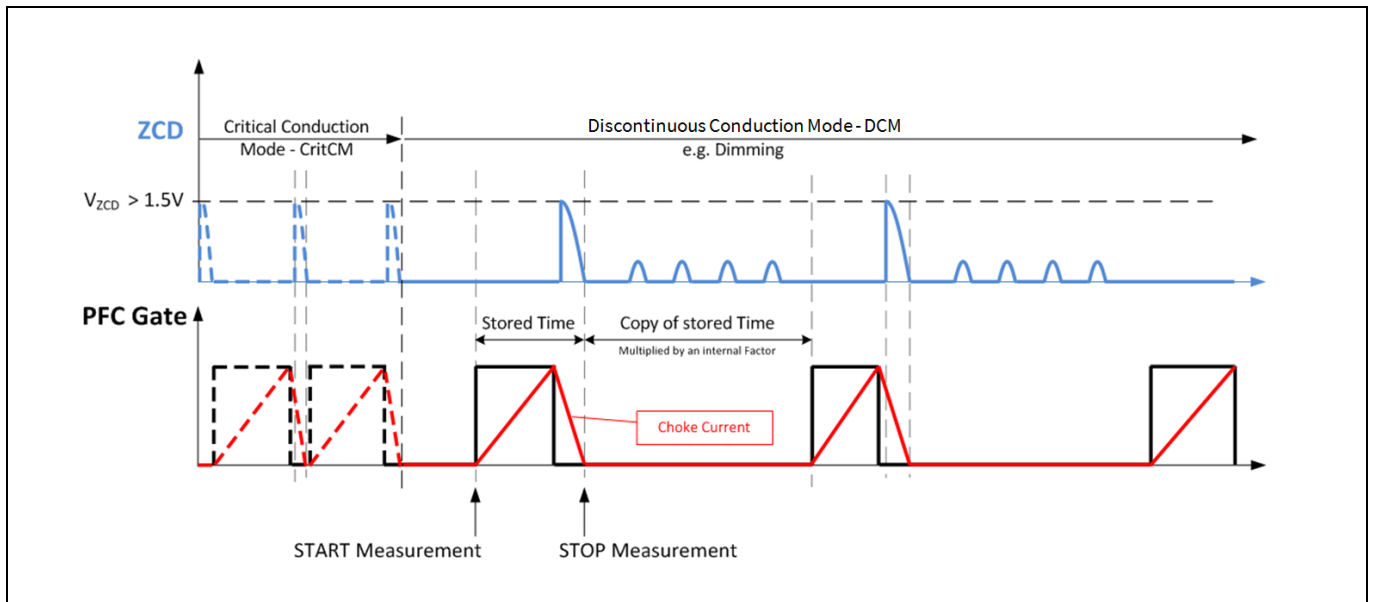


**Figure 5** Switching Cycle of ICL5102 Critical Conduction Mode PFC

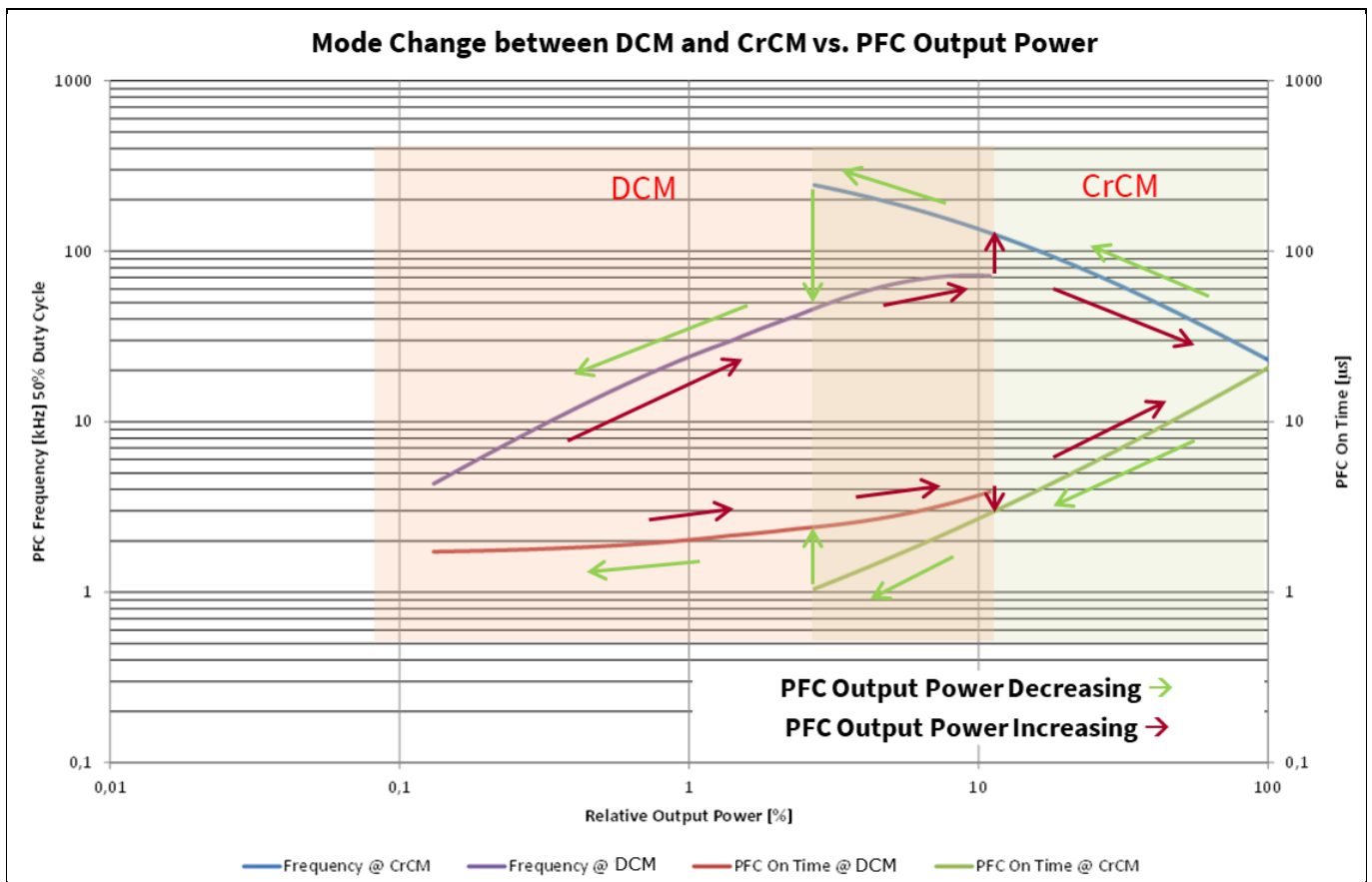
PFC CrCM is ideal for full and heavy load conditions, where the constant on-time is large. As load decreases and/or the input AC input peak voltage increases towards the magnitude of the PFC output bus voltage, on-times reduces (switching frequency increases), and PFC switching losses increase. This results in poor efficiency at light load and/or high AC line conditions.

To help minimize switching losses during this condition and to optimize light load efficiency, the ICL5102 PFC controller switches from CrCM to DCM mode. This transition occurs once the PFC MOSFET on-time reduces below 1 us. In DCM operation, the switching frequency can be further reduced by skipping switching cycles once the PFC inductor current reaches zero. As shown in the **Figure 6**, the inserted delay is the switching time (from PFC gate on until the PFC inductor current decreases to zero) multiplied with an internal factor. Once the PFC on-time increases to 4 us in the DCM operation, ICL5102 will switch back to CrCM. The transferred power is regulated both in CrCM and DCM operation. The on-time hysteresis between the two modes (overlapped area) ensures the smooth mode change as shown in the **Figure 7**.





**Figure 6** ICL5102 PFC Mode Change from CrCM to DCM



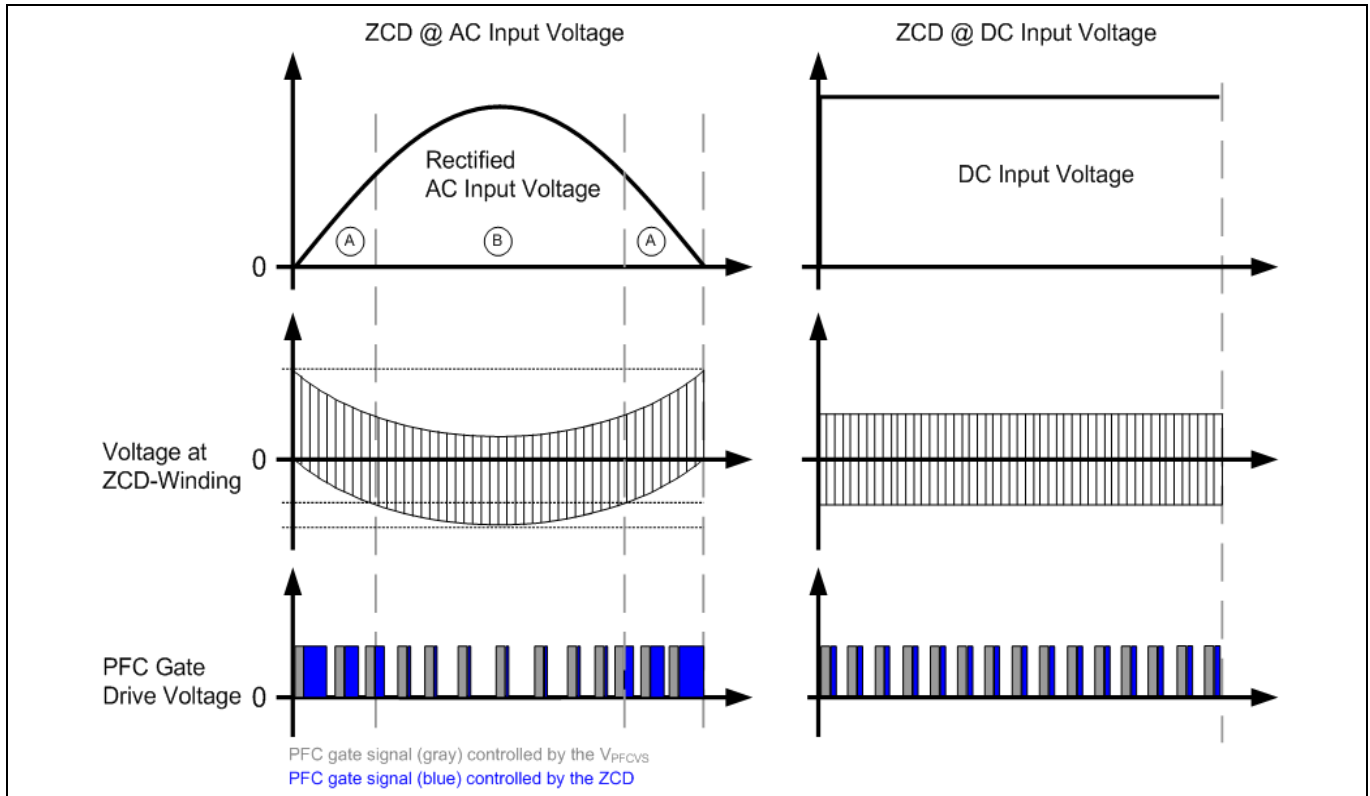
**Figure 7** ICL5102 Operating Frequency and On-Time in CrCM and DCM

### 3.2.1.3 PFC THD Correction

The input AC current becomes most distorted in the area when zero-crossings of AC input voltage occurs. In order to ensure the sinusoidal current waveform in this area, the ICL5102 extends the PFC on-time dynamically up to two times of PFC maximum on-time according to the instantaneous value of the input voltage amplitude. The

### Functional Description

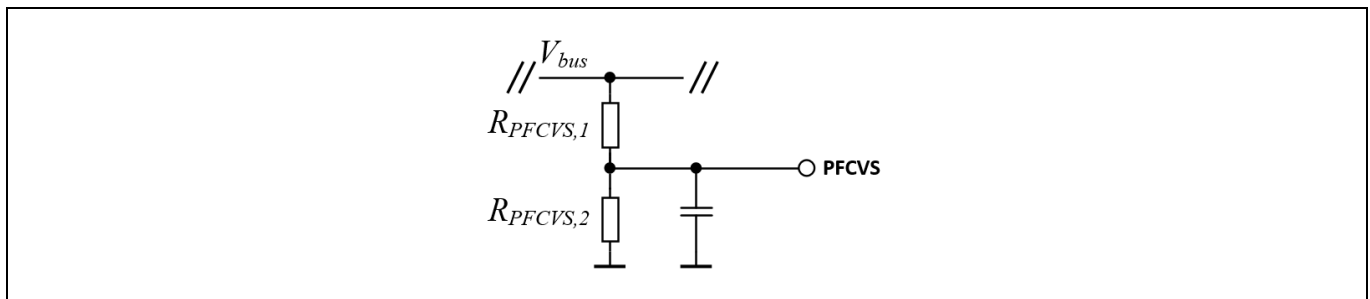
detection of AC input voltage zero-crossings is realized through the PFC auxiliary winding. When the voltage across the PFC auxiliary winding after PFC MOSFET turns-off reaches the maximum value, AC zero-crossings is detected. The concept of THD correction is shown in the following **Figure 8**.



**Figure 8 PFC THD Correction**

### 3.2.2 PFC Bus voltage Sensing

The PFC output bus voltage is scaled down using a resistor divider and sensed at the pin PFCVS pin as shown in the **Figure 9**. A good quality ceramic filter capacitor should be placed as close as possible at the pin to filter any high frequency switching noise. This filter capacitor ensures no false PFC bus voltage protections are triggered due to noise perturbations.



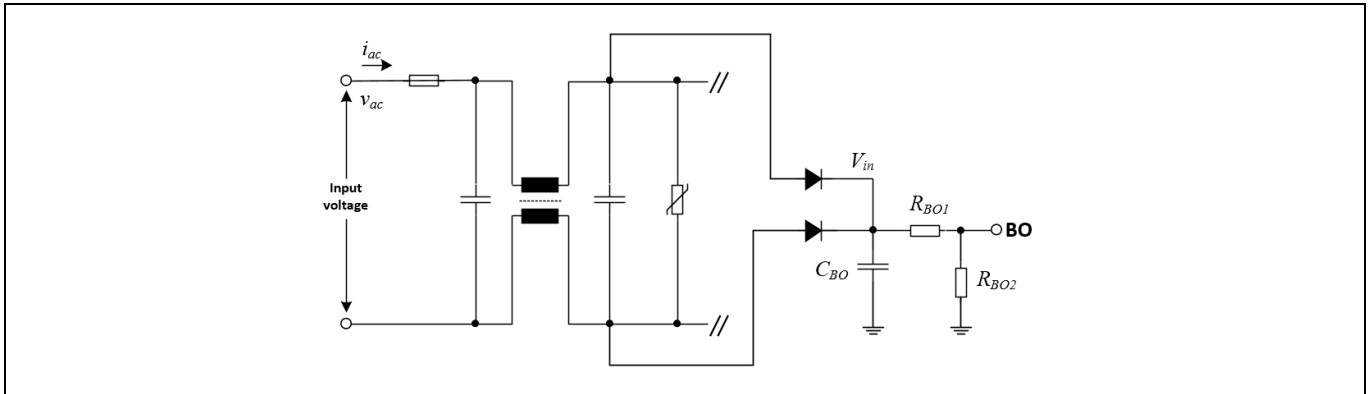
**Figure 9 ICL5102 PFC Bus Voltage Sensing**

### 3.2.3 Input voltage sensing

As shown in the **Figure 10**, the AC input voltage is sensed at the BO pin with a resistor divider which scales down the full wave rectified AC line voltage. A smooth capacitor  $C_{BO}$  with a high ohmic resistor  $R_{BO1}$  are strongly recommended direct after the full wave rectifier diodes so that the peak value of AC input voltage is sensed. As

### Functional Description

the peak value of AC input voltage is not distorted when the input current is near zero (e.g. in case of brown-out) compared to the RMS value.



**Figure 10 ICL5102 Input Voltage Sensing**

The voltage at the BO pin which represents the peak voltage of the AC input has feed-forward control on the PFC converter.

- It decides the initial on-time of the initial PFC soft-start.
- In the light load condition, the PFC on-time is dependent on the input voltage.

The brown-in and brown-out are implemented by sensing the voltage at BO pin. The conditions are defined as following:

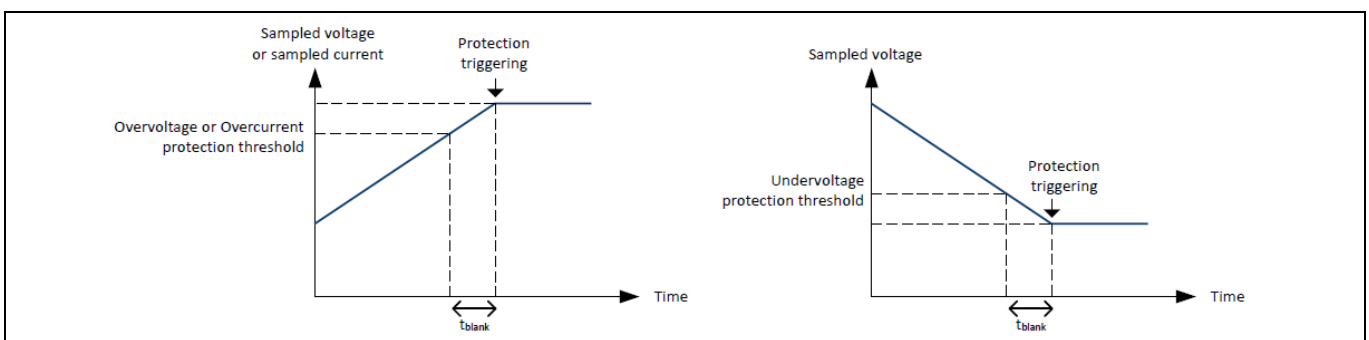
- Brown-in: the voltage at pin BO is higher than  $V_{BO\_in} = 1.4 \text{ V}$ .
- Brown-out: the voltage at pin BO is lower than  $V_{BO\_out} = 1.2 \text{ V}$  in the normal operation.

### 3.2.4 PFC Inductor Peak Current limitation

The PFC inductor peak current through the PFC MOSFET is monitored via the PFC shunt resistor  $R_{PFCCS}$  to limit the maximum power through the PFC inductor, MOSFET and the freewheeling diode. Once the voltage across the shunt resistor exceeds the over-current threshold  $V_{PFC\_OCP1} = 1.0 \text{ V}$  for longer than the blanking time (including propagation delay)  $t_{PFC\_OCP1\_blanking} = 200 \text{ ns}$ , the PFC MOSFET is turned off immediately. The next PFC switching cycle will be initialized on either PFC ZCD or maximum period time out. This peak current limitation is active in every switching cycle.

### 3.2.5 PFC Protection features

Protections features are triggered if fault conditions are present longer than the blanking time. The controller may continue operation after exceeding protection threshold because of blanking time as shown in **Figure 11**.



**Figure 11 Excess of threshold due to Blanking Time**

#### 3.2.5.1 PFC Bus Under-voltage Protection

PFC bus under-voltage is monitored at the PFCVS pin.

In the normal operation, the PFCVS pin voltage is sensed and compared to the under-voltage threshold  $V_{PFC\_UV1} = 75\% * V_{PFC\_ref} = 1.88 \text{ V}$ . Once the pin voltage is below this threshold for longer than the blanking time, PFC stops switching and ICL5102 will enter auto-restart.

#### 3.2.5.2 PFC Bus Over-voltage Protection Level 1

PFC bus over-voltage level 1 is monitored at the PFCVS pin.

The PFCVS pin voltage is sensed and compared to the over-voltage threshold  $V_{PFC\_OV1} = 109\% * V_{PFC\_ref} = 2.73 \text{ V}$ . Once the pin voltage is above this threshold, PFC will stop switching within 5 us. As long as the pin voltage drops below  $V_{PFC\_OV} = 105\% * V_{PFC\_ref} = 2.63 \text{ V}$ , PFC resumes operation.

#### 3.2.5.3 PFC Bus Over-voltage Protection Level 2

PFC bus over-voltage level 2 is monitored at the PFCVS pin.

The PFCVS pin voltage is sensed and compared to the over-voltage threshold  $V_{PFC\_OV2} = 115\% * V_{PFC\_ref} = 2.88 \text{ V}$ . Once the pin voltage is above this threshold for longer than the blanking time, both PFC and HB stop switching and ICL5102 will enter auto-restart.

#### 3.2.5.4 PFC Open Control Loop Protection

PFC control loop open is monitored at the PFCVS pin.

The PFCVS pin voltage is sensed and compared to the over-voltage threshold  $V_{PFC\_UV2} = 12.5\% * V_{PFC\_ref} = 0.31 \text{ V}$ .

- In the normal operation, once the pin voltage is below this threshold for longer than the blanking time, both PFC and HB stop switching and ICL5102 will enter auto-restart.
- In the IC power up phase, if the pin voltage is below this threshold, ICL5102 will not start-up.

#### 3.2.5.5 PFC Inductor Over-current Protection

PFC inductor over-current is monitored at the PFCCS pin.

The voltage across the PFC current sense shunt resistor is sensed at the PFCCS pin and compared to the over-current threshold  $V_{PFC\_OCP1} = 1.0 \text{ V}$ . Once the pin voltage is above this threshold for longer than the blanking time  $t_{PFC\_OCP1\_blanking} = 200 \text{ ns}$ , the PFC MOSFET is turned off in the current switching cycle.

#### 3.2.5.6 Input Brown-out Protection

Input brown-out is monitored at the BO pin.

The BO pin voltage is sensed and compared to the brown-out threshold  $V_{BO\_out} = 1.2 \text{ V}$ .

- In the normal operation, once the pin voltage is below this threshold for longer than the blanking time  $t_{blanking\_BO} = 50 \text{ ms}$ , both PFC and HB stop switching and ICL5102 will enter auto-restart. Once the pin voltage is higher than  $V_{BO\_in} = 1.4 \text{ V}$ , normal operation starts (brown-in).
- In the IC power up phase, if the pin voltage is below this threshold, ICL5102 will not start-up.

### 3.3 Resonant Half-Bridge Controller

Resonant Half-Bridge (HB) topologies reduce losses and switching noise in the converter compared to traditional “Hard Switching” topologies. This is accomplished by soft commutation in a sinusoidal manner and zero voltage switching (ZVS) of HB MOSFETs.

Soft commutation of the power devices allows for increased converter operating switching frequency and smaller sizes of the passive components such as transformers and filters. ICL5102 provides the independent control of resonant HB (e.g. LLC or LCC) for constant voltage (CV) or constant current (CC) output. It supports both fixed and variable switching frequency control.

#### 3.3.1 Control Scheme

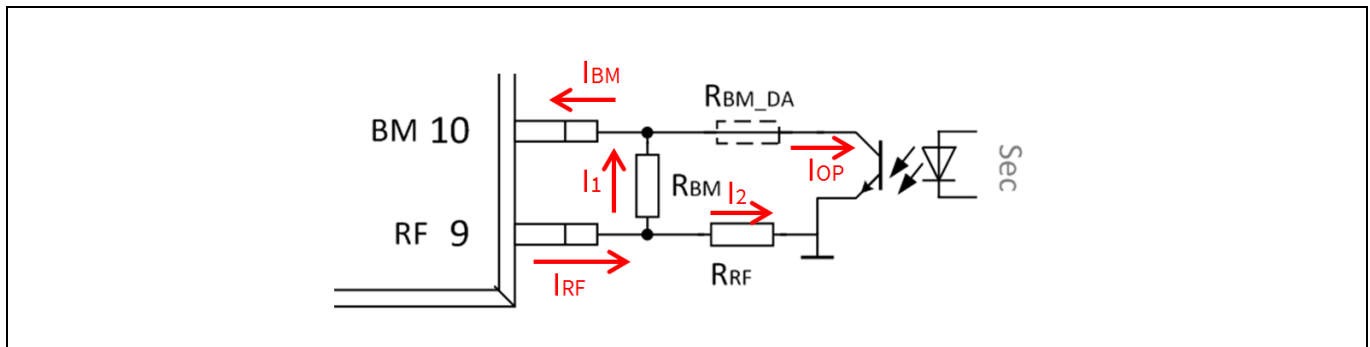
The ICL5102 resonant HB control is realized through a TCO (Time Controlled Oscillator) in the soft-start phase and a current controlled oscillator (CCO) in the regulated normal operation. During light load operation the ICL5102 will enter Burst Mode (BM) to maximize light-load efficiency. This is described as following:

- HB switching frequency control via the Current Controlled Oscillator (CCO)
- HB controller frequency setting
- Soft-start control via a Time Controlled Oscillator (TCO)
- HB Burst Mode (BM) operation

##### 3.3.1.1 HB Frequency Control via CCO

During normal operation, ICL5102 HB controller uses CCO to determine the switching frequency. The switching frequency is determined by current  $I_{RF}$  that flows out of the RF pin. The RF pin maintains a constant voltage of  $V_{RF} = 2.5\text{ V}$ . This voltage together with the voltage at pin  $V_{BM}$ , resistors  $R_{BM}$  and  $R_{RF}$ , and the opto-coupler define the current flowing out of the RF pin as shown in the following formula and **Figure 12**:

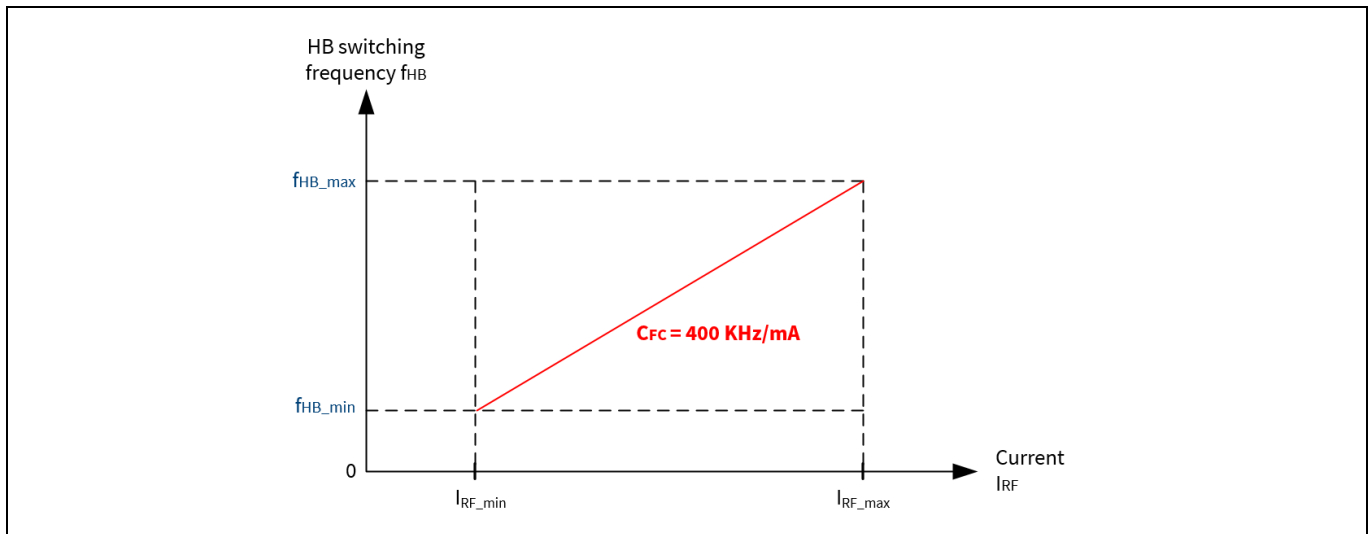
$$I_{RF} = I_1 + I_2 = I_{BM} + I_{OP} + \frac{V_{RF}}{R_{RF}}$$



**Figure 12** ICL5102 RF Pin Current Definition

The CCO of ICL5102 HB controller is defined linearly with the constant slew rate  $C_{FC}$  as shown in **Figure 13**:

$$C_{FC} = 400\text{ KHz/mA}$$



**Figure 13 CCO of ICL5102 in Normal Operation**

### 3.3.1.2 HB Controller Frequency Setting

Both TCO and CCO of ICL5102HV operate based on the defined minimum and maximum HB operating frequency.

- Minimum HB operating frequency  $f_{HB\_min}$ :

It is defined in the HB resonant tank calculation to prevent HB operation in the capacitive region where reverse gain occurs and HB MOSFETs ZVS is lost. ICL5102 HB controller operates with  $f_{HB\_min}$  if the minimum current  $I_{RF\_min}$  flows out of the RF pin according to the CCO:

$$f_{HB\_min} = C_{FC} * I_{RF\_min}$$

This minimum current occurs when the opto-coupler is off  $I_{OP} = 0$  and the voltage of the pin is clamped at  $V_{BM\_max} = 2.25$  V:

$$I_{RF\_min} = \frac{V_{RF}}{R_{RF}} + \frac{V_{RF} - V_{BM\_max}}{R_{BM}}$$

- Maximum HB operating frequency  $f_{HB\_max}$ :

ICL5102 HB controller increases the HB operating frequency as the output load reduces. However above the maximum operating frequency  $f_{HB\_max}$  the output power cannot be reduced furthermore and HB controller enters BM. According to the CCO,  $f_{HB\_max}$  is defined with the maximum current  $I_{RF\_max}$ :

$$f_{HB\_max} = C_{FC} * I_{RF\_max}$$

ICL5102 enters BM when the voltage at BM pin is  $V_{BM\_entry} = 0.75$ V:

$$I_{RF\_max} = \frac{V_{RF}}{R_{RF}} + \frac{V_{RF} - V_{BM\_entry}}{R_{BM}}$$

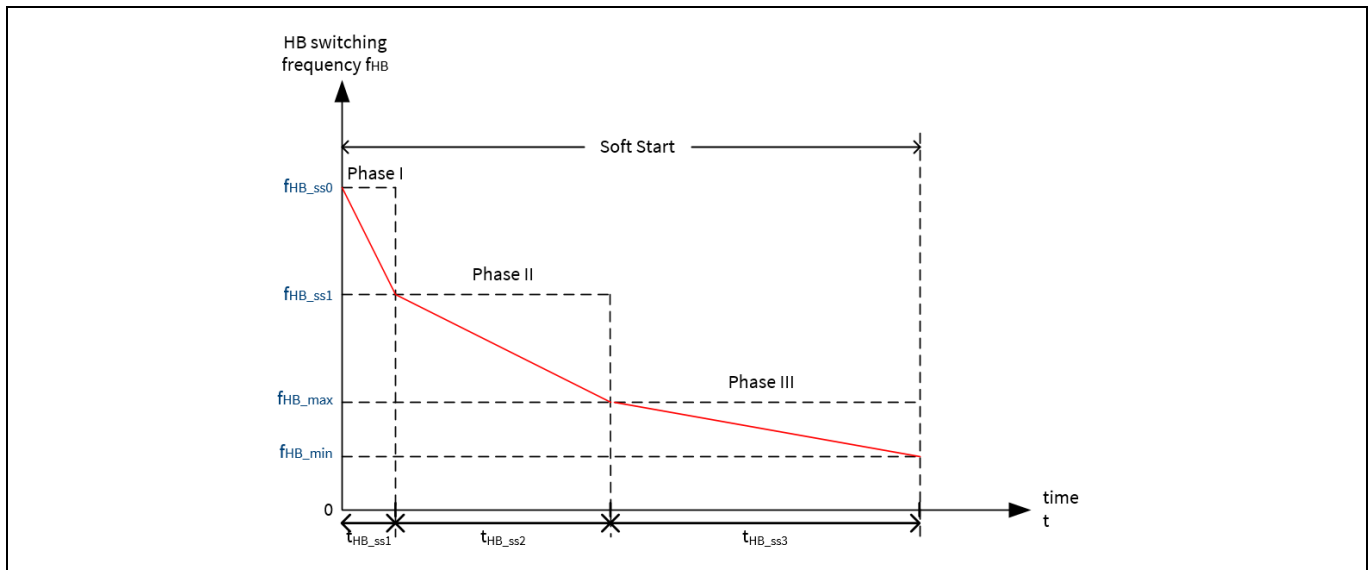
- The minimum and maximum HB operating frequencies must fulfill the following condition:

$$f_{HB\_max} < 7 * f_{HB\_min}$$

Both minimum and maximum HB operating frequencies are set together by the external resistors  $R_{BM}$  and  $R_{RF}$  as shown in the **Figure 12**.

### 3.3.1.3 HB Soft-Start Control via TCO

ICL5102 HB controller initializes a soft-start at power up after the bus voltage reaches 75% of nominal value (when the VSPFC pin reaches the  $V_{PFC\_UV1} = 75% * V_{PFC\_ref} = 1.88$  V). During soft-start, the HB switching frequency reduces with respect to the elapsed time (time controlled oscillator), which is shown in **Figure 14**:



**Figure 14 TCO for Half-Bridge Soft-start**

The complete HB soft-start takes maximum 7 ms and is divided into three time phases in which the frequency reduction has different slew rate:

- Soft-start phase I

- The maximum duration of soft-start phase I is  $t_{HB\_SS1} = 624 \text{ us}$ .
- The HB soft-start phase I begins with the switching frequency  $f_{HB\_ss0}$ , which is defined as:

$$f_{HB\_ss0} = 4 * (f_{max} - f_{min}) + f_{min}$$

- The maximum possible soft-start start frequency is  $f_{HB\_ss\_start\_max} = 1300 \text{ KHz}$ .
- The HB soft-start phase I ends with the switching frequency  $f_{HB\_ss1}$ , which is defines as:

$$f_{HB\_ss1} = 2.6 * (f_{max} - f_{min}) + f_{min}$$

- Soft-start phase II

- The maximum duration of soft-start phase II is  $t_{HB\_SS2} = 2.5 \text{ ms}$ .
- The HB soft-start phase II begins with the switching frequency  $f_{HB\_ss1}$ .
- The HB soft-start phase II ends with the maximum switching frequency  $f_{HB\_max}$ .

- Soft-start phase III

- The maximum duration of soft-start phase III is  $t_{HB\_SS3} = 3.75 \text{ ms}$ .
- The HB soft-start phase III begins with the switching frequency  $f_{HB\_max}$ .
- The HB soft-start phase III ends with the minimum switching frequency  $f_{HB\_min}$ .

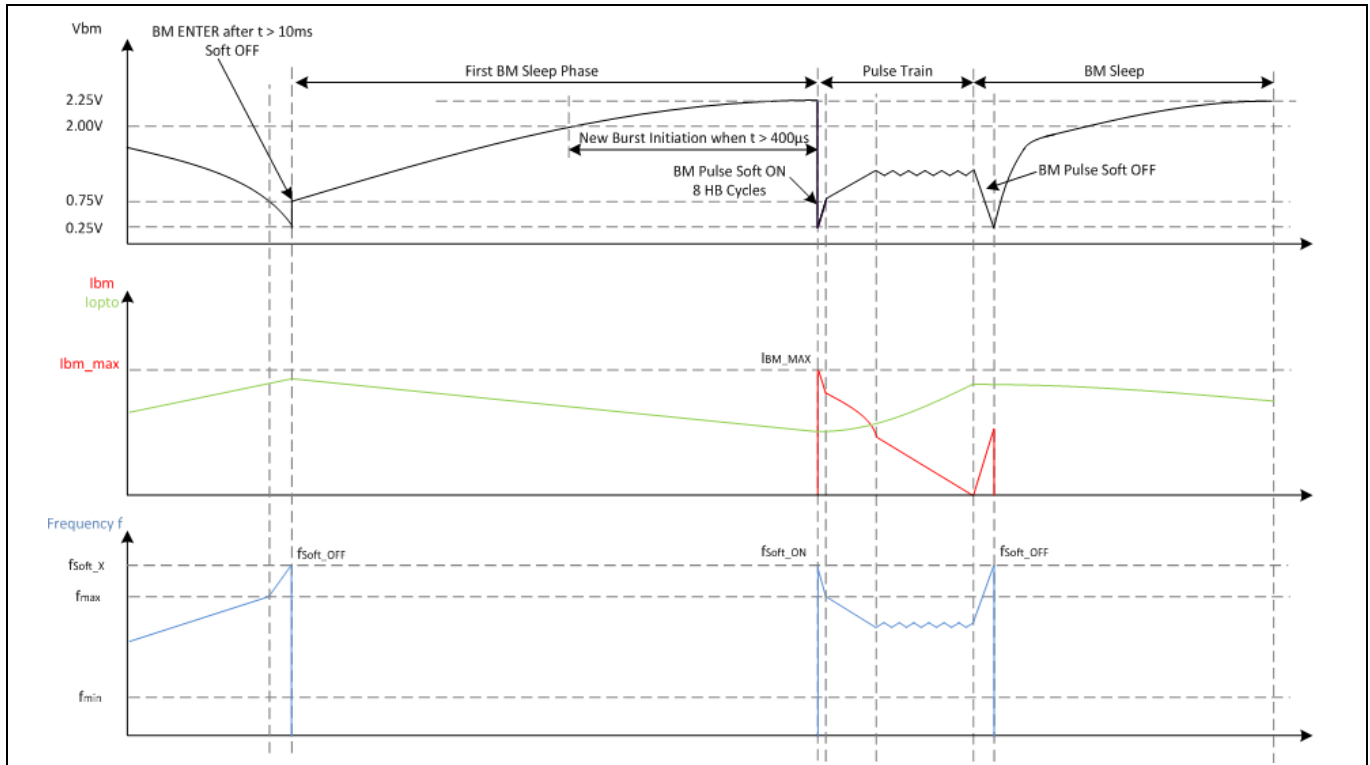
The voltage at the BM pin is clamped to 0.75 V during soft-start phase I and phase II. Therefore the current flowing out of the RF pin is constant and the HB switching frequency is only determined by the TCO.

In the soft-start phase III, the voltage at BM pin is ramped up from 0.75 V to 2.25 V and the current flowing out of the RF pin reduces accordingly. In the meantime, as the secondary side output voltage approaches the target value, the current flowing through the opto-coupler primary side begins to increase. Once the current through opto-coupler  $I_{OP}$  is equal to the current  $I_1$  through the resistor  $R_{BM}$  so that the current  $I_{BM} = 0$  (see [Figure 12](#)), the soft-start is terminated and the CCO will takes over the control from the TCO.

During soft-start operation, if the voltage at the LSCS pin is greater than the threshold 0.8V, the HB controller will stop reducing the switching frequency. The switching frequency reduction resumes once the voltage drops below the threshold.

#### 3.3.1.4 HB Burst Mode operation

ICL5102 HB controller will enter the BM as the transferred power to output is greater than the output load demands although the HB is operated at the maximum switching frequency  $f_{HB\_max}$ . It is recommended to put ICL5102 into BM in standby (dim-to-off) mode for lowest input standby power.



**Figure 15** HB BM Control

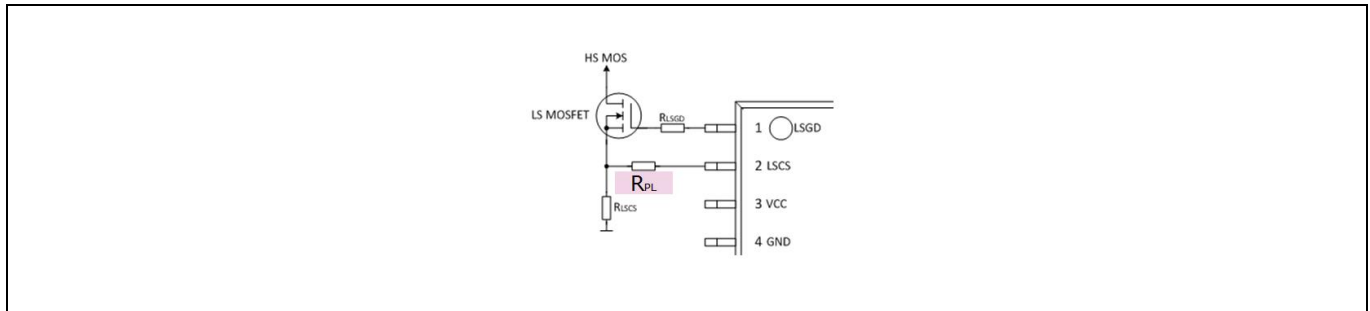
As shown in the **Figure 15**, the BM control is implemented by the sensing the voltage  $V_{BM}$  at pin BM:

- **BM entry:**  
During normal operation, once the BM pin voltage is lower than  $V_{HB\_BM\_Entry} = 0.75V$  for longer than  $V_{HB\_BM\_Entry\_blanking} = 10ms$ , ICL5102 will first initialize a soft-off by increasing the HB switching frequency from  $f_{HB\_max}$  to  $f_{HB\_BM}$ . After  $f_{HB\_BM}$  is reached, both PFC and HB switching are stopped and ICL5102 is in sleep mode.

$$f_{HB\_BM} = \frac{4}{3} * (f_{max} - f_{min}) + f_{min}$$

- **BM burst-on:**  
During sleep mode, the BM pin voltage  $V_{BM}$  increases as the output voltage drops. ICL5102 will activate both PFC and HB stages once  $V_{BM} = 2.25V$  is reached.  
The ICL5102 HB controller turns on with a switching frequency of  $f_{HB\_BM}$  and steadily decreases it to  $f_{HB\_max}$  to initialize a soft-on. After soft-on, the switching frequency continues to decrease until the BM power limitation is active.
- **BM power limitation:**  
The ICL5102 activates power limitation in the BM burst-on phase once the switching frequency  $f_{HB\_PL}$  is reached. The transferred power in BM can be adjusted through the resistor  $R_{PL}$  from LSCS pin to the HB low side MOSFET source as shown in the **Figure 16**. In the BM power limitation phase, the HB switching frequency is maintained around  $f_{HB\_PL}$ .





**Figure 16 ICL5102 Burst Mode Power Limitation**

- **BM burst-off:**

Once current flowing through the opto-coupler (as output voltage increasing) is equal to the current  $I_1$  through the resistor  $R_{BM}$  which means  $I_{BM} = 0$  (see **Figure 12**), soft-off operation is initialized by increasing the HB switching frequency to  $f_{HB\_BM}$ . After  $f_{HB\_BM}$  is reached, both PFC and HB stages stop switching and ICL5102 enter the sleep mode.

- **BM exit:**

ICL5102 will exit the BM under 4 different conditions:

- **During BM burst-off:**

If a sudden output load-step increase occurs during the burst-off phase (sleep mode) the voltage at BM pin will increase abruptly. If  $V_{BM}$  increases from 2.0 V to 2.25 V within 400 us, ICL5102 will exit the BM.

- **During BM burst-on when power limitation is active:**

When the ICL5102 is in the burst-on phase and power limitation is active, the voltage at BM pin is clamped, and cannot change quickly. Once the voltage change (increasing)  $\Delta V_{BM} = + 100$  mV within 8 HB switching cycles, an output load step is detected and ICL5102 will exit BM.

- **During BM burst-on when power limitation is active:**

Once the BM burst-on duration is longer than 10 ms, which means that a static load at output consumes more power than the BM power limitation level, ICL5102 will exit the BM.

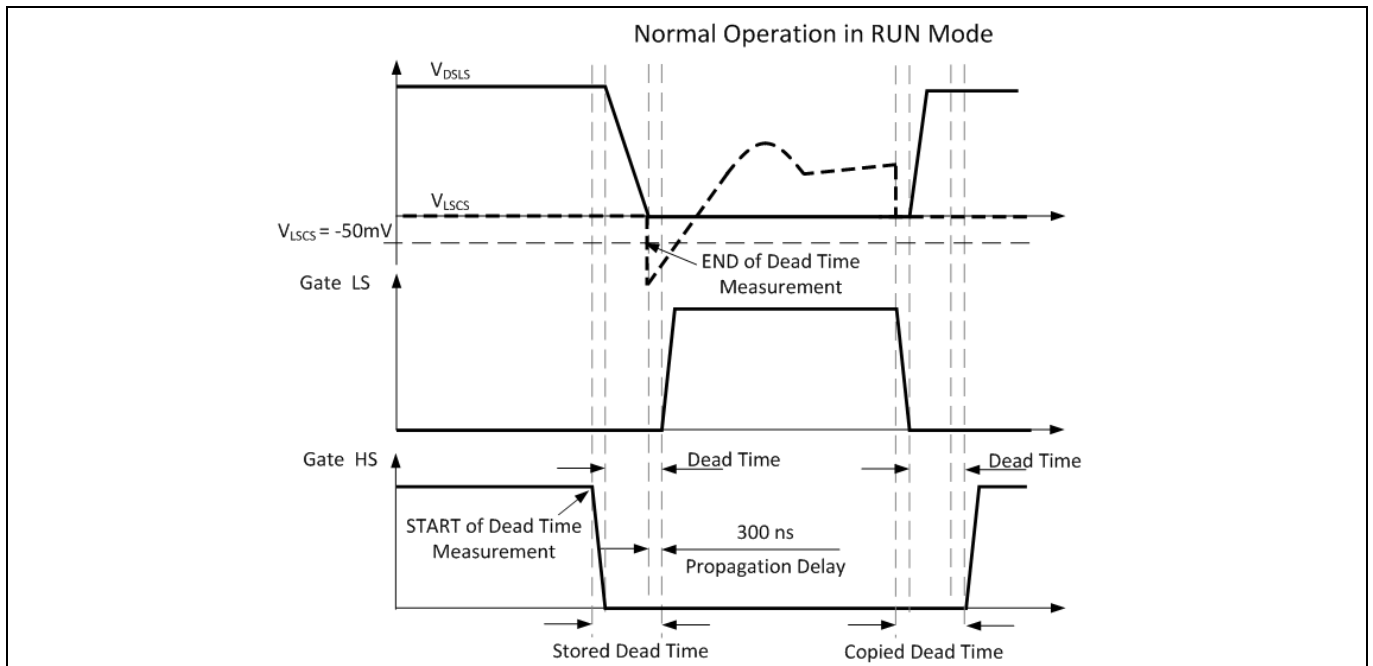
- **During BM burst-on when power limitation is active:**

Once the BM burst-on duration is 2 times longer than the burst-off duration, which means a higher load at output and the BM is not efficient enough. ICL5102 will exit the BM.

To disable the HB BM operation, a resistor between the BM pin and the opto-coupler should be added to prevent the voltage at BM pin to reduce below 0.75 V.

### 3.3.2 HB Self-Adaptive Dead Time

The dead time between ICL5102 HB low side (LS) and high side (HS) gate driver turn-on signals is self-adaptive. The typical range of the dead time adjustment is between 250 and 750 ns. The dead time is measured after the HS gate driver is turned off until the voltage at pin LSCS drops below -50 mV. This time is then used for the dead time between LS and HS as shown in the **Figure 17**.



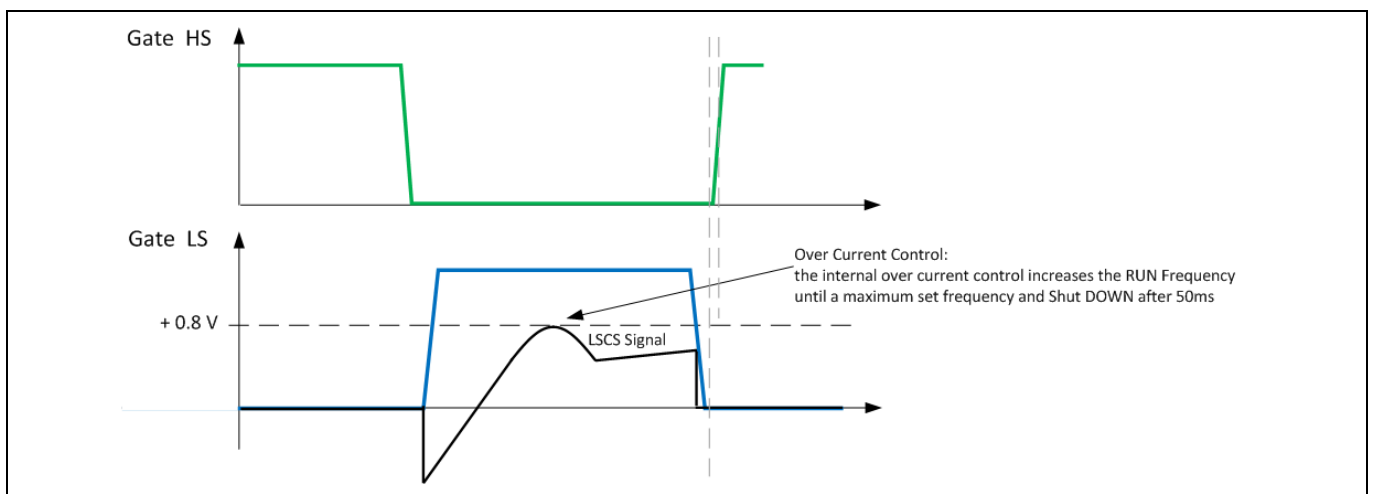
**Figure 17** HB Self-Adaptive Dead Time

### 3.3.3 HB Protection Features

#### 3.3.3.1 HB Over-Current Protection Level 1 (OCP1)

HB over-current level 1 is monitored at the LSCS pin.

The voltage across the HB LSCS shunt resistor is sensed at the LSCS pin during the HB low side gate driver turning-on and compared to the over-current threshold  $V_{HB\_OCP1} = 0.8\text{ V}$ . Once the voltage exceeds this threshold, the controller will increase the HB switching frequency cycle by cycle till the maximum switching frequency  $f_{HB\_max}$  is reached. If a HB over-current event occurs (HB OCP1) beyond the blanking time  $t_{HB\_OCP1\_blanking} = 50\text{ms}$ , ICL5102 will enter auto-restart.



**Figure 18** HB Over-current Protection Level 1

#### 3.3.3.2 HB Over-Current Protection Level 2 (OCP2)

HB over-current level 2 is monitored at the LSCS pin.

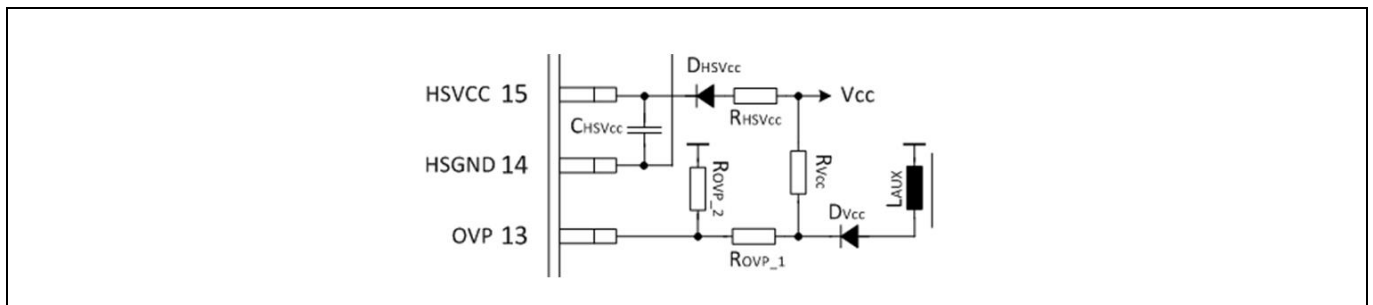
### Functional Description

The voltage across the HB low side current sense shunt resistor is sensed at the LSCS pin during the HB low side gate driver turning-on and compared to the over-current threshold  $V_{HB\_OCP2} = 1.6\text{ V}$ . Once the voltage exceeds this threshold for longer than the blanking time  $t_{HB\_OCP2\_blanking} = 500\text{ ns}$ , both PFC and HB stop switching and ICL5102 will enter auto-restart.

### 3.3.3.3 HB Output Over-Voltage Protection

HB output over-voltage is monitored at the OVP pin.

ICL5102 provides an independent OVP pin for the output-over voltage protection. This pin should be connected to the auxiliary winding of the HB transformer as shown in the **Figure 19** below:



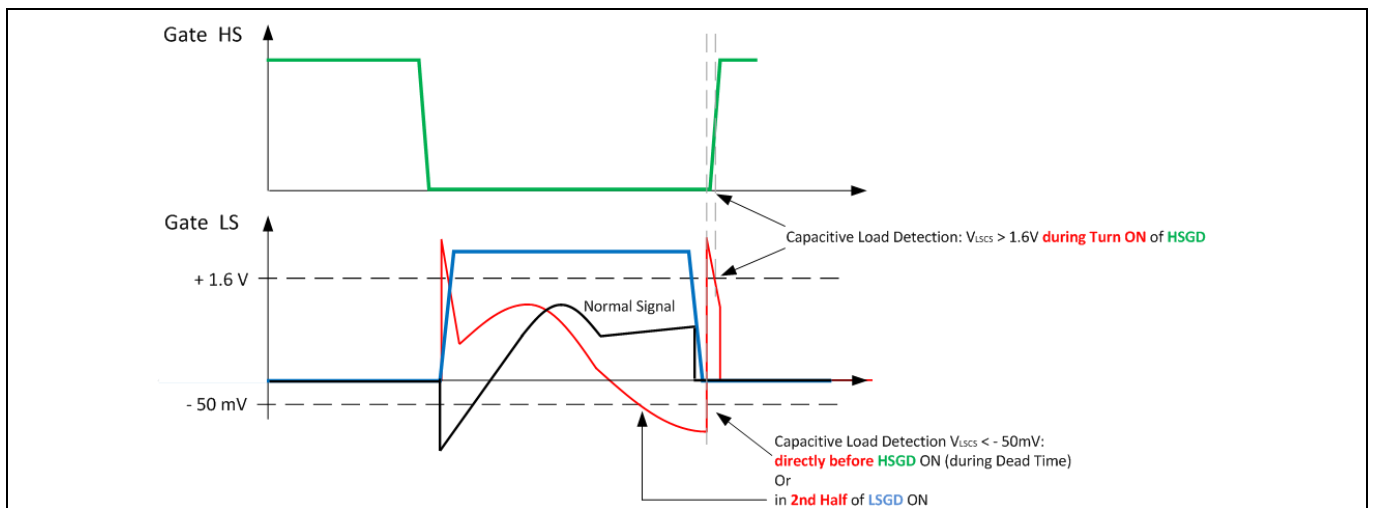
**Figure 19** HB Output OVP Detection Circuit

A resistor divider scales down the auxiliary winding voltage, allowing for auxiliary voltage sensing and OVP protection. Once the voltage at OVP pin  $V_{OVP}$  is higher than  $V_{OVP\_ref} = 2.5\text{ V}$  for longer than  $t_{HB\_OVP\_blank} = 5\text{ }\mu\text{s}$ , both PFC and HB stages stop switching and ICL5102 enters auto-restart.

### 3.3.3.4 HB Capacitive Mode Protection

The designed impedance of the resonant network is inductive when the minimum HB switching frequency is above the peak gain frequency. Once the HB switching frequency is below the peak gain frequency, the impedance of the resonant network becomes capacitive and the HB converter enters capacitive mode. Capacitive mode occurs most often due to low input voltage to the HB resonant converter, or during an overload condition on the HB output (shorted or overloaded).

ICL5102 detects the capacitive mode operation by monitoring the LSCS pin:

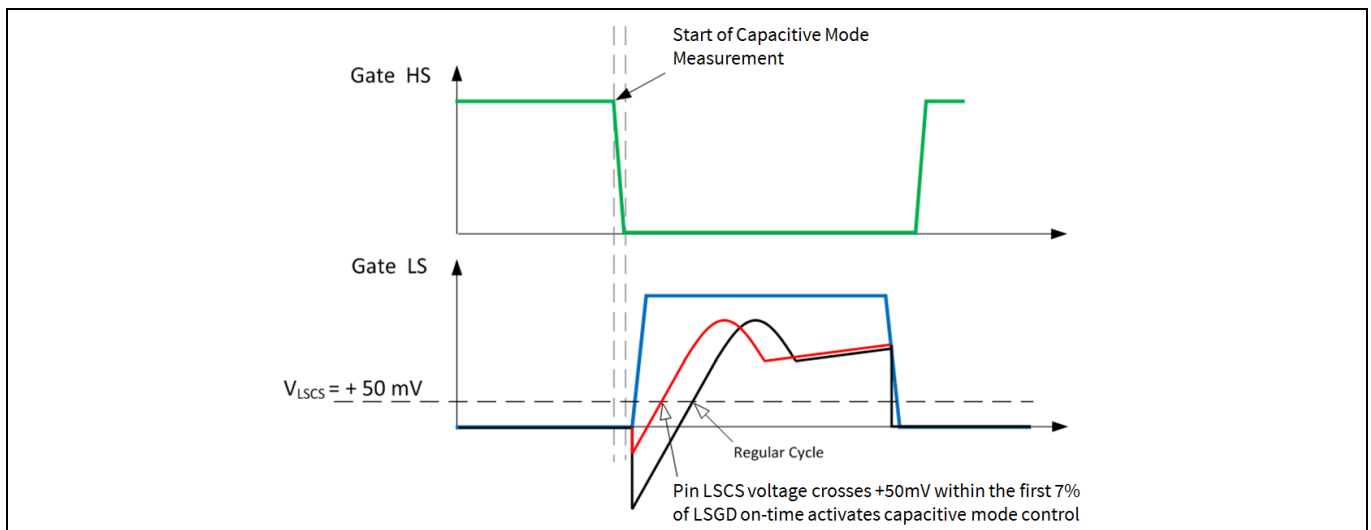


**Figure 20** HB Capacitive Mode Detection

### Functional Description

As shown in the **Figure 20**, once the voltage at the LSCS pin is greater than 1.6 V during turn-on of the HS gate driver or drops below -50 mV in the second half of LSGD on-time or during the dead time between LS and HS, capacitive mode operation is detected.

ICL5102 is able to provide the cycle by cycle frequency control for capacitive mode regulation. This is activated if the LSCS pin voltage is higher than +50 mV within the first 7% of LSGD on-time. The HB controller will increase the frequency cycle by cycle till the +50 mV crossing of the LSCS pin voltage shifts behind the 7% threshold as shown in the **Figure 21**.



**Figure 21** HB Capacitive Mode Regulation

If the capacitive mode operation is detected longer than 620 us despite the capacitive mode control, ICL5102 will enter auto-restart.

## 3.4 Other Protection Features

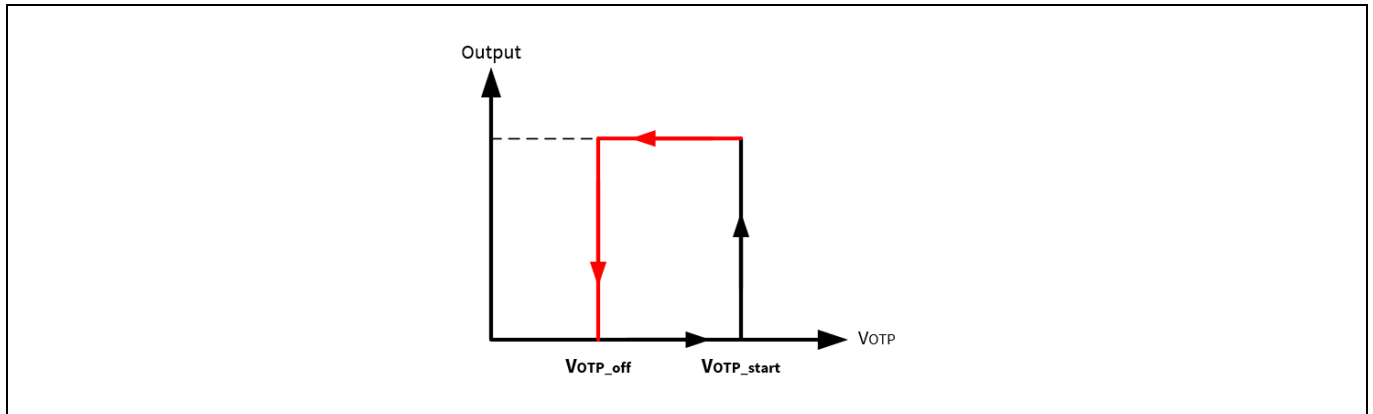
### 3.4.1 External Over-Temperature Protection (OTP)

External temperature is sensed at the OTP pin via an external NTC resistor from OTP pin to GND.

The source current out of the OTP pin is  $I_{OTP} = 100 \mu A$ . The current generates a voltage drop on the connected NTC. Once the voltage at the OTP pin decreases below  $V_{OTP\_off} = 625 \text{ mV}$  longer than the blanking time  $t_{OTP\_blanking} = 620 \mu s$  in the normal operation, both PFC and HB stages stop switching and ICL5102 will enter auto-restart. PFC and HB operations recover after the voltage at the OTP pin is higher than  $V_{OTP\_start} = 703 \text{ mV}$  for longer than  $t_{OTP\_blanking}$ . This is shown in the **Figure 22**.

It is recommended to place good quality ceramic capacitor close to the OTP pin to prevent noise from falsely triggering OTP protection.

To disable the External OTP, a resistor can be added at the OTP pin instead of the NTC to hold the voltage always higher than  $V_{OTP\_start} = 703 \text{ mV}$ .



**Figure 22 External Over-Temperature Protection**

### 4 ICL5102 Operation Flow Chart

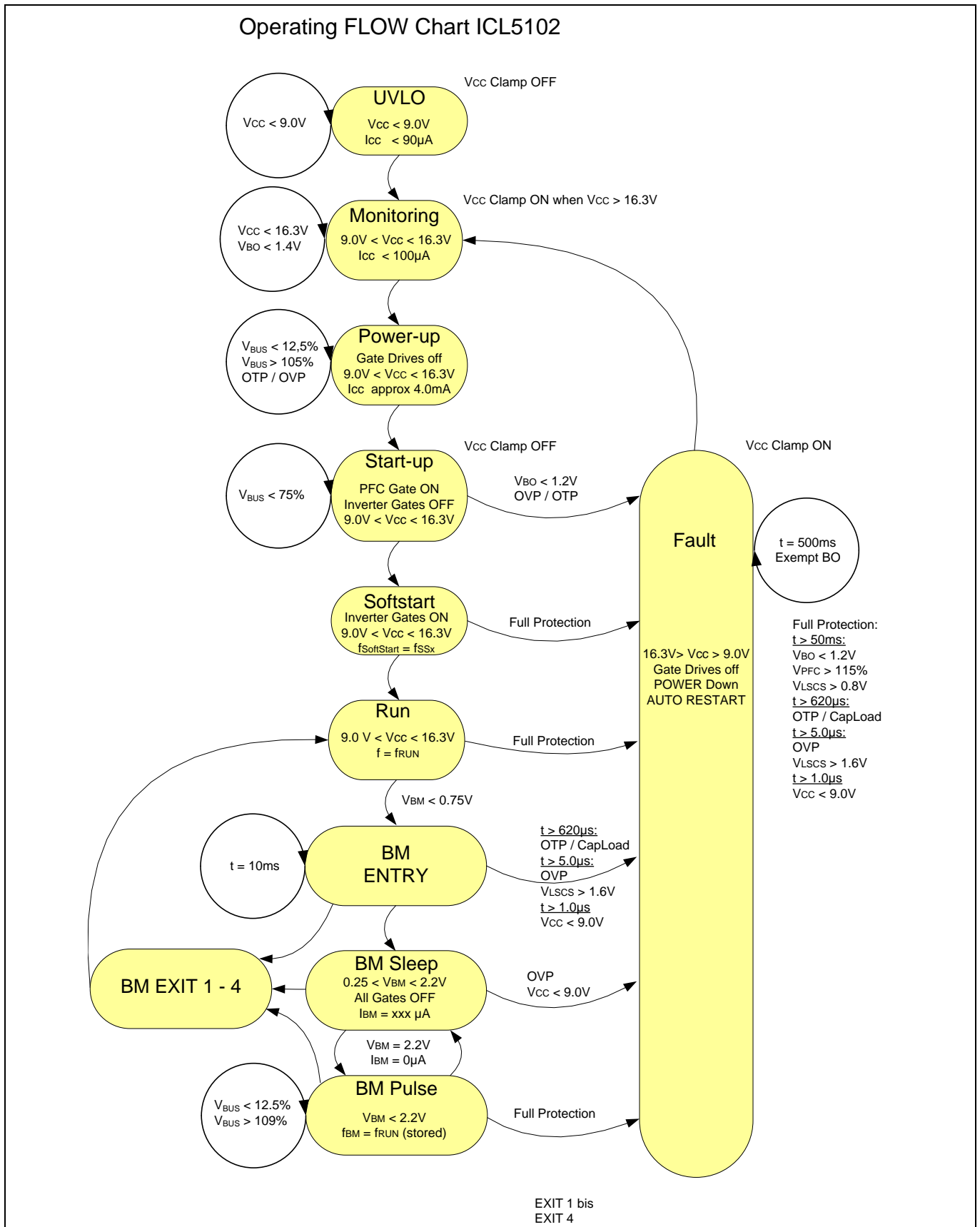


Figure 23 ICL5102 Operation Flow Chart

## 5 Electrical Characteristics

*Note: All voltages except the high-side signals are measured with respect to GND (pin 4). The high-side voltages are measured with respect to HSGND (pin 14). The voltage levels are valid if other ratings are not violated.*

### 5.1 Package Characteristics

**Table 2 Package Characteristics**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Thermal resistance for PG-DSO-16	$R_{thJA}$	—	119	K/W	PG-DSO-16 @ $T_A = 85^\circ\text{C}$ & PCB Area > 30mm x 20mm
Creepage distance HSGND vs OVP pin	$D_{CRHS}$	0.78	—	mm	

### 5.2 Absolute Maximum Ratings

*Note: Absolute maximum ratings (Table 2) are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are under DC condition unless specified and are not tested during production test.*

**Table 3 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
LSCS pin Voltage	$V_{LSCS}$	- 5	6	V	
LSCS pin Current	$I_{LSCS}$	- 3	3	mA	
LSGD pin Voltage	$V_{LSGD}$	- 0.3	$V_{CC}+0.3$	V	Internally clamped to 11V
LSGD pin peak source current <sup>1</sup>	$I_{LSGD\_O\_max}$	- 75	5	mA	< 500 ns
LSGD pin peak sink current <sup>2</sup>	$I_{LSGD\_I\_max}$	- 50	400	mA	< 100 ns
Voltage externally supplied to pin VCC	$V_{VCC}$	- 0.3	18.5	V	
Vcc pin internal zener diode clamp current	$I_{VCC\_clamp}$	- 5	5	mA	
PFCGD pin voltage	$V_{PFCGD}$	- 0.3	$V_{CC}+0.3$	V	Internally clamped to 11V
PFCGD pin peak source current <sup>1</sup>	$I_{PFCGD\_O\_max}$	- 150	5	mA	< 500 ns
PFCGD pin peak sink current <sup>2</sup>	$I_{PFCGD\_I\_max}$	- 100	700	mA	< 100 ns
PFCCS pin voltage	$V_{PFCCS}$	- 5	6	V	

<sup>1</sup> Current when PFCGD pin is high. The negative sign means a current flowing out from the IC.

<sup>2</sup> Current when PFCGD pin is low. The negative sign means a current flowing out from the IC.

### Electrical Characteristics

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
PFCSS pin current	$I_{PFCSS}$	- 3	3	mA	
PFCZCD pin voltage	$V_{PFCZCD}$	- 3	6	V	
PFCZCD pin current	$I_{PFCZCD}$	- 5	5	mA	
PFCVS pin voltage	$V_{PFCVS}$	- 0.3	5.3	V	
RF pin voltage	$V_{RF}$	- 0.3	5.3	V	
OTP pin voltage	$V_{OTP}$	- 0.3	5.3	V	
OVP pin voltage	$V_{OVP}$	- 0.3	5.3	V	
BM pin voltage	$V_{BM}$	- 0.3	5.3	V	
BO pin Voltage	$V_{BO}$	- 0.3	5.3	V	
HSGND pin voltage	$V_{HSGND}$	- 650	650	V	Referring to GND <sup>1</sup>
HSGND pin voltage transient	$dV_{HSGND} / dt$	- 40	40	V/ns	
Voltage externally supplied to pin HSVCC	$V_{HSVCC}$	- 0.3	18.0	V	Referred to HSGND
HSGD pin voltage	$V_{HSGD}$	- 0.3	$V_{HSVCC} + 0.3$	V	Internally clamped to 11V
HSGD pin peak source current <sup>2</sup>	$I_{HSGD\_O\_max}$	- 75	0	mA	< 500 ns
HSGD pin peak sink current <sup>3</sup>	$I_{HSGD\_I\_max}$	0	400	mA	< 100 ns
Junction temperature	$T_J$	- 40	150	°C	
Storage temperature	$T_S$	- 55	150	°C	
Total IC power dissipation	$P_{TOT}$	—	1	W	PG-DSO-16 / $T_{amb} = 25^\circ\text{C}$
Soldering temperature	$T_{SOLD}$	—	260	°C	Wave Soldering <sup>4</sup>
Latch-up capability	$I_{LU}$	—	150	mA	Pin voltages acc. to abs. maximum ratings <sup>5</sup>
ESD Capability HBM	$V_{ESD\_HBM}$	—	2	kV	Human Body Model <sup>6</sup>
ESD Capability CDM	$V_{ESD\_CDM}$	—	500	V	Charged Device Model <sup>7</sup>

<sup>1</sup> Limitation due to creepage distance between the high side and low side pins (CTT 900V inside)

<sup>2</sup> Current when PFCGD pin is high. The negative sign means a current flowing out from the IC.

<sup>3</sup> Current when PFCGD pin is low. The negative sign means a current flowing out from the IC.

<sup>4</sup> According to JESD22-A111 Rev A

<sup>5</sup> Latch-up capability according to JEDEC JESD78D,  $T_A = 85^\circ\text{C}$

<sup>6</sup> ESD-HBM according to ANSI/ESDA/JEDEC JS-001-2012

<sup>7</sup> ESD-CDM according to JESD22-C101F



### Electrical Characteristics

## 5.3 Operating Conditions

The recommended operating conditions are shown for which the DC Electrical Characteristics are valid.

**Table 4 Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Voltage externally supplied to pin HSVCC	$V_{HSVCC}$	$V_{HSVCC\_Off}$	17.5	V	Referring to HSGND
HSGND pin voltage	$V_{HSGND}$	- 650	650	V	Referring to GND
External supplied $V_{CC}$	$V_{VCC}$	$V_{VCC\_Off}$	17.5	V	$T_J = 25^\circ\text{C}$
External supplied $V_{CC}$	$V_{VCC}$	$V_{VCC\_Off}$	18.0	V	$T_J = 125^\circ\text{C}$
LSCS pin voltage	$V_{LSCS}$	- 4	5	V	In active mode
PFCVS pin voltage	$V_{PFCVS}$	0	4	V	
PFCCS pin voltage	$V_{PFCCS}$	- 4	5	V	In active mode
PFCZCD pin voltage	$I_{PFCZCD}$	- 3	3	mA	In active mode
OVP pin voltage	$V_{OVP}$	0	2.5	V	
Junction temperature	$T_J$	- 40	125	$^\circ\text{C}$	
Adjustable HB switching frequency	$f_{HB}$	20	500	kHz	
HB Soft-start switching frequency	$f_{HB\_SS\_max}$	—	1300	kHz	@ Soft Start
AC mains input frequency	$f_{AC}$	45	65	Hz	For notch filter

## 5.4 DC Electrical Characteristics

*Note:* The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range  $T_J$  from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . Typical values represent the median values, which are given in reference to  $25^\circ\text{C}$ . If not otherwise stated, a supply voltage of 15 V and  $V_{HSVCC} = 15\text{ V}$  is assumed and the IC operates in active mode. Furthermore, all voltages refer to GND if not otherwise mentioned.

### 5.4.1 Power Supply Characteristics

**Table 5 Operating Range**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Vcc Quiescent supply Current 1	$I_{VCC\_QU1}$	—	70	120	$\mu\text{A}$	$V_{VCC} = 8.0\text{V}$
Vcc Quiescent supply Current 2 <sup>1</sup>	$I_{VCC\_QU2}$	—	4.0	5.8	mA	$V_{PFCVS} > V_{PFCVS0V2}, V_{VCC} = 15\text{V}$
Vcc supply current in sleep mode	$I_{VCC\_sleep}$	—	100	160	$\mu\text{A}$	
Vcc turn-on threshold	$V_{VCC\_On}$	15.4	16.0	16.6	V	

<sup>1</sup> Device active but with inactive gates

### Electrical Characteristics

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Vcc turn-off threshold	$V_{VCC\_Off}$	8.5	9.0	9.5	V	
Vcc on-off hysteresis	$V_{VCC\_Hys}$	6.7	7.0	7.4	V	
Vcc internal clamping voltage	$V_{VCC\_Clamp}$	15.4	16.3	16.6	V	$I_{VCC} = 2mA$
Vcc internal clamping current	$I_{VCC\_clamp}$	2.5	3.5	4.5	mA	$V_{VCC} = 18V$
High side leakage current	$I_{HSGND\_leak}$	—	0.01	2.0	$\mu A$	$V_{HSGND} = 650V, V_{GND} = 0V$
HSVcc Quiescent supply Current 1	$I_{HSVCC\_QU1}$	—	190	280	$\mu A$	$V_{HSVCC} = 8.0V^{12}$
HSVcc Quiescent supply Current 2 <sup>1</sup>	$I_{HSVCC\_QU2}$	—	0.65	1.2	mA	$V_{HSVCC} > V_{HSVCC\_On}$
HSVcc turn-on threshold	$V_{HSVCC\_On}$	9.55	10.3	11	V	<sup>2</sup>
HSVcc turn-off threshold	$V_{HSVCC\_Off}$	7.9	8.6	9.3	V	<sup>12</sup>
HSVcc on-off hysteresis	$V_{HSVCC\_Hy}$	1.4	1.7	2.1	V	<sup>12</sup>

## 5.4.2 PFC Stage Characteristics

**Table 6 Electrical Characteristics of the PFCGD Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
PFCGD low voltage	$V_{PFCGD}$	0.40	0.70	0.92	V	$I_{PFCGD} = 5mA$
		0.40	0.75	1.12	V	$I_{PFCGD} = 20mA$
		- 0.20	0.30	0.62	V	$I_{PFCGD} = -20mA$
PFCGD high voltage	$V_{PFCGDH}$	10.0	11.0	11.6	V	$I_{PFCGD} = -20mA$
		7.5	—	—	V	$I_{PFCGD} = -1mA^3$
		7.0	—	—	V	$I_{PFCGD} = -5mA^{13}$
PFCGD active shut down	$V_{PFCGDASD}$	0.40	0.75	1.12	V	$I_{PFCGD} = 20mA / V_{VCC} = 5V$
PFCGD UVLO shut down	$V_{PFCGDUVLO}$	0.30	1.00	1.60	V	$I_{PFCGD} = 5mA / V_{VCC} = 2V$
PFCGD peak source current	$I_{PFCGDSO}$	—	- 100	—	mA	<sup>4</sup>
PFCGD peak sink current	$I_{PFCGDSI}$	—	500	—	mA	<sup>14</sup>
PFCGD voltage during sink current	$V_{PFCGDHS}$	10.8	11.7	12.3	V	$I_{PFCGD} = 3mA$
PFCGD rise time	$t_{PFCGDR}$	125	275	580	ns	$2V < V_{PFCGD} < 8V^5$
PFCGD fall time	$t_{PFCGDF}$	20	45	72	ns	$2V < V_{PFCGD} < 8V^{15}$

<sup>1</sup> Device active but with inactive gates

<sup>2</sup> Referring to high-side ground (HSGND)

<sup>3</sup>  $V_{VCC} = V_{VCC\_off} + 0.3V$

<sup>4</sup> The parameter is not subject to production testing – verified by design/characterization

<sup>5</sup>  $R_{Load} = 4\Omega$  and  $C_{Load} = 3.3nF$

### Electrical Characteristics

**Table 7 Electrical Characteristics of the PFCCS Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
PFC OCP1 comparator reference voltage	$V_{PFC\_OCP1}$	0.95	1.0	1.05	V	
PFC OCP1 blanking time (incl. prorogation delay)	$t_{PFC\_OCP1\_blanking}$	140	200	260	ns	
Leading-edge blanking	$t_{PFC\_LEB}$	180	250	320	ns	Pulse width when $V_{PFCCS} > 1.0V$
PFCCS pin bias current	$I_{PFCCSBIAS}$	- 0.5	—	0.5	$\mu A$	$V_{PFCCS} = 1.5V$

**Table 8 Electrical Characteristics of the PFCZCD Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
ZCD reset threshold	$V_{PFCZCDTHR}$	1.4	1.5	1.6	V	
ZCD threshold	$V_{PFCZCDTHRL}$	0.4	0.5	0.6	V	
ZCD hysteresis	$V_{PFCZCDHY}$	—	1.0	—	V	
Input voltage positive clamping level	$V_{PFCZCDCLAMPH}$	4.1	4.6	5.10	V	$I_{PFCZCD} = 2mA$
Input voltage negative clamping level	$V_{PFCZCDCLAMPL}$	- 1.70	- 1.4	- 1.0	V	$I_{PFCZCD} = - 2mA$
PFCZCD pin bias current, high	$I_{PFCZCDBIASH}$	- 0.5	—	5.0	$\mu A$	$V_{PFCZCD} = 1.5V$
PFCZCD pin bias current, low	$I_{PFCZCDBIASL}$	- 0.5	—	0.5	$\mu A$	$V_{PFCZCD} = 0.5V$
Ringing suppression-time	$t_{PFCZCDRING}$	350	500	650	ns	
Limit value for ON-time extension	$\Delta t \times I_{ZCD}$	400	600	670	pC	

**Table 9 Electrical Characteristics of the PFCVS Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
PFCVS pin reference voltage	$V_{PFCVS\_ref}$	2.46	2.50	2.54	V	
PFC OVP level 2 threshold (115% $V_{PFCVS\_ref}$ )	$V_{PFCVS OV2}$	2.82	2.88	2.93	V	PFC and HB OFF
PFC OVP level 1 threshold (109% $V_{PFCVS\_ref}$ )	$V_{PFCVS OV1}$	2.67	2.73	2.78	V	PFC OFF
PFC OVP recovery threshold (105% $V_{PFCVS\_ref}$ )	$V_{PFCVS OVR}$	2.56	2.63	2.68	V	
PFC OVP hysteresis	$V_{PFCVS O VHY}$	70	100	130	mV	4 % rated bus voltage
PFC rated bus voltage (95% $V_{PFCVS\_ref}$ )	$V_{PFCVS RATED}$	2.32	2.38	2.425	V	

### Electrical Characteristics

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
PFC UVP threshold (75% $V_{PFCVS\_ref}$ )	$V_{PFCVSUV1}$	1.83	1.88	1.92	V	
PFC open loop threshold (12.5% $V_{PFCVS\_ref}$ )	$V_{PFCVSUV2}$	0.237	0.31	0.387	V	
PFCVS pin bias current	$I_{PFCVSBIAS}$	- 1.0	—	1.0	$\mu$ A	$V_{PFCVS} = 2.5V$

**Table 10 PFC PWM Generation**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
PFC initial on-time in soft-start	$t_{PFC\_on\_initial}$	1.75	6.0	10.64	$\mu$ s	$V_{PFCZCD} = 0V, V_{BO} = 2.0V$
PFC maximum on-time	$t_{PFC\_on\_max}$	17	22	26	$\mu$ s	$V_{ACIN} = 90V$
PFC minimum on-time in CrCM operation	$t_{PFC\_on\_min}$	100	220	370	ns	
PFC repetition-time	$t_{PFC\_rep}$	47	52	60	$\mu$ s	$V_{PFCZCD} = 0V$
PFC maximum off-time	$t_{PFC\_off}$	42	47	52.5	$\mu$ s	

### 5.4.3 HB Stage Characteristics

**Table 11 Electrical Characteristics of the LSGD Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
LSGD low voltage	$V_{LSGDL}$	0.40	0.70	1.00	V	$I_{LSGD} = 5\text{ mA}$
		0.40	0.80	1.20	V	$I_{LSGD} = 20\text{ mA}$
		- 0.30	0.20	0.53	V	$I_{LSGD} = - 20\text{ mA}$
LSGD high voltage	$V_{LSGDH}$	10.0	10.8	11.6	V	$I_{LSGD} = - 20\text{ mA}$
		7.5	—	—	V	$I_{LSGD} = - 1\text{ mA}^1$
		7.0	—	—	V	$I_{LSGD} = - 5\text{ mA}^{16}$
LSGD active shut down	$V_{LSGDLASD}$	0.4	0.75	1.12	V	$I_{LSGD} = 20\text{ mA} / V_{CC} = 5V$
LSGD UVLO shut down	$V_{LSGDLUVLO}$	0.3	1.0	1.6	V	$I_{LSGD} = 5\text{ mA} / V_{CC} = 2\text{ V}$
LSGD peak source current	$I_{LSGDSO}$	—	- 50	—	mA	<sup>2</sup>
LSGD peak sink current	$I_{LSGDSI}$	—	300	—	mA	<sup>17</sup>
LSGD voltage during sink current	$V_{LSGDHS}$	—	11.7	—	V	$I_{LSGD} = 3\text{ mA}$
LSGD rise time	$t_{LSGDR}$	125	275	580	ns	$2\text{ V} < V_{LSGD} < 8\text{ V}^3$
LSGD fall time	$t_{LSGDF}$	20	35	60	ns	$2\text{ V} < V_{LSGD} < 8\text{ V}^{18}$

<sup>1</sup>  $V_{CC} = V_{CCOFF} + 0.3\text{ V}$

<sup>2</sup> The parameter is not subject to production testing – verified by design/characterization

<sup>3</sup> Load:  $R_{Load} = 10\ \Omega$  and  $C_{Load} = 1\text{ nF}$

### Electrical Characteristics

**Table 12 Electrical Characteristics of the LSCS Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
HB over-current protection level 2	$V_{HB\_OCP2}$	1.54	1.6	1.66	V	
Blanking time for HB over-current protection level 2	$t_{HB\_OCP2\_blanking}$	430	600	670	ns	
HB over-current protection level 1	$V_{HB\_OCP1}$	0.74	0.8	0.86	V	
Blanking time for HB over-current protection level 1	$t_{HB\_OCP1\_blanking}$	—	50	—	ms	<sup>1</sup>
HB capacitive mode detection level 1	$V_{HB\_Cap1}$	1.54	1.6	1.66	V	during turn-on of the HSGD
Blanking time for HB capacitive mode detection level 1	$t_{HB\_Cap1\_blanking}$	30	50	90	ns	
HB capacitive mode detection level 2	$V_{HB\_Cap2}$	- 70	- 50	- 25	mV	before turn-on of the HSGD
Blanking time for HB capacitive mode detection level 2	$t_{HB\_Cap2\_blanking}$	300	390	550	ns	
HB capacitive mode regulation voltage	$V_{HB\_cap\_reg}$	25	50	70	mV	
HB capacitive mode regulation ratio	$K_{HB\_cap\_reg}$	4.5	7.0	9.0	%	
HB over-current control	$V_{LSCSCC}$	0.74	0.8	0.86	V	
LSCS pin bias current	$I_{LSCSBA}$	-1.0	—	1.0	$\mu$ A	$V_{LSCS} = 1.5$ V

**Table 13 Electrical Characteristics of the HSGD Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
HSGD low voltage	$V_{HSGDL}$	0.018	0.05	0.1	V	$I_{HSGD} = 5$ mA
		0.40	1.10	2.50	V	$I_{HSGD} = 100$ mA
		- 0.40	-0.20	- 0.04	V	$I_{HSGD} = - 20$ mA
HSGD high voltage	$V_{HSGDH}$	9.7	10.5	11.3	V	$V_{CC\_HS} = 15$ V $I_{HSGD} = - 20$ mA
		7.8	—	—	V	$V_{CCHSOFF} + 0.3$ V $I_{HSGD} = - 1$ mA
HSGD active shut down	$V_{HSGDLASD}$	0.04	0.22	0.5	V	$V_{CCHS} = 5$ V $I_{HSGD} = 20$ mA
HSGD peak source current	$I_{HSGDSO}$	—	-50	—	mA	<sup>19</sup>
HSGD peak sink current	$I_{HSGDSI}$	—	300	—	mA	<sup>19</sup>
HSGD rise time	$t_{HSGDR}$	120	220	320	ns	$2$ V < $V_{HSGD}$ < $8$ V <sup>2</sup>
HSGD fall time	$t_{HSGDF}$	17	35	70	ns	$2$ V < $V_{HSGD}$ < $8$ V <sup>20</sup>

<sup>1</sup> The parameter is not subject to production testing – verified by design/characterization

<sup>2</sup> Load:  $R_{Load} = 10$   $\Omega$  and  $C_{Load} = 1$  nF

### Electrical Characteristics

**Table 14 Electrical Characteristics of the RF Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
RF pin voltage in normal operation	$V_{RF}$	2.46	2.5	2.54	V	@ $100\mu A < I_{RFM} < 800\mu A$
HB nominal switching frequency	$f_{NOM}$	97.5	100	102.5	kHz	$R_{RF} = 10k\Omega$ without the resistor to BM pin
Adjustable HB switching frequency via the CCO	$f_1$	37	40	43	kHz	$I_{RF} = - 100 \mu A$
	$f_2$	76	80	84	kHz	$I_{RF} = - 200 \mu A$
	$f_3$	190	200	210	kHz	$I_{RF} = - 500 \mu A$
	$f_4$	220	240	260	kHz	$I_{RF} = - 600 \mu A$
	$f_5$	290	320	350	kHz	$I_{RF} = - 800 \mu A$
	$f_{max-25^\circ C}$	450	500	—	kHz	$I_{RF} = - 1.25 \text{ mA} / @ T_j = - 25^\circ C^1$
	$f_{max-40^\circ C}$	400	500	—	kHz	$I_{RF} = - 1.25 \text{ mA} / @ T_j = - 40^\circ C^1$

**Table 15 Electrical Characteristics of the BM Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
HB burst mode entry voltage threshold	$V_{HB\_BM\_entry}$	710	750	790	mV	
Blanking time for HB burst mode entry	$t_{HB\_BM\_entry\_blanking}$	8.5	10.0	11.5	ms	
HB burst mode turn-on threshold	$V_{HB\_BM\_on}$	2.13	2.20	2.27	V	
HB burst mode exit threshold	$V_{HB\_BM\_exit}$	1.93	2.0	2.07	V	
Maximum sink current into the BM pin	$I_{BM\_max}$	—	800	—	$\mu A$	<sup>2</sup>
BM pin current in the sleep mode	$I_{BM\_Stop}$	-3	—	14	$\mu A$	

**Table 16 Electrical Characteristics of the BO Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Brown-out threshold	$V_{BO\_out}$	1.14	1.2	1.26	V	
Brown-in threshold	$V_{BO\_in}$	1.34	1.4	1.46	V	
BO pin bias current	$I_{BOBA}$	-0.5	—	0.5	$\mu A$	$V_{BO} = 5.0V$

<sup>1</sup> Make sure, that the expected ambient temperature does NOT causes a maximum junction temperature higher than 125°C

<sup>2</sup> The parameter is not subject to production testing – verified by design/characterization

### Electrical Characteristics

**Table 17 Electrical Characteristics of the OVP Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
HB OVP pin reference voltage for OVP detection	$V_{HB\_OVP\_ref}$	2.45	2.5	2.55	V	$t > 5\mu s$
Blanking time for HB OVP detection	$t_{HB\_OVP\_blanking}$	—	5	—	$\mu s$	
OVP pin bias current	$I_{OVPBA}$	- 0.5	—	0.5	$\mu A$	$V_{OVP} = 3.0V$

**Table 18 Electrical Characteristics of the OTP Pin**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
OTP turn-on threshold	$V_{OTP\_start}$	670	703	735	mV	
OTP turn-off threshold	$V_{OTP\_off}$	594	625	665	mV	
Blanking time for OTP detection	$t_{OTP\_blanking}$	—	620	—	$\mu s$	<sup>1</sup>
OTP pin source current in normal operation	$I_{OTP}$	- 106	- 100	- 94	$\mu A$	

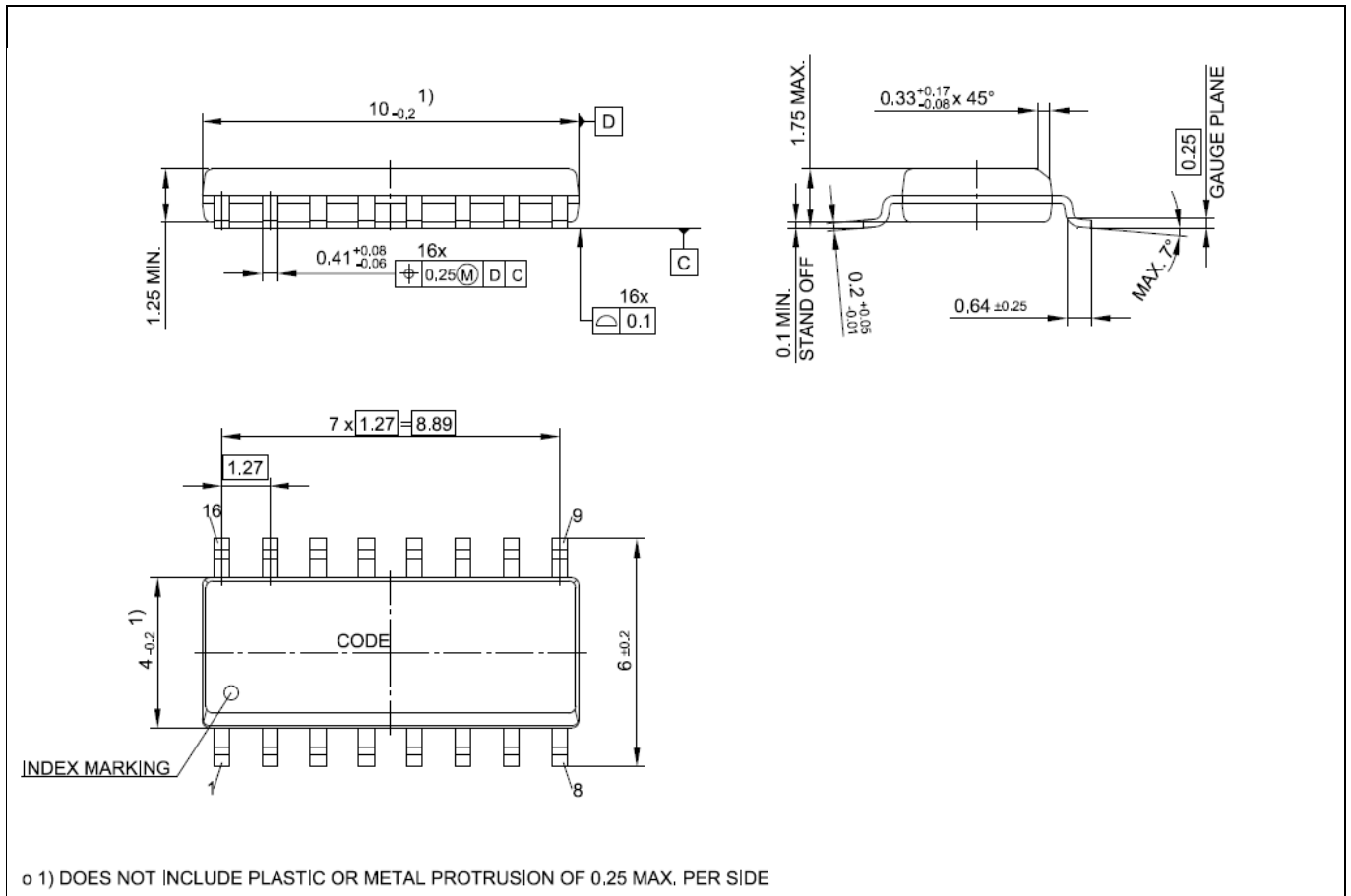
**Table 19 Time Section**

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
HB maximum dead time 1	$t_{Dead\_max1}$	550	750	930	ns	LSCS > - 50mV / 100kHz
HB maximum dead time 2	$t_{Dead\_max2}$	350	500	600	ns	LSCS > - 50mV / 500kHz
HB minimum dead time	$t_{Dead\_min}$	150	250	300	ns	LSCS < - 50mV / 500kHz

<sup>1</sup> The parameter is not subject to production testing – verified by design/characterization

## 6 Package Dimensions

The package dimensions of PG-DSO-16 are provided.



**Figure 24** Package Dimensions for PG-DSO-16

Note: Dimensions in mm.

Note: You can find all of our packages, packing types and other package information on our Infineon internet page “Products”: <http://www.infineon.com/products>.



### Revision history

Document version	Date of release	Description of changes
V1.31	12.01.2022	Correction of test conditions in electrical characteristics tables
V1.2	01.04.2019	Errors correction and content modification
V1.1	09.11.2018	Errors correction and content modification
V1.0	01.06.2018	First release

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