

## FK4B01120L1

## Single N-channel MOS FET

For Load switching circuits

### ■ Features

- Low Drain-source ON resistance:  $R_{DS(on)}$  typ. =  $17\text{m}\Omega$  ( $V_{GS} = 2.5\text{ V}$ )
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1 compliant)

### ■ Marking Symbol: 1C

### ■ Packaging

Embossed type (Thermo-compression sealing) : 1 000 pcs / reel (standard)

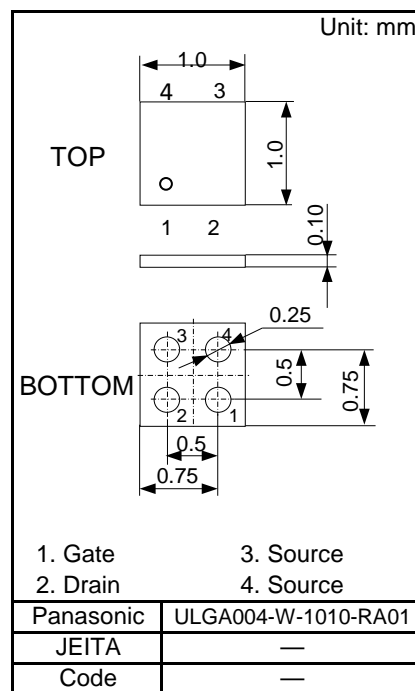
### ■ Absolute Maximum Ratings $T_a = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	VDS	12	V
Gate-Source Voltage	VGS	$\pm 8$	V
Drain Current	ID1 <sup>*1</sup>	3.9	A
	ID2 <sup>*2</sup>	6.5	
	ID3 <sup>*3</sup>	7.9	
Peak Drain Current	IDp1 <sup>*1*4</sup>	31	A
	IDp2 <sup>*2*4</sup>	52	
	IDp3 <sup>*3*4</sup>	63	
Power Dissipation	PD1 <sup>*1</sup>	0.37	W
	PD2 <sup>*2</sup>	0.94	
	PD3 <sup>*3</sup>	1.5	
Channel Temperature	Tch	150	$^\circ\text{C}$
Operating Ambient Temperature	Topr	-40 ~ +85	$^\circ\text{C}$
Storage Temperature	Tstg	-55 ~ +150	$^\circ\text{C}$

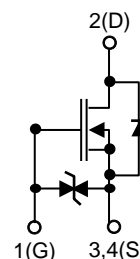
Note \*1 FR4 board (25.4mm×25.4mm×1.0mm), Min Cu 36mm<sup>2</sup> Copper

\*2 FR4 board (25.4mm×25.4mm×1.0mm), Full Cu

\*3 Ceramic substrate (70mm×70mm×1.0mm)

\*4  $t = 10\text{ }\mu\text{s}$ , Duty Cycle < 1%

### ■ Internal Connection



**■ Electrical Characteristics** Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0	12			V
Zero Gate Voltage Drain Current	IDSS	VDS = 12 V, VGS = 0			10	μA
Gate-Source Leakage Current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate Threshold Voltage	Vth	ID = 394 μA, VDS = 10 V	0.3		1.0	V
Drain-Source ON Resistance	RDS(on)	ID = 1.5 A, VGS = 4.5 V		14	24	mΩ
		ID = 1.0 A, VGS = 2.5 V		17	27	
		ID = 0.5 A, VGS = 1.8 V		21	36	
		ID = 0.25 A, VGS = 1.5 V		27	62	
Input Capacitance <sup>*1</sup>	Ciss	VDS = 10 V		490		pF
Output Capacitance <sup>*1</sup>	Coss	VGS = 0		184		
Reverse Transfer Capacitance <sup>*1</sup>	Crss	f = 1MHz		128		
Turn-on delay time <sup>*1,*2</sup>	td(on)	VDD = 6 V VGS = 0 to 4.5 V ID = 1.0 A		4.3		ns
Rise time <sup>*1,*2</sup>	tr			3.7		
Turn-off delay time <sup>*1,*2</sup>	td(off)			235		
Fall time <sup>*1,*2</sup>	tf			147		
Total Gate Charge <sup>*1</sup>	Qg	VDD = 6 V		7		nC
Gate to Source Charge <sup>*1</sup>	Qgs	VGS = 4.5 V		1.4		nC
Gate to Drain Miller Charge <sup>*1</sup>	Qgd	ID = 1.0 A		1.5		nC
Body Diode Forward Voltage	VF(D-S)	IF = 0.2A, VGS = 0V		0.6	1.2	V

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

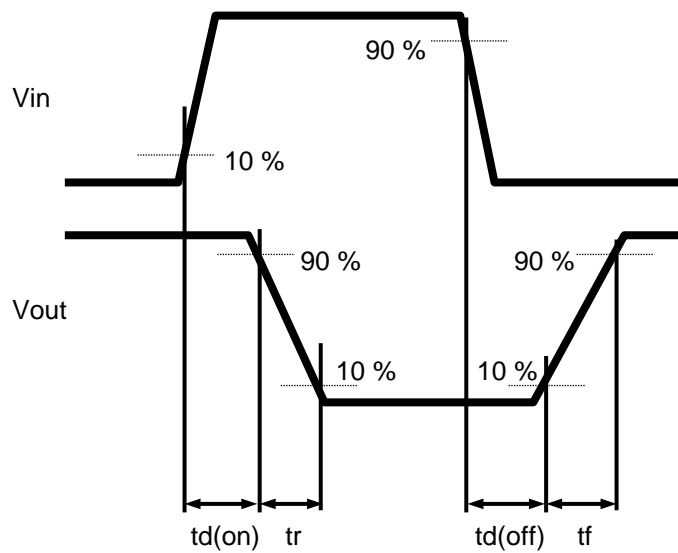
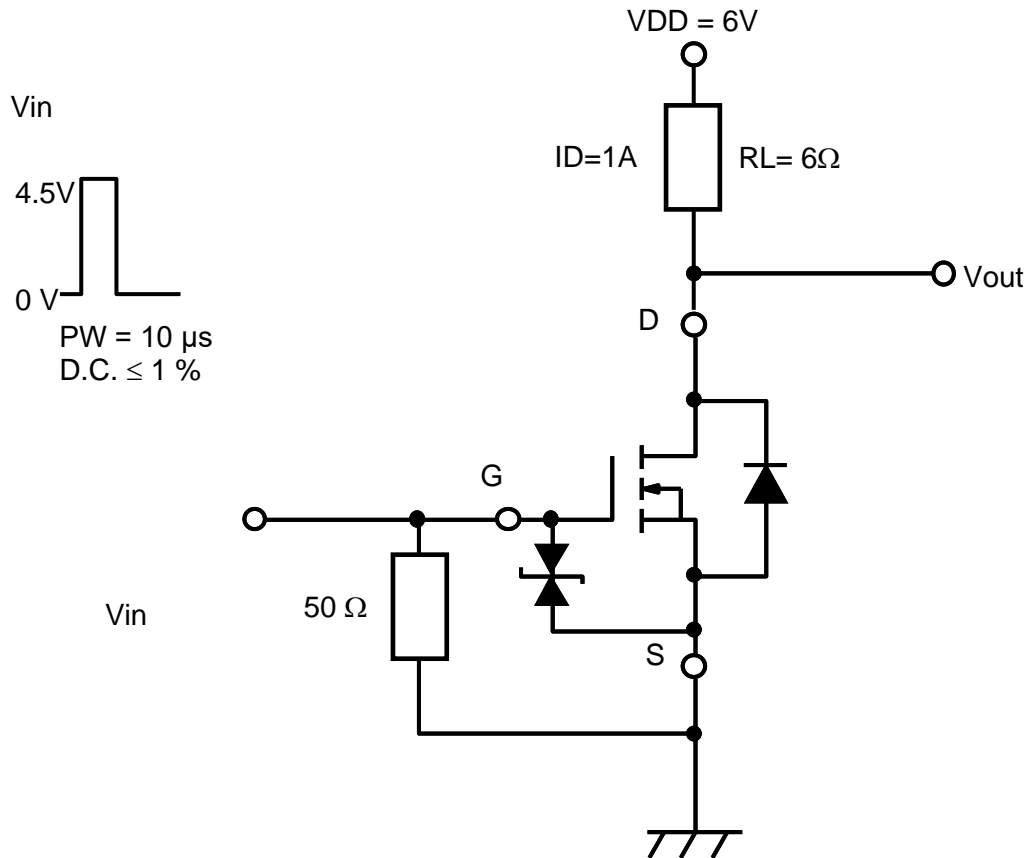
\*1 Guaranteed by design, not subject to production testing

\*2 Measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time

**■ Electrical State Discharge Characteristics**

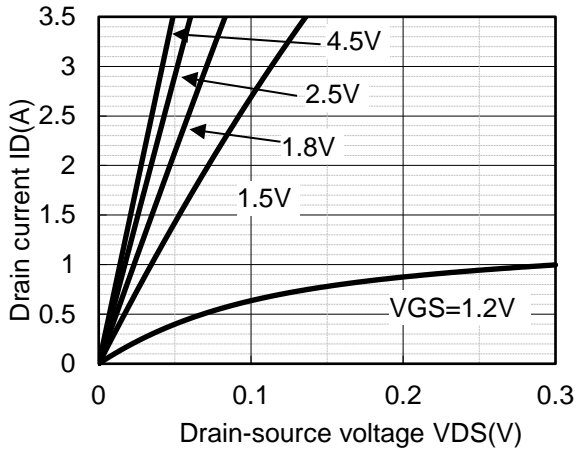
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human body model	HBM	C = 100 pF, R = 1.5 kΩ	H2	>2k to ≤ 4k	V
	Machine model	MM	C = 200 pF, R = 0 Ω	M2	>100 to ≤ 200	V

Note2: Measurement circuit

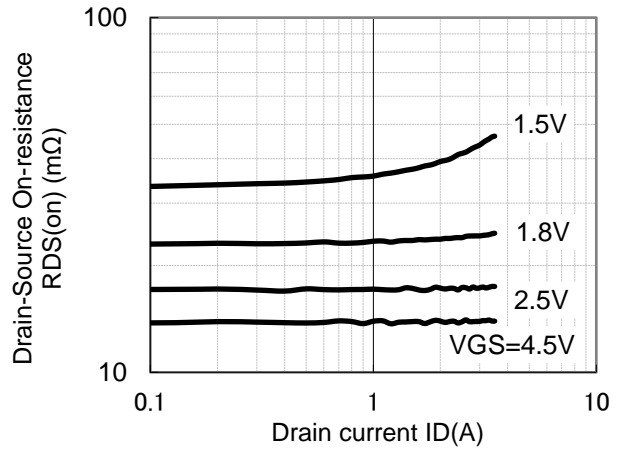




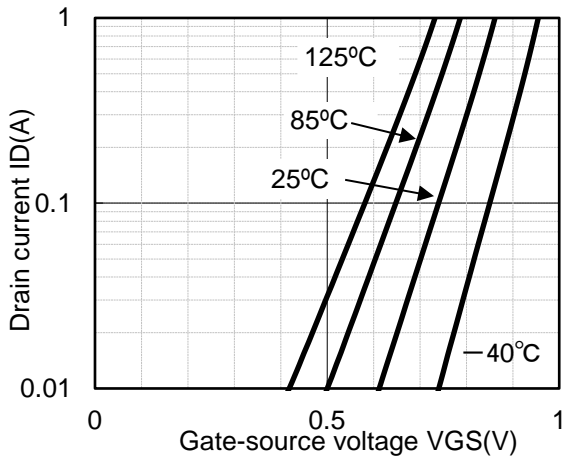
ID - VDS



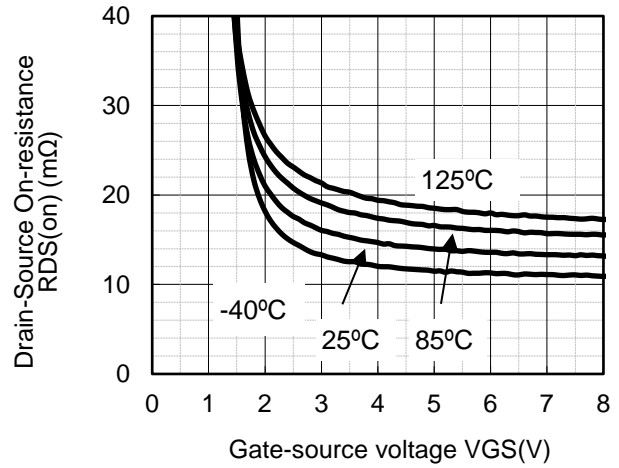
RDS(on) - ID



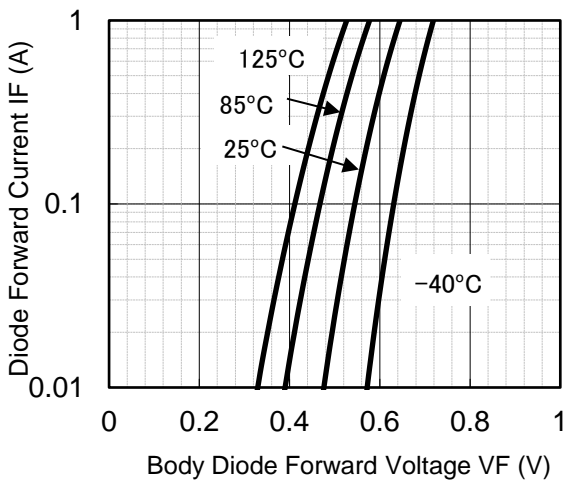
ID - VGS



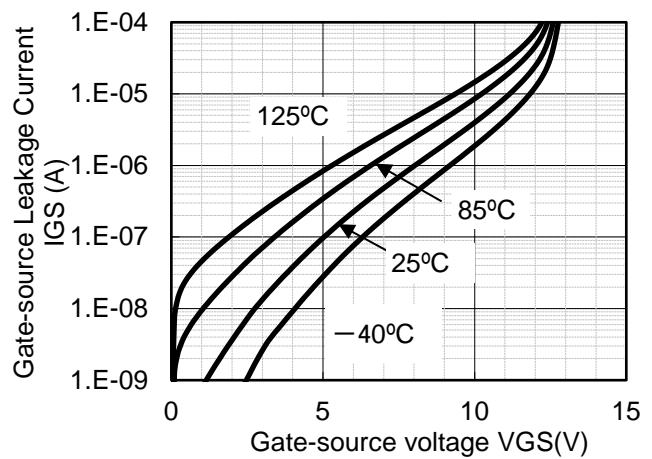
RDS(on) - VGS



IF - VF

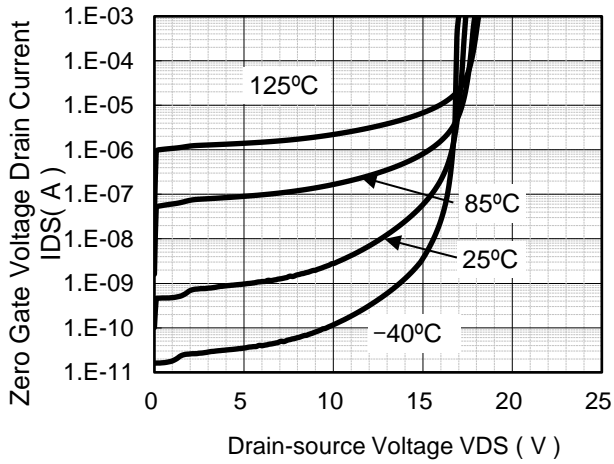


IGS - VGS

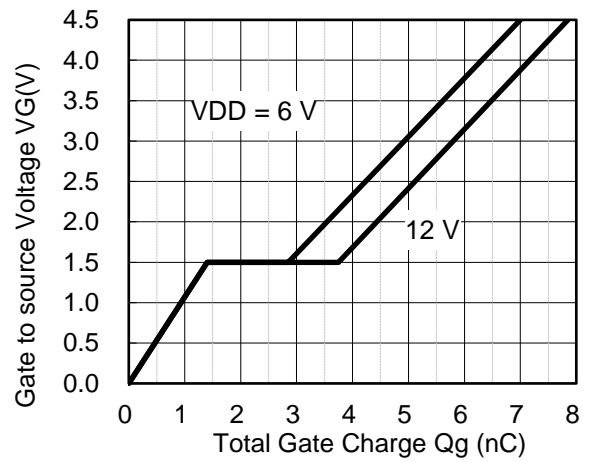




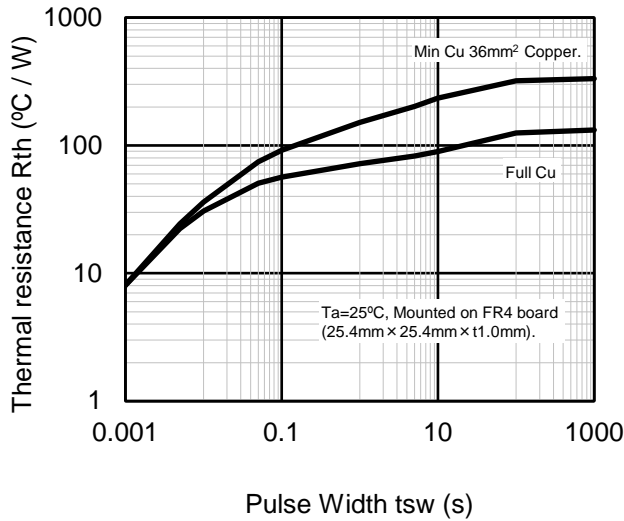
IDS - VDS



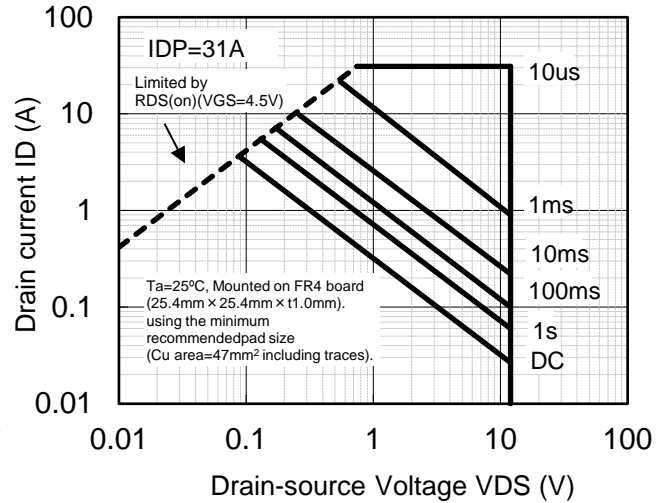
Dynamic Input/Output Characteristics



Rth - tsw

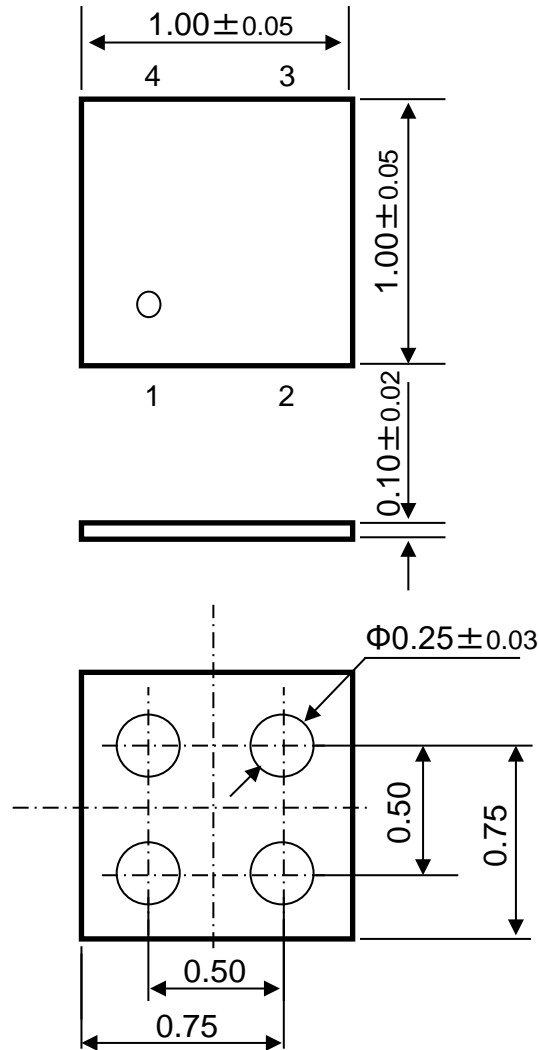


Safe Operating Area



■ ULGA004-W-1010-RA01

Unit: mm



■ Land Pattern (Reference)

