MAX20307

High-Frequency Optimized Configurable eGaN Driver

General Description

The MAX20307 is a configurable driver IC for enhancement mode Gallium Nitride (eGaN) FETs, optimized for high-frequency operation. The device is designed to drive both the high-side and low-side FETs in a half-bridge topology. The floating high-side driver is capable of driving a high-side eGaN FET operating up to 60V. A synchronous bootstrap technique provides the high-side bias voltage and is internally clamped at 5.2V. This clamping prevents the gate voltage from exceeding the maximum rated gate-source voltage of eGaN FETs.

The gate driver input signal is 3.3V TTL logic compatible, and can withstand input voltages up to 6V regardless of the V_{CC} voltage. Additionally, the MAX20307 features adaptive dead time control.

High-frequency H-bridge drive capability and adaptive dead time control make the MAX20307 ideal for high-efficiency buck applications. TTL logic compatibility allows the INH drive input to operate directly from the outputs of most PWM controllers allowing for flexible design.

The device covers wireless power (transmitting) levels from a few Watts to over 20 Watts making it well suited for wireless charging of various portable devices. High frequency optimization enables the use of wireless charging standards such as A4WP (6.78MHz) and ISM band (13.56MHz) wireless charging.

The MAX20307 is available in a space-saving, 15-bump, 1.2 x 2.0mm wafer-level package (WLP) and operate over the -40°C to +85°C extended temperature range.

Applications

- Switching Power Supply Topology Support
  - Half and Full-Bridge converters
  - Current Fed Push-Pull converters
  - Synchronous Buck converters
- A4WP Wireless Charging
- Medical Device Wireless Charging in ISM Band
- WPC and PMAT

Benefits and Features

- Flexible/Configurable Gate Drive
  - Single Control Input
  - 1A/5A Gate Source/Sink Current
- High-Efficiency SMPS Design
  - Low Loss Gate Drive: Optimized Bootstrap Circuit
  - Automatic Dead Time Control Optimized for Half-Bridge Converters
  - Programmable Maximum Dead Time
    - 0ns–9ns GPIO Controlled
  - Fast Propagation Delay (22ns)
- Safe Gate Drive
  - High-Side Floating Node Voltage up to 60V
  - Gate Supply Voltage UVLO
- Space-Saving Design
  - 0.4mm pitch 1.2mm x 2.0mm WLP

Ordering Information appears at end of data sheet.

19-100281; Rev 0; 3/18

maxim integrated™

Absolute Maximum Ratings

(Voltages reference to GND unless otherwise noted)

V_{CC} .....-0.3V to +6V
V_{IN} .....-0.3V to +66V
LO .....-0.3V to V_{CC} + 0.3V
HO .....V_{HS} – 0.3V to V_{HB} + 0.3V
HB.....-0.3V to +66V
HB to V_{CC} .....-0.3V to +60V
HS.....-0.3V to +60V
INL, INH, LDTY0, LDTY1, DTP0, DTP1 .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C):
WLP (derate 16.4mW/°C above +70°C.).....1312mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature..... -40°C to +150°C
Storage Temperature Range..... -40°C to +150°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....52°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 4.5 to 5.5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at V_{CC} = 5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}						
Supply Voltage Range	V_{CC}		4.5		5.5	V
V_{CC} Quiescent Current	I_Q	INH = 0V		6	13	mA
V_{CC} Operating Current	I_{CC}	f = 13.56MHz, C_L = 47pF		35		mA
V_{CC} Undervoltage Lockout (UVLO)	V_{CC_UVLO}	V_{CC} Rising	3.1	3.6	3.8	V
V_{CC} UVLO Hysteresis	$V_{CC\_UVLOHYS}$	V_{CC} Falling		0.1		V
eGaN GATE DRIVER						
LO Output Low	LO_{OUT_LOW}	I_{LO} = 100mA		<0.1		V
LO Output High	LO_{OUT_HIGH}	I_{LO} = 100mA		V_{CC} – 0.5V		V
HO Output Low	HO_{OUT_LOW}	I_{HO} = 100mA		<0.1		V
HO Output High	HO_{OUT_HIGH}	I_{HO} = 100mA, V_{BS} = V_{HB} - V_{HS}		V_{BS} – 0.5V		V
Peak Source Current ON				1		A
Peak Sink Current OFF				5		A

DC Electrical Characteristics (continued)

(V_{CC} = 4.5 to 5.5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at V_{CC} = 5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL CONTROL INPUT SIGNALS (INL, INH)						
Input High Threshold	V_{IH}	Rising Edge		52		$\%V_{CC}$
Input Hysteresis				3		$\%V_{CC}$
Input Pull Down	PD_{INH}		80	200	370	kΩ
DIGITAL IO SIGNALS (DTP0, DTP1, LDTY0, LDTY1)						
Input High Threshold	V_{IH}		1.6			V
Input Low Threshold	V_{IL}				0.4	V
Input Leakage Current	I_{LEAK}		-1		1	µA
Output High Leakage Current	$I_{LEAKOUT}$	V_{IO} = 5.5V	-1		1	µA
Output Low	V_{OL}	$I_{LDTY\_}$ = 10mA			0.4	V
TIMING CHARACTERISTICS (FIGURE 1)						
L Turn-On Propagation Delay	t_{PLON}	INH rising to LO rising (Note 3), DTP0 = DTP1 = 0		22		ns
L Turn-Off Propagation Delay	t_{PLOFF}	INH falling to LO falling, DTP0 = DTP1 = 0		22		ns
H Turn-On Propagation Delay	t_{PHON}	INH rising to HO rising (Note 3), DTP0 = DTP1 = 0		22		ns
H Turn-Off Propagation Delay	t_{PHOFF}	INH falling to HO falling, DTP0 = DTP1 = 0		22		ns
LO HO Delay Matching	t_{DMHON}	L off to H on		2		ns
HO LO Delay Matching	t_{DMLON}	H off and L on		2		ns
Minimum Input Signal Length		INH input deglitching duty cycle mismatch 4%		2		ns
LO Rise Time		C_L = 1000pF		5		ns
LO Fall Time		C_L = 1000pF		1		ns
HO Rise Time		C_L = 1000pF		5		ns
HO Fall Time		C_L = 1000pF		1		ns
Minimum Output Dead Time		(Note 4)		0		ns
Maximum Output Dead Time		(Note 4)		9		ns
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			150		°C
Thermal Hysteresis	T_{HYST}			20		°C

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 3: The specified propagation delay of a rising edge includes dead time.

Note 4: See Table 1 for details on configuring the dead time on MAX20307. The minimum and maximum dead time will vary with supply voltage.

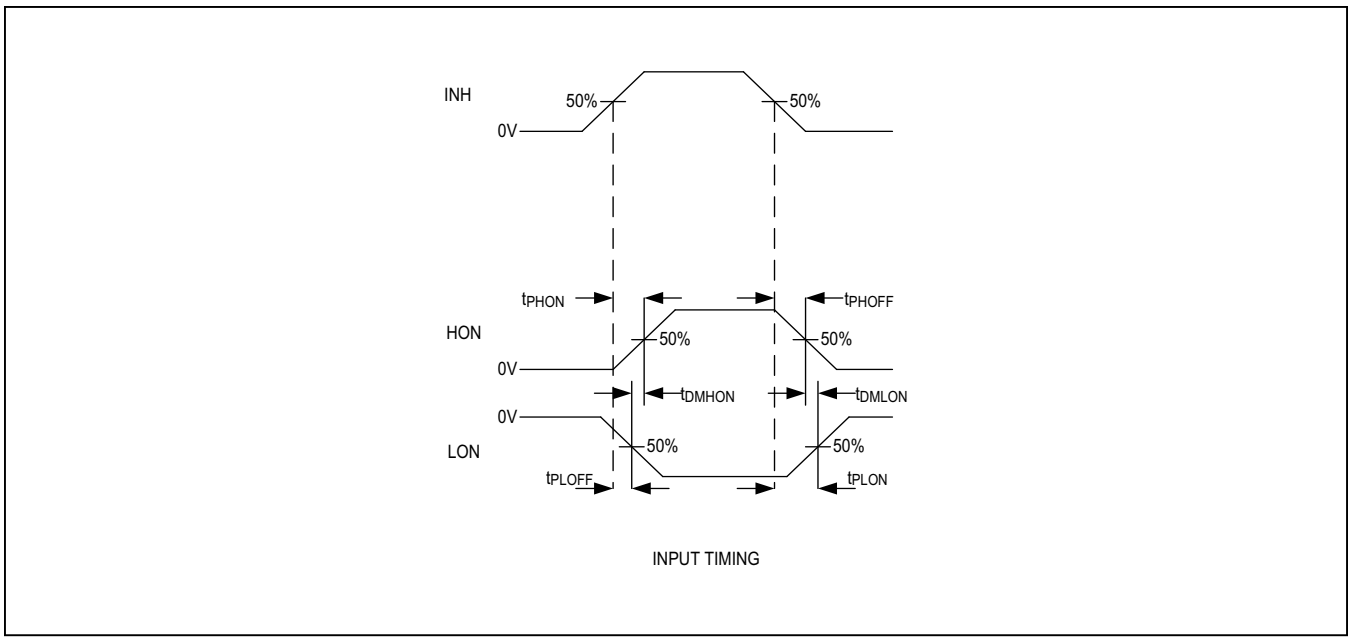
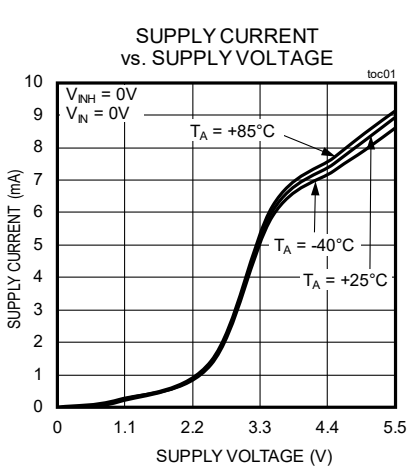
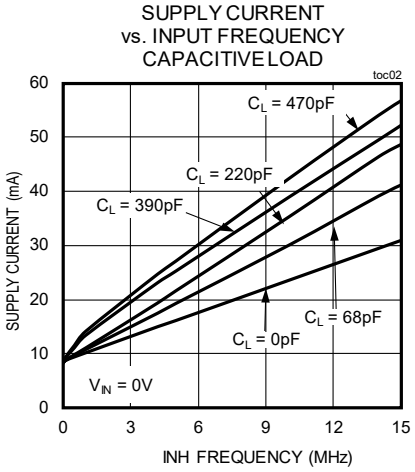


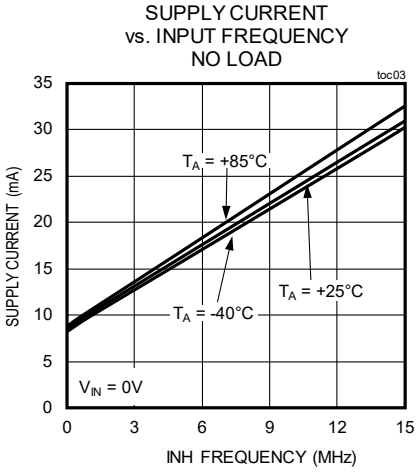
Figure 1. Timing Diagram

Typical Operating Characteristics

(V_{CC} = 5V, V_{IN} = 48V, T_A = +25°C unless otherwise noted.)



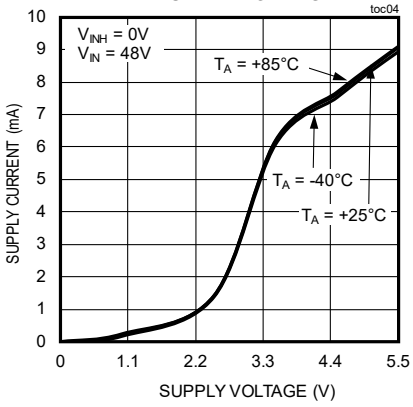




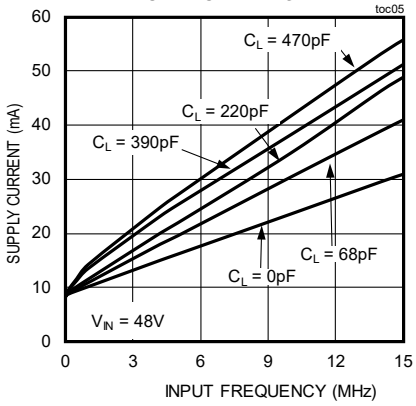
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{IN} = 48V, T_A = +25°C unless otherwise noted.)

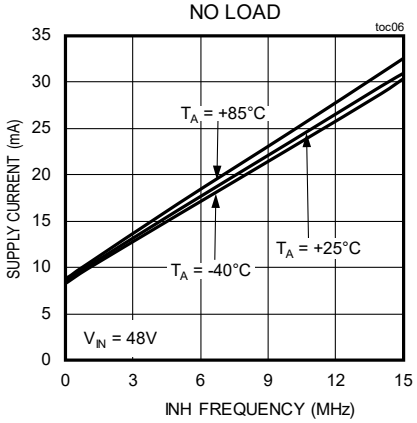
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



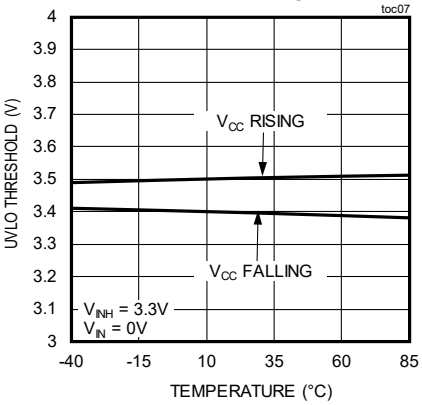
SUPPLY CURRENT
vs. INPUT FREQUENCY
CAPACITIVE LOAD



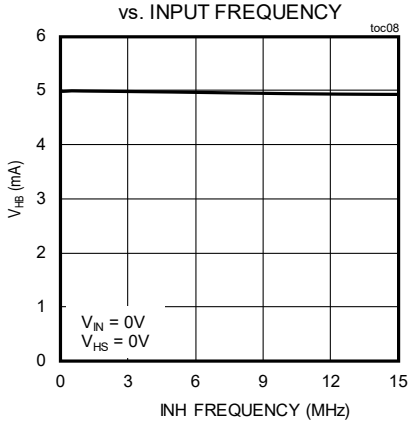
SUPPLY CURRENT
vs. INPUT FREQUENCY
NO LOAD



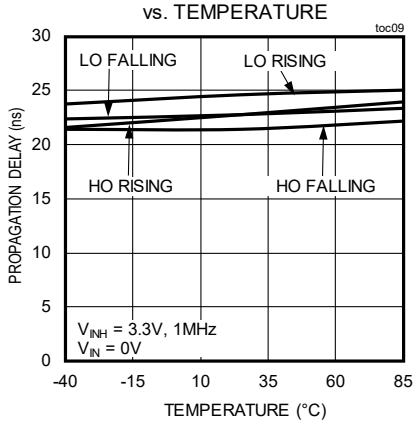
UVLO THRESHOLD
vs. TEMPERATURE



HB VOLTAGE
vs. INPUT FREQUENCY



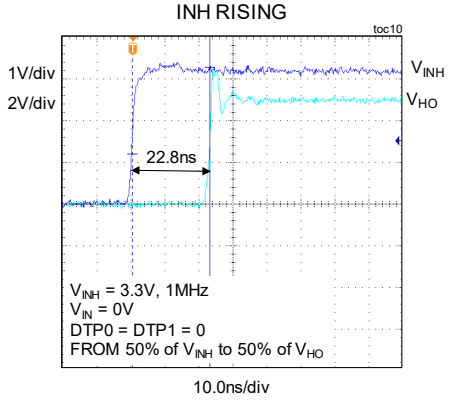
OUTPUT PROPAGATION DELAY
vs. TEMPERATURE



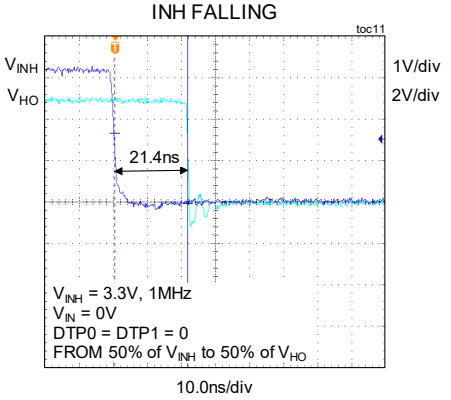
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{IN} = 48V, T_A = +25°C unless otherwise noted.)

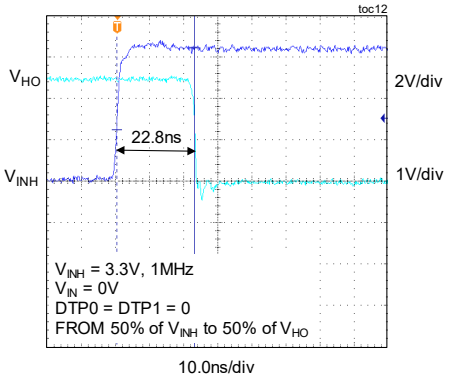
HO PROPAGATION DELAY
INH RISING



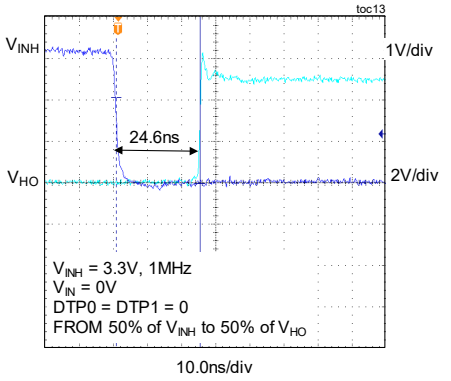
HO PROPAGATION DELAY
INH FALLING



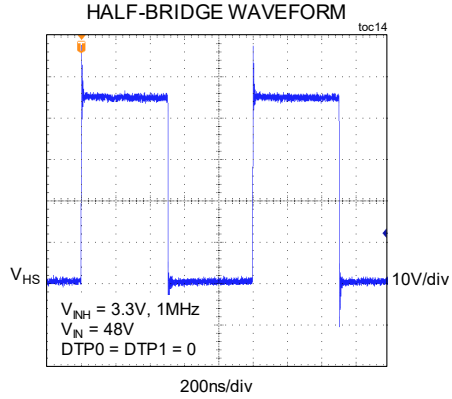
LO PROPAGATION DELAY
INH RISING



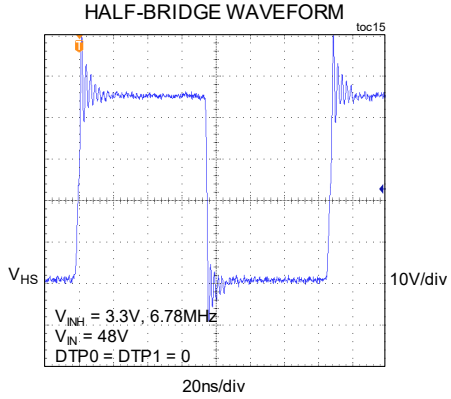
LO PROPAGATION DELAY
INH FALLING



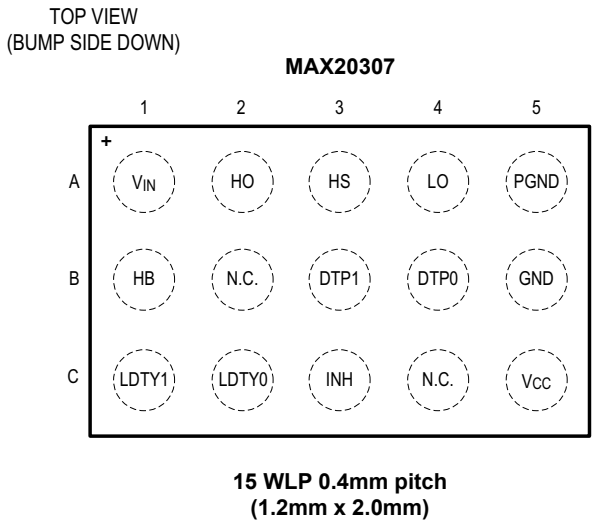
HALF-BRIDGE WAVEFORM



HALF-BRIDGE WAVEFORM



Pin Configurations

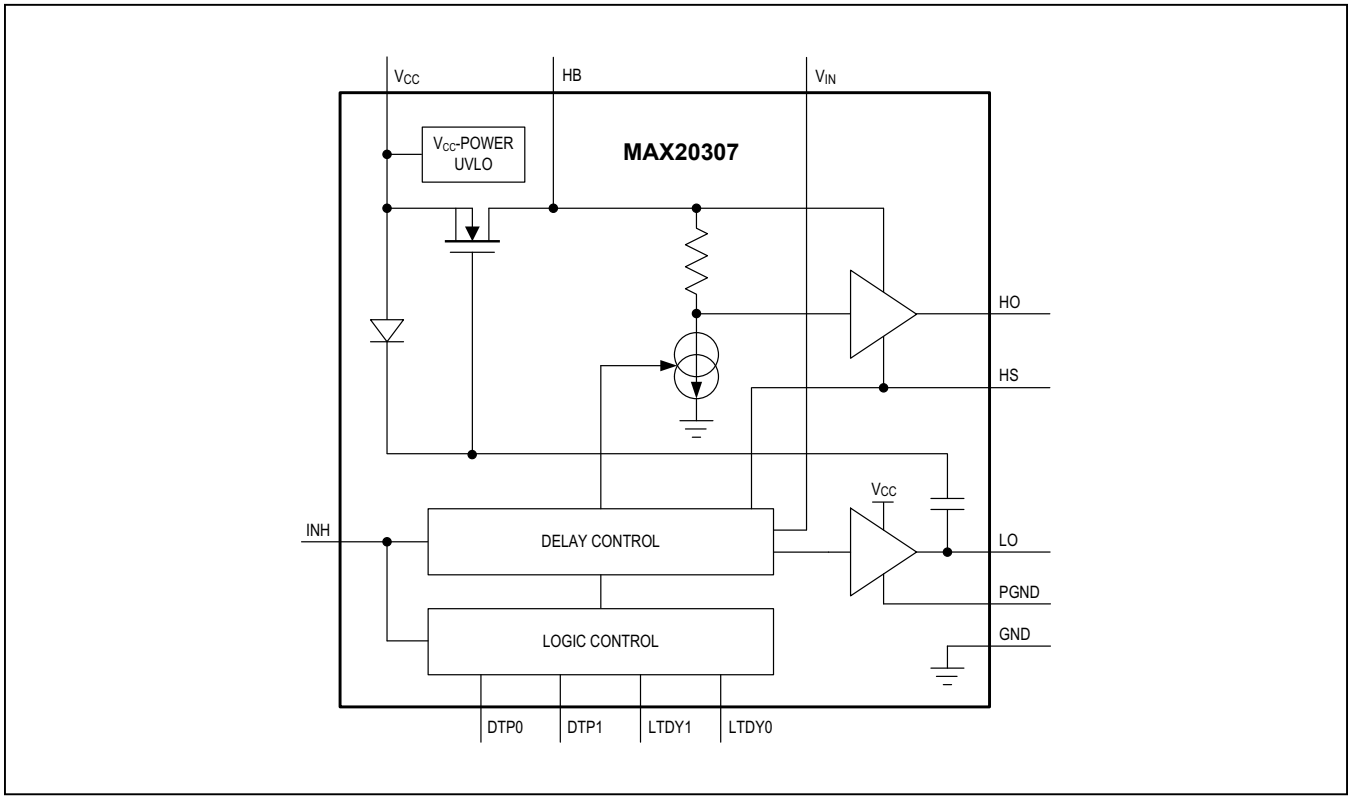


15 WLP 0.4mm pitch
(1.2mm x 2.0mm)

Bump Descriptions

BUMP	NAME	FUNCTION
A1	V_{IN}	High-Side Rail. Connect to drain of the high-side eGaN FET.
A2	HO	High-Side eGaN FET Gate Driver Output
A3	HS	High-Side eGaN FET Source Connection
A4	LO	Low-Side eGaN FET Gate Driver Output
A5	PGND	Low-Side eGaN FET Source Connection. Power ground. Connect to GND.
B1	HB	High-Side eGaN FET Gate Driver Bootstrap
B2, C4	N.C.	No Connect. Leave pin floating.
B3	DTP1	Maximum Dead Time Programming Bit 1 Input.
B4	DTP0	Maximum Dead Time Programming Bit 0 Input.
B4	GND	Ground
C1	LDTY1	Load Type Indicator for Capacitive Load. Open drain output.
C2	LDTY0	Load Type Indicator for Inductive Load. Open drain output.
C3	INH	Drive Input
C5	V_{CC}	Power

Block Diagram



Detailed Description

The MAX20307 is designed to drive the high-side and low-side eGaN FETs of a half-bridge configuration or two low-side eGaN FETs with a single-drive input. The device features adaptive dead time control to maximize switching efficiency, making the MAX20307 well suited for high-frequency switching converters.

The device features TTL logic compatible inputs and can withstand input voltages of up to +6V regardless of the V_{CC} voltage. This wide operating range enables most PWM controllers to directly drive the input of the MAX20307.

The asymmetrical sink/source gate drive outputs of the device are optimized for high-frequency applications. A low impedance path in the gate driver prevents accidental turn-on by the high dv/dt characteristic of HS switching transitions.

Power Consumption

The total power consumption of the device is critical as it ultimately determines the maximum operating frequency of the gate driver. Power losses in the MAX20307 are defined by the V_{CC} supply current. V_{CC} supplies the low-side gate drive circuit directly, but also powers the high-side circuit through the synch-FET circuit. Gate driver losses are proportional to the gate charge of the eGaN FET as it charges and discharges. The synch-FET reduces losses through the bootstrap clamping diode caused by the diode's reverse recovery charge (Q_{RR}).

Dead Time Control

An adaptive dead time control feature maximizes efficiency when the MAX20307 drives a half-bridge. The MAX20307 automatically increases or decreases the dead time between 0ns and the maximum dead time set by DTP0 and DTP1. This allows the device to minimize the losses caused by body diode conduction and reverse recovery while also avoiding shoot-through. Table 1 details the maximum dead time setting for a DTP_ configuration. Setting DTP0 and DTP1 to 0 gives the device full control of the dead time without delay.

Table 1. Maximum Dead Time Programming

DTP1	DTP0	DEAD TIME (ns)
0	0	0
0	1	3
1	0	6
1	1	9

Load Type Indicator

The MAX20307 features the ability to distinguish between inductive and capacitive loads. Two open-drain outputs, LDTY0 and LDTY1, indicate if the load connected to HS is capacitive or inductive. By connecting pullup resistors from LDTY0 and LDTY1 to the V_{CC} supply, the pins can signal the type of load attached. LDTY0 will output high if the load is inductive and LDTY1 will output high if the load is capacitive.

Applications Information

V_{CC} Bypass Capacitor

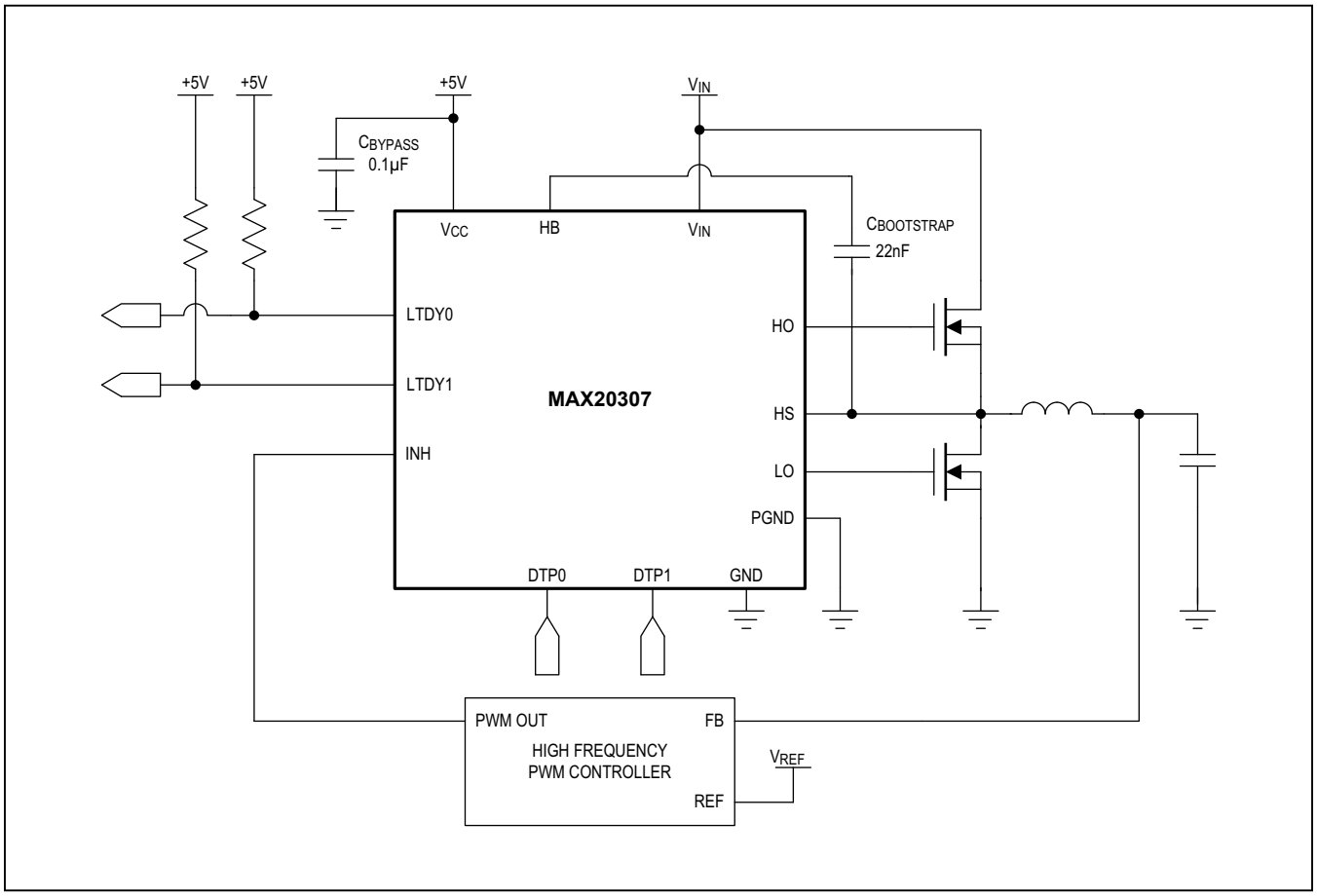
An external V_{CC} bypass capacitor provides the gate charge for the low- and high-side transistors and absorbs the reverse recovery charge of the bootstrap diode. A 0.1µF or larger ceramic capacitor with low ESR and low temperature coefficient is recommended. The bypass capacitor should be placed close to the V_{CC} pin of the devices to minimize parasitic inductance.

Bootstrap Capacitor

When driving a half-bridge configuration, the MAX20307 needs an external bootstrap capacitor to drive the high-side eGaN FET. The bootstrap capacitor is charged by the synch-FET whenever the HS is pulled to ground. Since the source to drain voltage drop of an eGaN FET is much higher than that of a typical PN junction diode, the MAX20307 features an internal clamping circuit with synch-FET control to prevent the gate drive voltage from exceeding the maximum gate-source voltage of the eGaN FET and damaging the high-side eGaN FET.

The bootstrap capacitor provides the gate charge for the high-side switch, DC bias power for HB UVLO circuit, and the clamping circuit. A 0.1µF for 1MHz applications or 22nF for 6.78MHz applications or larger ceramic capacitor with low ESR and low temperature coefficient are recommended. The bypass capacitor should be placed close to the HB pin of the devices to minimize parasitic inductance.

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20307EWL+	-40°C to +85°C	15 WLP
MAX20307EWL+T	-40°C to +85°C	15 WLP

+Denotes a lead (Pb)-free package/RoHS-compliant package
T = Tape and reel

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
15 WLP	W151E2+1	**21-1031**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—

