

TPIC2603

6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

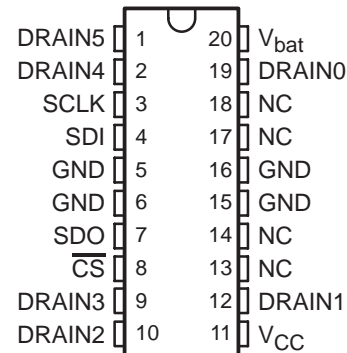
- Serial Control With Diagnostics
- Six Power DMOS Transistor Outputs of 350-mA Continuous Current
- Internal 60-V Inductive Load Clamp
- Independent ON-State Shorted-Load/Short-to-Battery Fault Detection on All Drain Terminals
- Independent OFF-State Open-Load Fault Sense on All Drain Terminals
- Transition of Drain Outputs to Low Duty Cycle Pulsed-Width-Modulation (PWM) Mode for Over-Current Condition
- Over-Battery-Voltage-Lockout Protection
- Over-Temperature Sense With Serial Interface Fault Status
- Fault Diagnostics Returned Through Serial Output Terminal
- Internal Power-On Reset of Registers
- CMOS Compatible Inputs With Hysteresis

description

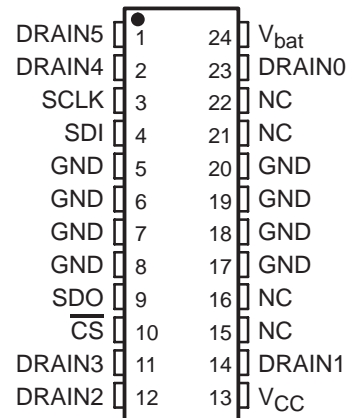
The TPIC2603 is a monolithic low-side driver which provides serial interface and diagnostics to control six on-board power DMOS switches. Each channel has independent OFF-state open-load sense, ON-state shorted-load/short-to-battery protection, over-battery-voltage-lockout protection, and over-temperature sense with fault status reported through the serial interface. The device also provides inductive voltage transient protection for each drain output. The TPIC2603 drives inductive and resistive loads such as relays, valves, and lamps.

Serial data input (SDI) is transferred through the serial register when \overline{CS} is low on low-to-high transitions of the serial clock (SCLK). Each string of data must consist of 8 or 16 bits of data. A logic high input data bit turns the respective output channel ON and a logic low data bit turns it OFF. \overline{CS} must be transitioned high after all of the serial data has been clocked into the device. A low-to-high transition of \overline{CS} transfers the last six bits of serial data to the output buffer, places the serial data out (SDO) terminal in a high-impedance state, and re-enables the fault register. Fault data for the device is sent out the SDO terminal. The first bit of the shift register is exclusively ORed with the fault registers. When a fault exists, the SDI data is inverted as it is transferred out of SDO. Fault data consists of fault flags for over-temperature (bit 6) and shorted/open-load (bits 0-5) for each of the six output channels. Fault register bits are set or cleared asynchronously, when \overline{CS} is high to reflect the current state of the hardware. The fault must be present when \overline{CS} is transitioned from high to low to be captured and reported in the serial fault data. New faults cannot be captured in the serial register when \overline{CS} is low.

**NE PACKAGE
(TOP VIEW)**



**DW PACKAGE
(TOP VIEW)**



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Copyright © 1996, Texas Instruments Incorporated

TPIC2603 6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

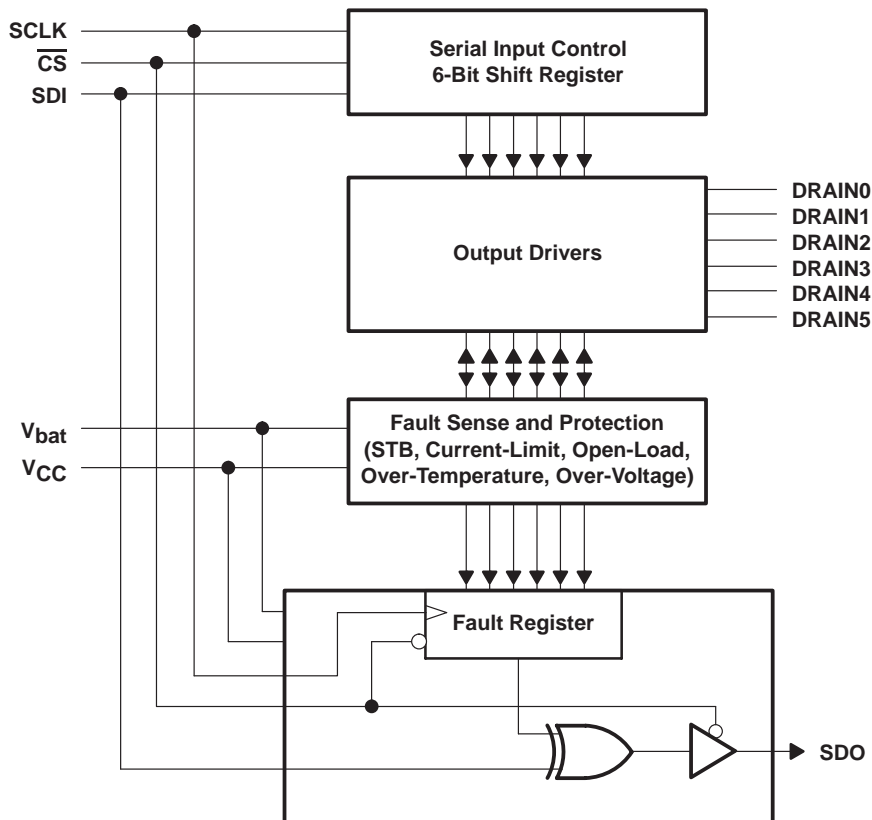
description (continued)

When an over-current or shorted-load fault occurs, the channel transits into a low duty cycle pulse-width-modulated (PWM) signal as long as the fault is present. More detail on fault detection operation is presented in the device operation section of this data sheet.

The TPIC2603 provides pulldown resistors on all active-high inputs except SCLK. A pullup resistor is used on \overline{CS} .

The TPIC2603 is characterized for operation over the operating case temperature of -40°C to 125°C .

functional block diagram



TPIC2603

6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

Terminal Functions

| TERMINAL NAME | NO.† | I/O | DESCRIPTION |
|--|---|-----|---|
| $\overline{\text{CS}}$ | 8 (10) | I | Chip select. The $\overline{\text{CS}}$ is an active-low input used to select the serial interface of the device. The device accepts serial input data and transmits fault data when $\overline{\text{CS}}$ is held low. An internal pullup resistor is provided on the $\overline{\text{CS}}$ input. |
| DRAIN0 DRAIN1 DRAIN2 DRAIN3 DRAIN4 DRAIN5 | 19 (23) 12 (14) 10 (12) 9 (11) 2 (2) 1 (1) | O | FET drain outputs. The DRAIN terminals are low-side switches for inductive and resistive loads. Each output provides an internal drain-gate clamp to snub inductive transients. |
| GND | 5, 6, 15, 16 (5, 6, 7, 8, 17, 18, 19, 20) | O | Ground. These terminals provide ground return paths for the device. |
| SCLK | 3 (3) | I | Serial clock. The SCLK clocks the shift register. Serial data is transferred into the SDI port and serial fault data is transferred out of the SDO port of the device on the rising edges of SCLK. |
| SDI | 4 (4) | I | Serial data input. The device receives serial data from the control device using the SDI. Serial input data can be configured in 8-bit or 16-bit data words. Refer to Figures 2 and 4 for input protocol. An internal pulldown resistor is provided on the SDI input. |
| SDO | 7 (9) | O | Serial data output. This 3-state output transfers fault data to the control device after the device has been selected by the $\overline{\text{CS}}$ terminal. |
| V _{bat} | 20 (24) | I | Battery voltage. The V _{bat} terminal monitors the battery voltage to detect over-voltage conditions. |
| V _{CC} | 11 (13) | I | Supply voltage. The V _{CC} terminal receives a 5-V supply for internal logic. |

† Terminal numbers listed in parenthesis are for the 24-pin DW package.

absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)‡

| | |
|---|------------------------------|
| Logic supply voltage range, V _{CC} (see Note 1) | –0.3 V to 7 V |
| Battery supply voltage range, V _{bat} | –1.5 V to 60 V |
| Logic input voltage range, V _I | –0.3 V to 7 V |
| Power DMOS drain-to-source voltage, V _{DS} (see Note 2) | 68 V |
| Continuous drain current, each output, all outputs on, I _D , T _C = 25°C | 350 mA |
| Pulsed drain current, single output, I _{DM} , T _C = 25°C (see Note 3) | 2.25 A |
| Single-pulse avalanche energy, E _{AS} (see Figure 11) | 100 mJ |
| Continuous total power dissipation | See Dissipation Rating Table |
| Avalanche current, I _{AS} (see Note 4) | 1 A |
| Operating virtual junction temperature range, T _J | –40°C to 150°C |
| Storage temperature range, T _{stg} | –55°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to GND.
 2. Each power DMOS source is internally connected to GND.
 3. Pulse duration ≤ 100 μs and duty cycle ≤ 2%.
 4. DRAIN supply voltage = 13 V, starting junction temperature (T_{J(S)}) = 25°C, L = 150 mH, I_{AS} = 1 A (see Figure 11).



TPIC2603

6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

DISSIPATION RATING TABLE

| PACKAGE | $T_C \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$ | $T_C = 125^\circ\text{C}$ POWER RATING |
|---------|---|---|---|
| DW | 1750 mW | 14 mW/ $^\circ\text{C}$ | 350 mW |
| NE | 2500 mW | 20 mW/ $^\circ\text{C}$ | 500 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|------------------------------------|--------------|--------------|----------|------------------|
| Logic supply voltage, V_{CC} | 4.5 | 5 | 5.5 | V |
| Battery supply voltage, V_{bat} | 5.5 | 12 | 25 | V |
| High-level input voltage, V_{IH} | $0.7 V_{CC}$ | | V_{CC} | V |
| Low-level input voltage, V_{IL} | 0 | $0.3 V_{CC}$ | | V |
| Operating case temperature, T_C | -40 | 125 | | $^\circ\text{C}$ |

electrical characteristics, $T_C = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | | | |
|-----------------|--|---|---|----------------------|--------------|---------------|------------------|---------------|---|
| V_{bat} | Battery supply voltage | Normal operation | | 5.5 | 25 | V | | | |
| I_{bat} | Battery supply current | $V_{CC} = 5\text{ V}$ | | 5 | | mA | | | |
| | | $V_{CC} = 0$ | | 50 | | μA | | | |
| V_{CC} | Logic supply voltage | | | 4.5 | 5.5 | V | | | |
| I_{CC} | Logic supply current | All outputs off, $V_{bat} = 5.5\text{ V}$ | | 5 | | mA | | | |
| $V_{(turn-on)}$ | V_{CC} turn-on voltage (logic operational) | $V_{bat} = 5.5\text{ V}$, Check output functionality | | 4.5 | | V | | | |
| $V_{(ov)}$ | Over-battery voltage shutdown | Gate disabled | | 30 | 38 | V | | | |
| $V_{hys(ov)}$ | Over-battery voltage reset hysteresis | | | 0.4 | 2 | V | | | |
| $r_{DS(on)}$ | Drain-to-source on-state resistance | $V_{bat} = 13\text{ V}$ | $I_O = 0.35\text{ A}$, $T_C = 25^\circ\text{C}$ | 0.7 | 1 | Ω | | | |
| | | $V_{bat} = 5.5\text{ V}$ | | 1.7 | 2.3 | | | | |
| | | $V_{bat} = 13\text{ V}$ | $I_O = 0.35\text{ A}$, $T_C = 125^\circ\text{C}$ | 1.2 | 1.7 | | | | |
| | | $V_{bat} = 5.5\text{ V}$ | | 2.7 | 3.8 | | | | |
| I_L | On-state current limit | 0.8 | 2 | 5 | A | | | | |
| $I_{L(sense)}$ | Over-current sense | 0.8 | 1.5 | 3 | A | | | | |
| I_{IH} | Input pullup current | $\text{GND} < V_I < 0.7 V_{CC}$, $\overline{\text{CS}}$ input only | | -5 | -10 | -50 | μA | | |
| I_{IL} | Input pulldown current | $0.3 V_{CC} < V_I < V_{CC}$, All other inputs | | 2.5 | 10 | 25 | μA | | |
| $I_{D(off)}$ | Off-state drain current | $V_{load} = V_{bat} = 14.5\text{ V}$ | | 20 | 40 | 80 | μA | | |
| $I_{O(sleep)}$ | Sleep-state output current | $V_{bat} < 0.5\text{ V}$, | $V_{CC} < 0.5\text{ V}$, | Load = 14 V | | 50 | μA | | |
| V_{OH} | High-level serial output voltage | $I_O = 1\text{ mA}$ | | $0.8 V_{CC}$ | | V | | | |
| V_{OL} | Low-level serial output voltage | $I_O = 1\text{ mA}$ | | 0.2 | 0.4 | V | | | |
| I_{OZ} | High impedance state output current | $V_{CC} = 5.5\text{ V}$ to 0 V , | SDO output | | -10 | 1 | 10 | μA | |
| $V_{(BR)DSX}$ | Drain-to-source breakdown voltage | dc < 1%, | $t_w = 100\ \mu\text{s}$, | $I_O = 20\text{ mA}$ | | 52 | 58 | 68 | V |
| $T_{j(sense)}$ | Thermal flag | | | 150 | 170 | 185 | $^\circ\text{C}$ | | |
| $T_{j(hys)}$ | Thermal flag hysteresis | | | 5 | 10 | 15 | $^\circ\text{C}$ | | |
| $V_{(open)}$ | Open-load detection voltage | | | $0.3 V_{CC}$ | $0.7 V_{CC}$ | | V | | |



TPIC2603

6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

switching characteristics, $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-----|-----|-----|---------------|
| t_w | Clock cycle period pulse duration, SCLK | See Figure 1 | | 250 | 555 | ns |
| $t_{wH}(\text{SCLK})$ | Pulse duration, SCLK high | See Figure 1 | | 100 | 248 | ns |
| $t_{wL}(\text{SCLK})$ | Pulse duration, SCLK low | See Figure 1 | | 100 | 248 | ns |
| t_{pd1} | Propagation delay from falling edge of $\overline{\text{CS}}$ to SDO valid | $\overline{\text{CS}} = 0.8\text{ V}$ to SDO low impedance (see Figure 1) | | 150 | 300 | ns |
| t_{pd2} | Propagation delay from rising edge of $\overline{\text{CS}}$ to SDO 3-state | $\overline{\text{CS}} = 2\text{ V}$ to SDO 3-state | | 150 | 200 | ns |
| t_{pd3} | Propagation delay from SCLK to SDO valid | $\overline{\text{CS}} < 0.8\text{ V}$ | | 80 | 172 | ns |
| $t_r(\text{SDO})$ | Rise time of SDO | $C_{load} = 200\text{ pF}$ | | 30 | 50 | ns |
| $t_f(\text{SDO})$ | Fall time of SDO | $C_{load} = 200\text{ pF}$ | | 30 | 50 | ns |
| $t_{(stb)}$ | Short-to-battery/shorted-load/open-load deglitch time | See Figures 5 and 6 | 25 | 70 | 100 | μs |
| $t_{d(on)}$ | Turn-on delay time, rising edge of $\overline{\text{CS}}$ to drain | $V_{bat} = 14\text{ V}$, $R_{load} = 30\ \Omega$ | 0.4 | 5 | 10 | μs |
| $t_{d(off)}$ | Turn-off delay time, rising edge of $\overline{\text{CS}}$ to drain | | 0.4 | 5 | 15 | |
| $t_r(\text{drain})$ | Rise time of drain terminal | | 0.4 | 5 | 10 | |
| $t_f(\text{drain})$ | Fall time of drain terminal | | 0.4 | 5 | 10 | |
| $f(\text{SCLK})$ | Serial clock frequency | | 1.8 | 4 | | MHz |
| $t_{cyc}(\text{ref})$ | Short-to-battery sense cycle time | See Figure 5 | 1.6 | 4 | 6.4 | ms |
| $t_w(\text{sense})$ | Short-to-battery sense pulse duration | See Figure 5 | 25 | 70 | 100 | μs |
| t_{su1} | Setup to/from the fall edge of $\overline{\text{CS}}$ to the rising edge of SCLK | See Figure 1 | | 150 | 200 | ns |
| $t_{su}(\text{SDI})$ | Setup time, SDI to SCLK | See Figure 1 | | 25 | 55 | ns |
| $t_h(\text{SDI})$ | Hold time, SDI after SCLK | See Figure 1 | | 10 | 55 | ns |

thermal resistance

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|--|------------------------------|-----|-----|------------------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | All outputs with equal power | | 50 | $^\circ\text{C}$ |
| $R_{\theta JC}$ | Junction-to-case thermal resistance | All outputs with equal power | | 10 | $^\circ\text{C}$ |



TPIC2603 6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

PRINCIPLES OF OPERATION

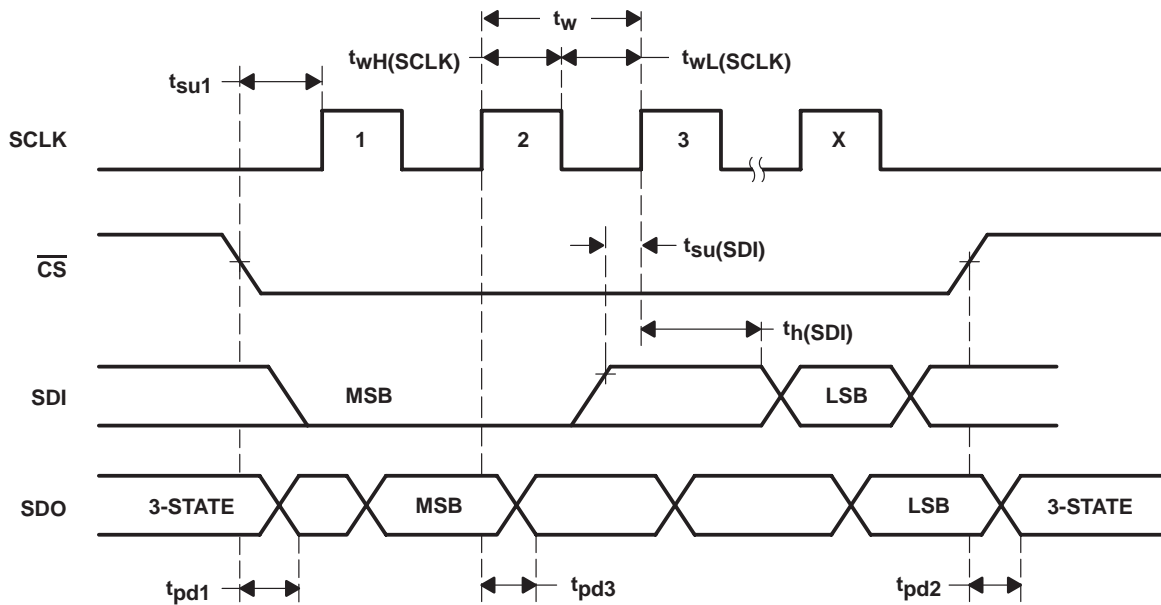


Figure 1. Switching Characteristics

serial interface

Control information is transferred into the TPIC2603 through the serial interface. The serial interface consists of a serial clock (SCLK), chip select (\overline{CS}), serial data input (SDI), and serial data output (SDO). Serial data is shifted, most significant bit (MSB) first, into the SDI shift register on the rising edge of the first SCLK after \overline{CS} has transitioned from high to low. The controller must shift either eight bits or sixteen bits of data into the device with the last six bits of input data containing control information for the output drivers. Data bits preceding the output control information should be set to 0. A low-to-high transition on \overline{CS} latches the contents of the last six bits of the serial shift register into the output buffer. A low input to SDI turns the corresponding parallel output OFF and a high input will turn the output ON (see Figure 2).

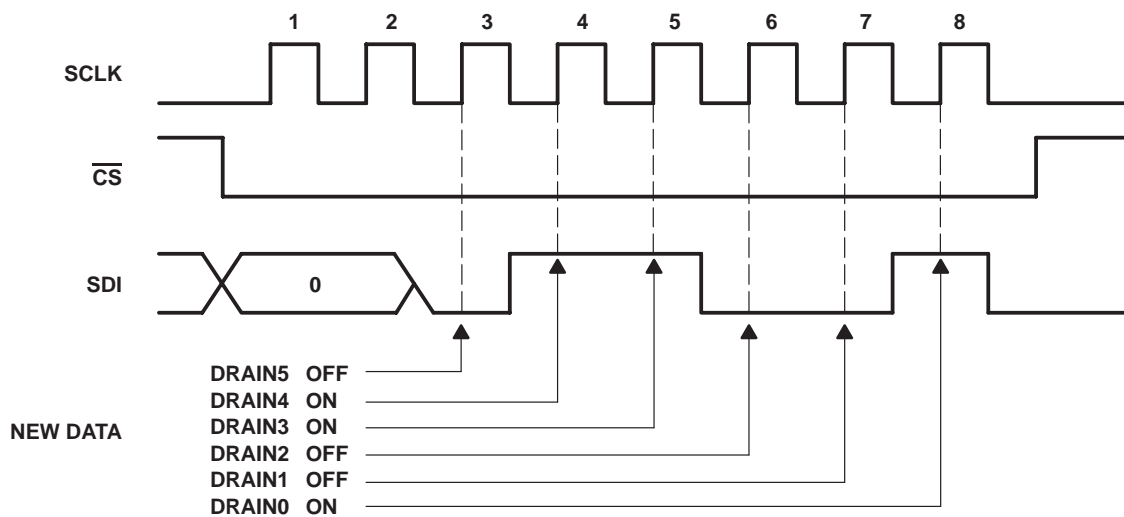


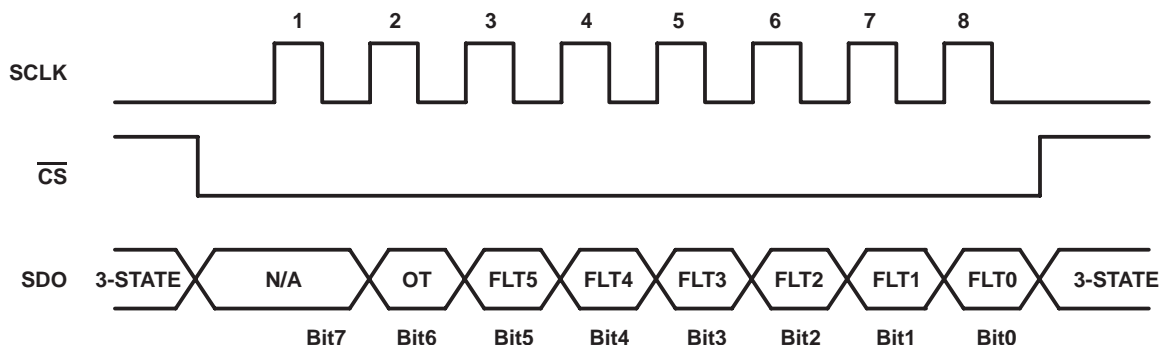
Figure 2. Serial Input Control



PRINCIPLES OF OPERATION

serial interface (continued)

Fault isolation data for each channel and global over-temperature status is transferred to the control device using the serial interface. Fault status for the TPIC2603 is captured as \overline{CS} transits low. The fault interface monitors the SDI terminal and exclusively ORs the respective input control bit with the corresponding fault information bit stored in the fault register. Each exclusive ORed fault bit is transferred out the SDO terminal on the rising edge of the SCLK. Serial data can be transferred in 8-bit or 16-bit words as illustrated in Figure 4, with fault data appearing in the first 8-bits of serial output data. The \overline{CS} must be transited high after the serial transfer has completely latched the new control data into the output control buffer and re-enable fault reporting on the device (see Figures 3 and 4).



- NA = Unused
- OT = Over-temperature fault bit
- FLT5 = Shorted or open-load fault on channel 5
- FLT4 = Shorted or open-load fault on channel 4
- FLT3 = Shorted or open-load fault on channel 3
- FLT2 = Shorted or open-load fault on channel 2
- FLT1 = Shorted or open-load fault on channel 1
- FLT0 = Shorted or open-load fault on channel 0

NOTE A: MSB is the first bit transferred.

Figure 3. Serial Output Control

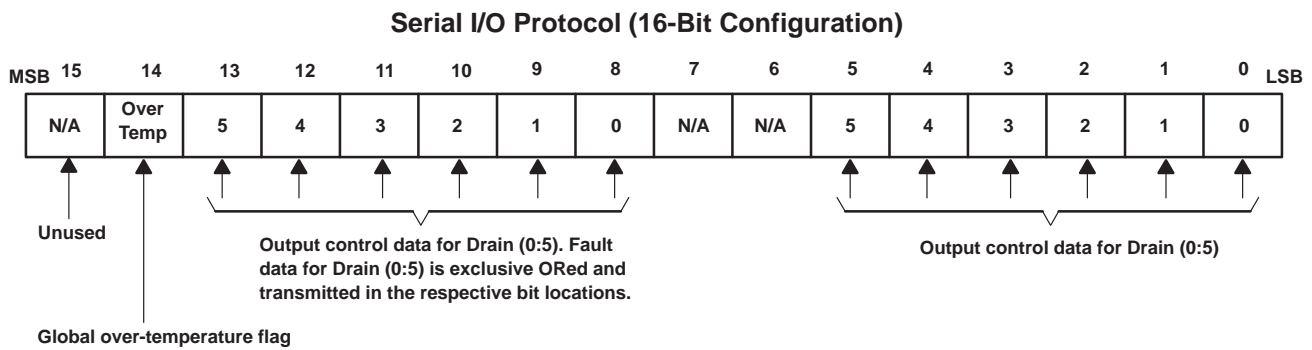
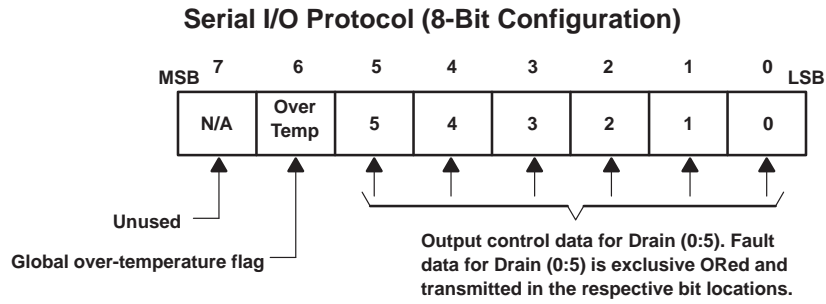
TPIC2603

6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

PRINCIPLES OF OPERATION

serial interface (continued)



NOTE A: MSB is the first bit transferred.

Figure 4. Serial Data Fault Protocol

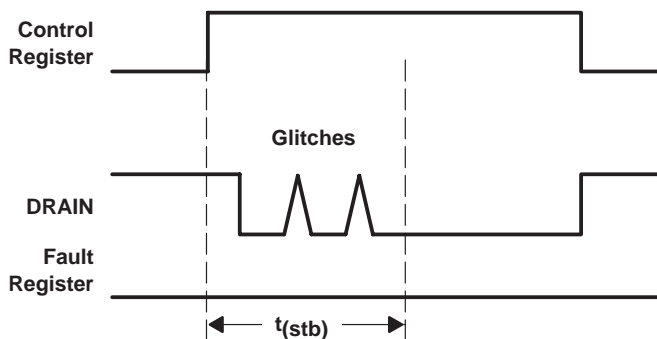
PRINCIPLES OF OPERATION

fault sense/protection circuitry

over-current/short-to-battery sensing and protection

The internal fault protection circuitry of the TPIC2603 monitors the drain current for each channel. Each channel offers two levels of protection from over-current conditions. The first level is a current-limit protection which through the internal FET prevents the switching current from exceeding the on-state current limit. The second level of protection transits the output to a low duty cycle PWM mode when the current exceeds the over-current sense threshold. The PWM mode protection is enabled approximately 70 μ s after the output has been turned on. The output remains in the PWM mode until the shorted-load condition has been corrected and then automatically returns to normal operation. Figure 5 illustrates device operation under an over-current or shorted-load condition.

NORMAL



SHORTED-LOAD

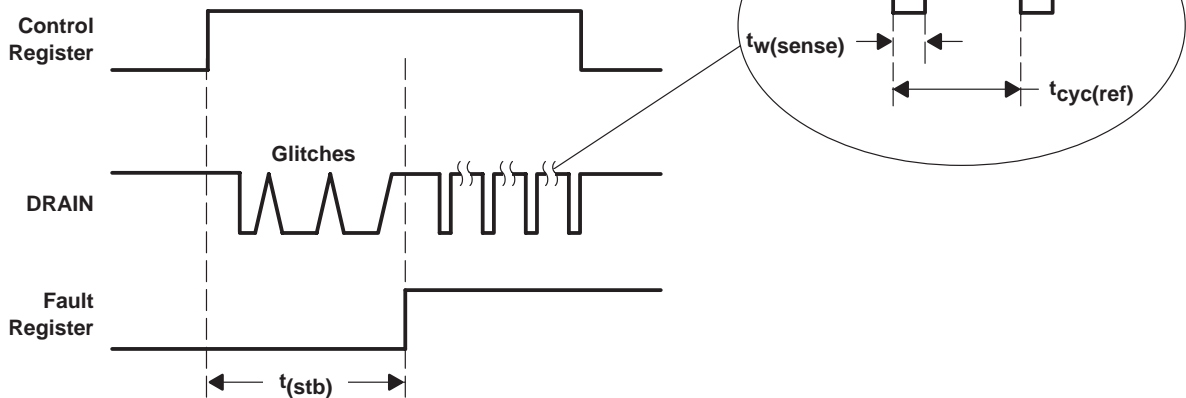


Figure 5. Shorted-Load Condition

TPIC2603

6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

PRINCIPLES OF OPERATION

open-load/short-to-ground sensing

The TPIC2603 checks for open-load and short-to-ground conditions when the output is turned OFF. When the output turns OFF, a 40- μ A current source switches onto the drain. Under normal conditions, the load provides adequate current to overcome the current source and the drain voltage remains above the open-load detection threshold. When the output is open, then the current source pulls the drain low and an open-load condition is flagged. The open-load test is enabled approximately 70 μ s after the output turns OFF to allow the drain to stabilize. Figure 6 illustrates device operation under open-load conditions.

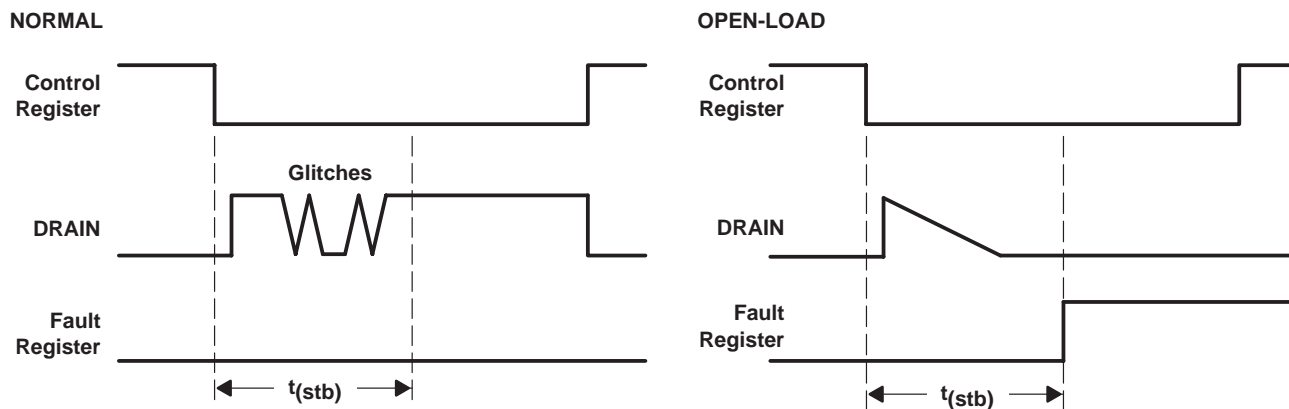


Figure 6. Open-Load Condition

over-voltage sensing and protection

The TPIC2603 monitors the V_{bat} input terminal to protect the device and load from over-battery voltage conditions. The device disables all of the drain outputs when V_{bat} goes above 35 V. An over-battery voltage hysteresis is provided to prevent the outputs from transiting ON and OFF erratically near the over-voltage threshold. The device automatically returns to normal operation after the over-voltage condition has been corrected. Figure 7 illustrates device operation under an over-battery voltage condition.

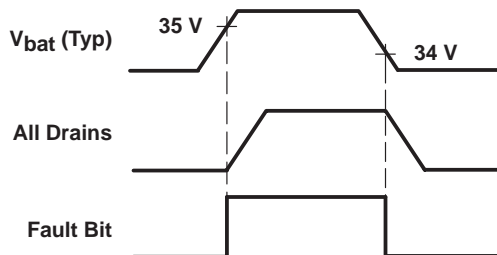


Figure 7. Over-Battery Voltage Condition

PRINCIPLES OF OPERATION

over-temperature sensing

The TPIC2603 monitors the junction temperature of the die to detect over-temperature conditions which may damage the device. When the junction temperature goes above approximately 170°C, the fault logic sets the global over-temperature fault bit. An over-temperature fault is reported using the serial interface on bit 6 (for 8-bit configuration) or bit 14 (for 16-bit configuration). The global over-temperature fault output in the serial data is exclusively ORed with the second bit (bit 6 for 8-bit configuration or bit 14 for 16-bit configuration) of data input to the SDI terminal. Bit 6 or bit 14 of the input data should be set low. Over-temperature faults are for informational purposes only and do not affect the state of the drains. Figure 8 illustrates device operation under over-temperature conditions.

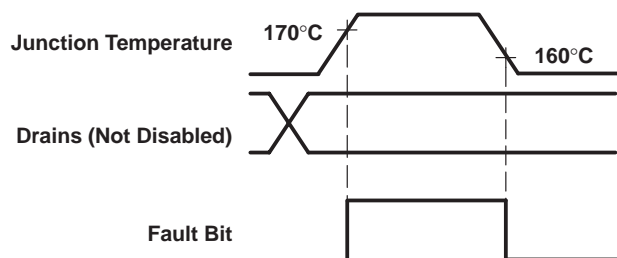
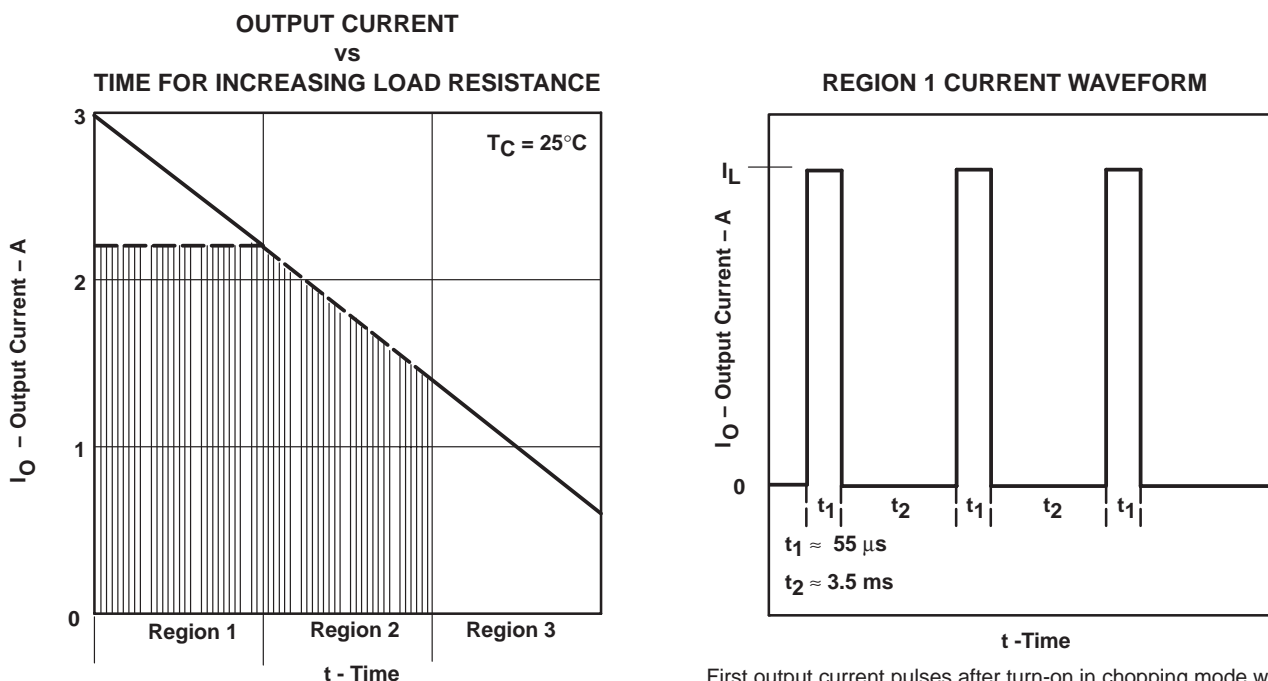


Figure 8. Over-Temperature Sense

PARAMETER MEASUREMENT INFORMATION



First output current pulses after turn-on in chopping mode with resistive load.

- NOTES: A. Region 1 – Analog current limit holds the maximum current while the device runs in chop mode.
 B. Region 2 – Analog current limit is removed but device continues in chop mode.
 C. Region 3 – Current is below chop mode sense; therefore, it is in normal operation. Variable load is resistance over time.

Figure 9. Chopping-Mode Characteristics



TPIC2603 6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

PARAMETER MEASUREMENT INFORMATION

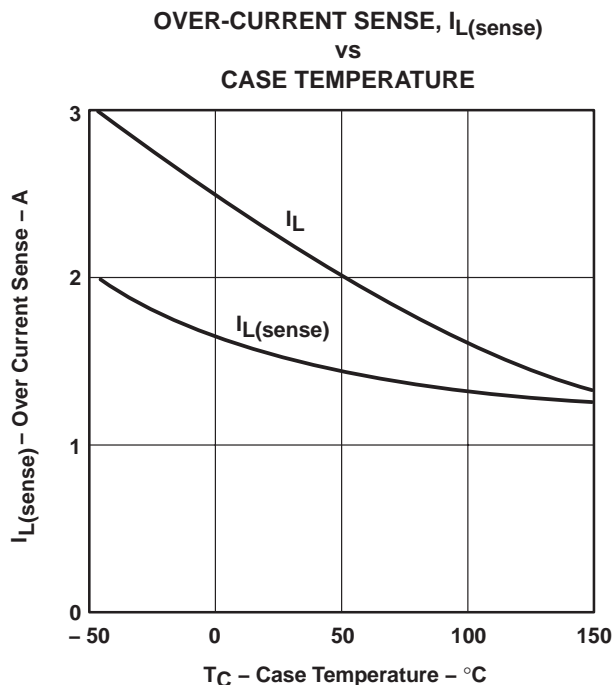
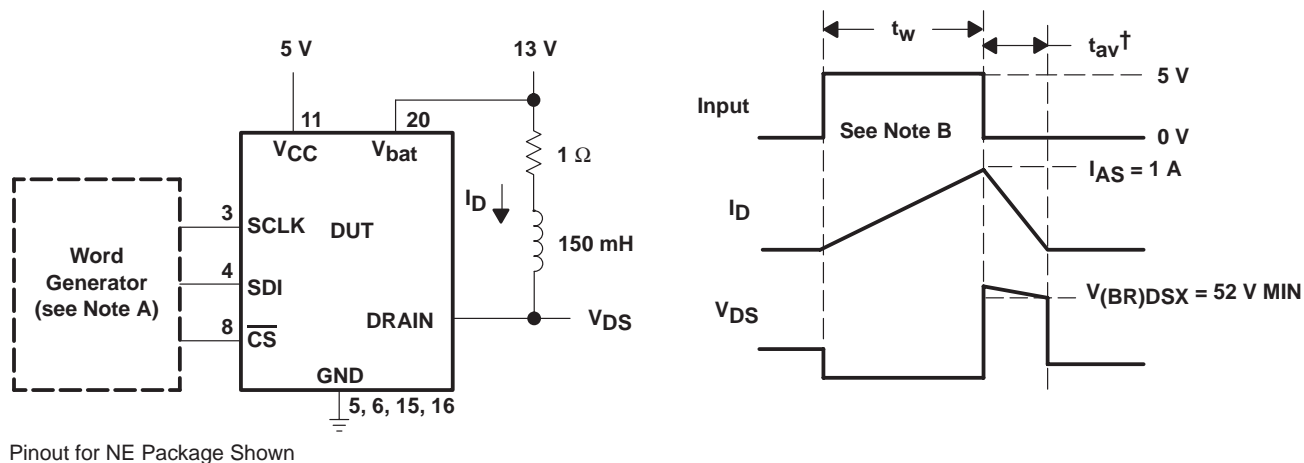


Figure 10



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

† Non-JEDEC symbol for avalanche time.

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.

B. Input pulse duration, t_w , is increased until peak current $I_{AS} = 1$ A.
Energy test level is defined as $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2 = 100$ mJ.

Figure 11. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

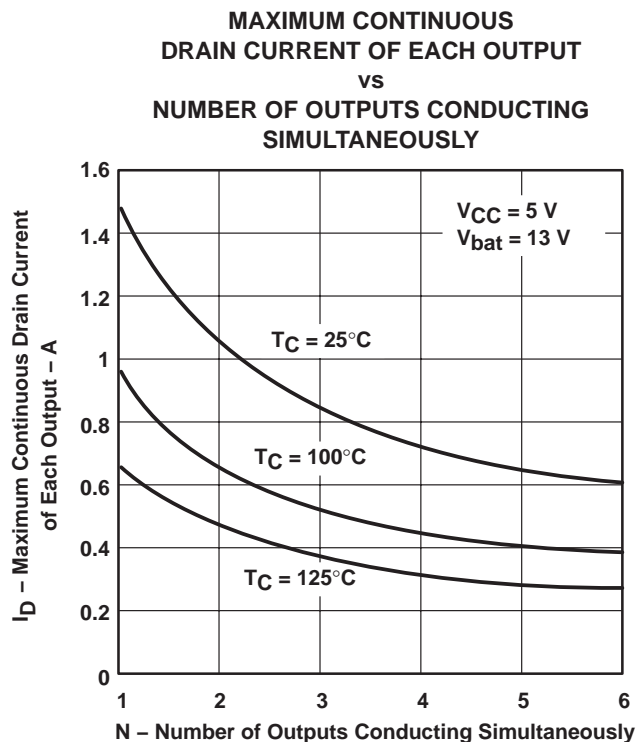


Figure 12

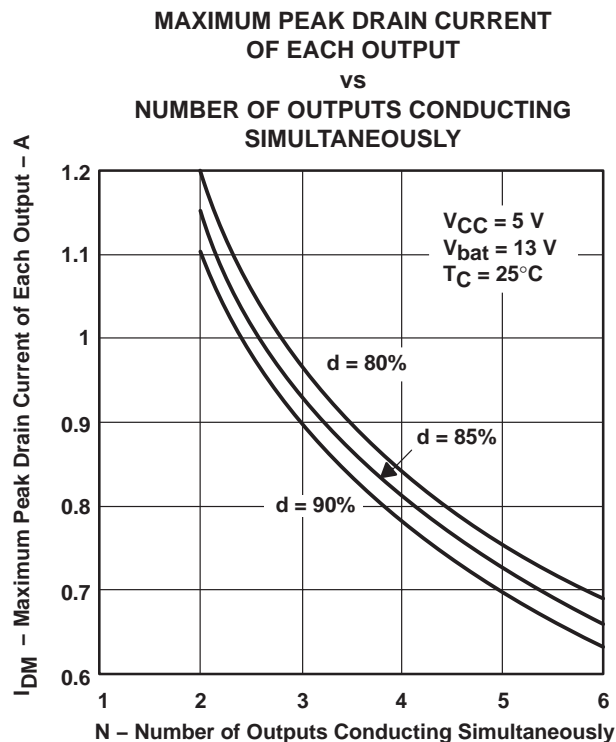
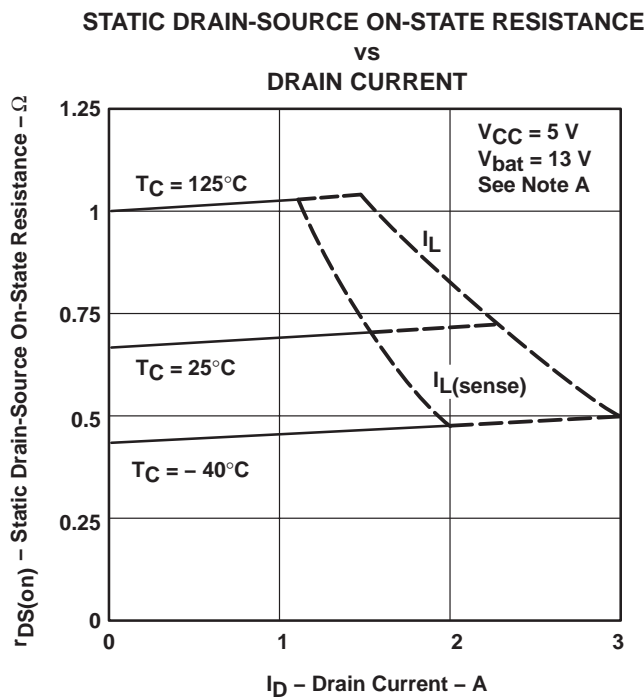
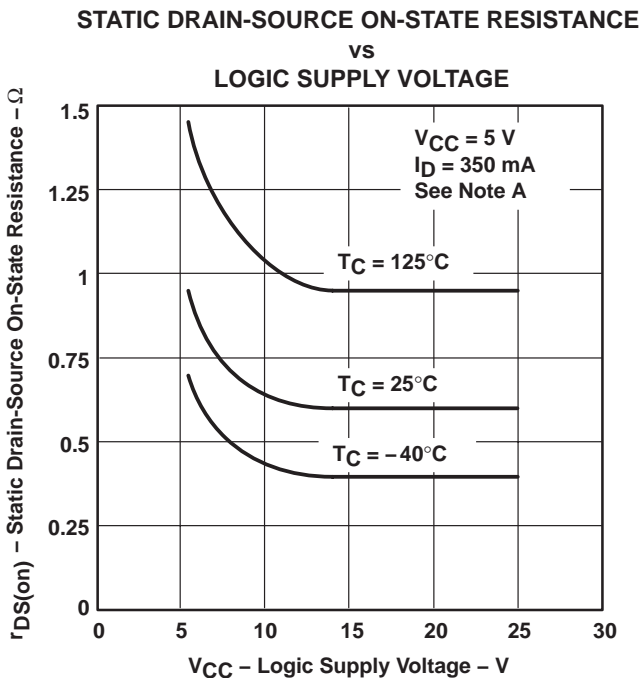


Figure 13



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 14



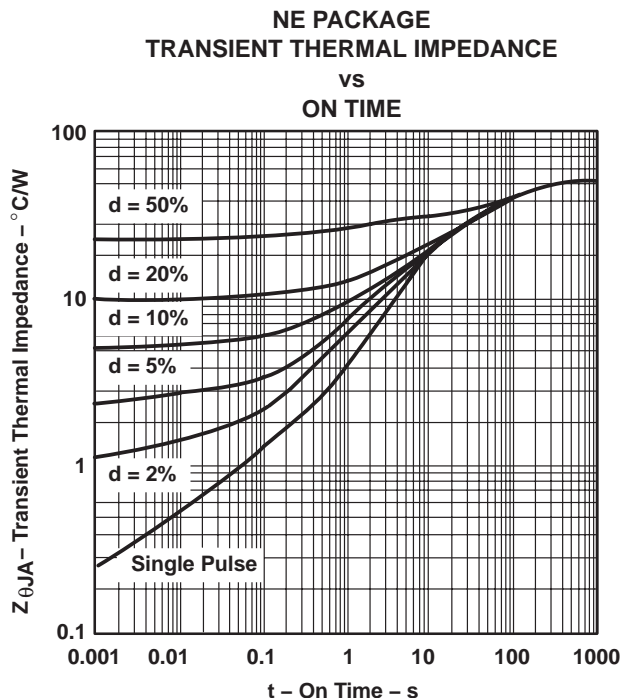
NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 15

TPIC2603 6-CHANNEL SERIAL INTERFACE LOW-SIDE DRIVER

SLIS056A – FEBRUARY 1995 – REVISED MARCH 1996

THERMAL INFORMATION



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta}(t_w + t_c) + Z_{\theta}(t_w) - Z_{\theta}(t_c)$$

Where:

$Z_{\theta}(t_w)$ = the single-pulse thermal impedance for $t = t_w$ seconds

$Z_{\theta}(t_c)$ = the single-pulse thermal impedance for $t = t_c$ seconds

$Z_{\theta}(t_w + t_c)$ = the single-pulse thermal impedance for $t = t_w + t_c$ seconds

$$d = t_w/t_c$$

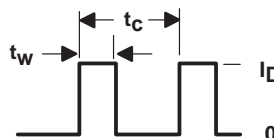


Figure 16

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPIC2603DW | ACTIVE | SOIC | DW | 24 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TPIC2603 | Samples |
| TPIC2603DWG4 | ACTIVE | SOIC | DW | 24 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TPIC2603 | Samples |
| TPIC2603DWR | ACTIVE | SOIC | DW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TPIC2603 | Samples |
| TPIC2603DWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TPIC2603 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

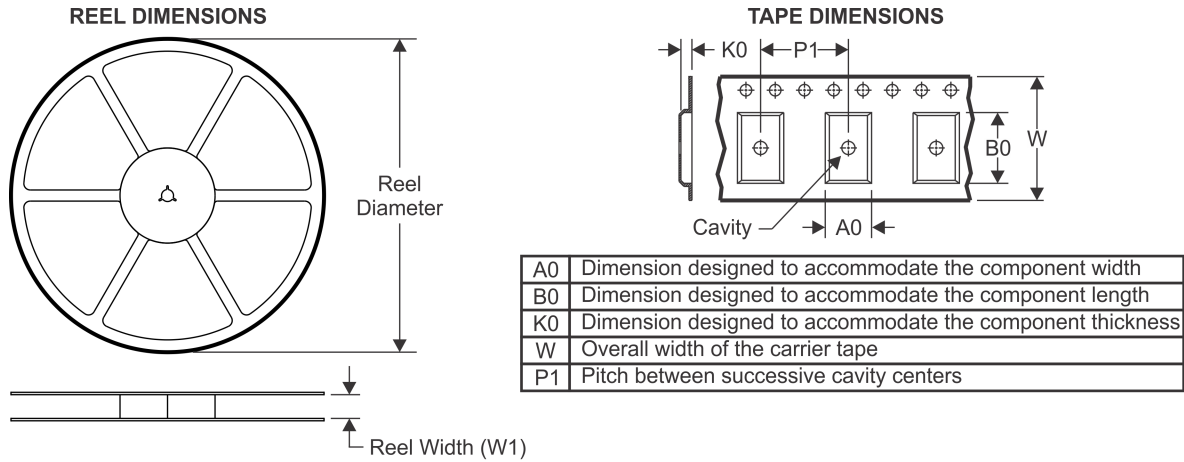
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPIC2603DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| TPIC2603DWRG4 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPIC2603DWR | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| TPIC2603DWRG4 | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated