PRODUCT CHANGE NOTIFICATION

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February 9, 2017 PCN#020917

Dear Sir/Madam:

Subject: Notification of Change to LTC3886 Die and Datasheet

Please be advised that Linear Technology Corporation has made enhancements to the LTC3886 product die to improve performance in the following areas:

1) Fix errata
2) Reduce power up times
3) Reduce the ADC update period
4) Improve on-chip EEPROM robustness

The documented errata in the LTC3886 are eliminated. Refer to the following link for the current errata documents http://cds.linear.com/docs/en/spec-notice/er3886f.pdf.

T_{INIT}, the time required from application of VIN until the part is ready to start sequencing output rails, is reduced from a typical value of 70ms to 35ms. This may allow applications to power up faster after application of VIN. This change is transparent in all applications that require sequencing of multiple power rails using multiple LTC Power System Management (PSM) parts connected in the recommended manner.

The ADC update period, $T_{CONVERT}$, is reduced from 100ms to 90ms, providing more timely telemetry of all monitored parameters.

The above changes are shown on the attached pages of the marked up datasheet.

Error Correcting Code (ECC) is added to the internal non-volatile memory to enhance its reliability. This change is transparent to the user and requires no modifications to programming files or system firmware. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced to 4 events. The read length of 147 bytes remains the same but the fifth and sixth events are a repeat of the fourth event if the part is reset. However, when reading the fault log from RAM, all 6 events of cyclical data are available.

The new silicon can be identified by the MFR_SPECIAL_ID, PMBus command code 0xE7, with a value of 0x460* where * is a value of 8-F.

No changes were made to the analog sections of the LTC3886, and no PWM characteristics changed. The die changes were qualified by performing characterization over the full operating junction temperature range and through rigorous engineering evaluation across a broad range of application conditions. The revised product will have successfully completed 1000 hours burn-in before production release.

Linear Technology will accept requests for revised samples within 30 days of the date of this notification. If we don't hear back from your company within this 30 day period, we will consider this change notice accepted by April 09, 2017. Production shipments of product incorporating the improved die will begin no sooner than April 09, 2017.

Should you have any further questions, please feel free to contact your local Linear Technology sales person or you may contact me at 408-432-1900 ext. 2077, or by E-mail JASON.HU@LINEAR.COM.

Sincerely,

Jason Hu

Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = 16V, $EXTV_{CC}$ = 0V, V_{RUN0} = 3.3V, V_{RUN1} = 3.3V f_{SYNC} = 350kHz (externally driven), and all programmable parameters at factory default unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage							
V_{IN}	Input Voltage Range	(Note 12)	●	4.5		60	V
I_Q	Input Voltage Supply Current Normal Operation	(Note 14) V_{RUN} = 3.3V, No Caps on TG and BG V_{RUN} = 0V			 26 22		 mA mA
V_{UVLO}	Undervoltage Lockout Threshold When V_{IN} > 4.2V	V_{INTVCC} Falling V_{INTVCC} Rising			3.7 3.95		V V
T_{INIT}	Initialization Time	Delay from RESTORE_USER_ALL, MFR_REST, or V_{INTVCC} > V_{UVLO} Until TON_DELAY Can Begin			~~70~~ 35		ms
Control Loop							
V_{OUTR0}	Range 0 Maximum V_{OUT} Range 0 Set Point Accuracy Range 0 Resolution Range 0 LSB Step Size, FSR = 16.38	 2.0V ≤ V_{OUT} ≤ 13.8V (Note 10)	 ● 	 –0.5 	14.0 12 4	 0.5 	V % Bits mV
V_{OUTR1}	Range 1 Maximum V_{OUT} Range 1 Set Point Accuracy Range 1 Resolution Range 1 LSB Step Size, FSR = 8.19V	 1.0V ≤ V_{OUT} ≤ 6.6V 	 ● 	 –0.5 	7.0 12 2	 0.5 	V % Bits mV
$V_{LINEREG}$	Line Regulation	16V < V_{IN} < 60V	●			±0.02	%/V
$V_{LOADREG}$	Load Regulation	ΔV_{ITH} = 1.35V – 0.7V ΔV_{ITH} = 1.35V – 2.0V	● ●		0.01 –0.01	0.1 –0.1	% %
$g_{m0,1}$	Resolution				3		bits
	Error Amplifier $g_{m(MAX)}$	I_{TH} =1.35V			5.76		mmho
	Error Amplifier $g_{m(MIN)}$	I_{TH} =1.35V			1.00		mmho
	Error Amplifier g_m LSB Step Size	I_{TH} =1.35V			0.68		mmho
$R_{ITHR0,1}$	Resolution				5		bits
	Compensation Resistor $R_{ITHR(MAX)}$				62		kΩ
	Compensation Resistor $R_{ITHR(MIN)}$				0		kΩ
I_{ISENSE}	Input Current	V_{ISENSE} = 14V	●		±1	±2	µA
$V_{I(ILIMIT)}$	Resolution				3		bits
	$V_{ILIM(MAX)}$	Hi Range Lo Range	● ●	68 44	75 50	82 56	mV mV
	$V_{ILIM(MIN)}$	Hi Range Lo Range			37.5 25		mV mV
Gate Driver							
TG t_r t_f	TG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
BG t_r t_f	BG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 20 20		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF			10		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF			30		ns
$t_{ON(MIN)}$	Minimum On-Time				90		ns

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OV/UV Output Voltage Supervisor							
N	Resolution				9		Bits
V_{RANGE0}	Range 0 Maximum Threshold				14		V
V_{RANGE1}	Range 1 Maximum Threshold				7		V
V_{OUSTP0}	Range 0 Step Size, FSR = 16.352V	(Note 10)			32		mV
V_{OUSTP1}	Range 1 Step Size, FSR = 8.176V				16		mV
V_{THACC0}	Range 0 Threshold Accuracy	2V < V_{OUT} < 14V	●			±2.5	%
V_{THACC1}	Range 1 Threshold Accuracy	1V < V_{OUT} < 7V	●			±2.5	%
$t_{PROPOV1}$	OV Comparator to FAULT Low Time	V_{OD} = 10% of Threshold				35	µs
$t_{PROPUV1}$	UV Comparator to FAULT Low Time	V_{OD} = 10% of Threshold				100	µs
V_{IN} Voltage Supervisor							
N	Resolution				9		Bits
$V_{IN(RANGE)}$	Full-Scale Voltage	(Note 11)		4.5		61.32	V
$V_{IN(STP)}$	Step Size				120		mV
$V_{IN(THACCH)}$	Threshold Accuracy 12V < V_{IN} < 60V		●			±3	%
$V_{IN(THACCL)}$	Threshold Accuracy 4.5V < V_{IN} < 15V		●			±6	%
$t_{PROP(VIN)}$	Comparator Response Time (VIN_ON and VIN_OFF)	V_{OD} = 10% of Threshold				100	µs
Output Voltage Readback							
N	Resolution LSB Step Size				16 250		Bits µV
$V_{F/S}$	Full-Scale Sense Voltage	(Note 10) V_{RUN} = 0V (Note 8)			16.384		V
V_{OUT_TUE}	Total Unadjusted Error	T_J = 25°C, V_{OUT} > 1.0V (Note 8)	 ●		0.2	 ±0.5	% %
V_{OS}	Zero-Code Offset Voltage		●			±500	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			~~100~~ 90		ms
V_{IN} Voltage Readback							
N	Resolution	(Note 5)			10		Bits
$V_{F/S}$	Full-Scale Input Voltage	(Note 11)			66.56		V
V_{IN_TUE}	Total Unadjusted Error	T_J = 25°C, V_{VIN} > 4.5V	 ●			0.4 2	% %
$t_{CONVERT}$	Conversion Time	(Note 6)			~~100~~ 90		ms
Output Current Readback							
N	Resolution LSB Step Size	(Note 5) 0V ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 16mV 16mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 32mV 32mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 64mV 64mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 100mV			10 15.26 30.52 61 122		Bits µV µV µV µV
$I_{F/S}$	Full-Scale Output Current	(Note 7) R_{ISENSE} = 1mΩ			±100		A
I_{OUT_TUE}	Total Unadjusted Error	(Note 8) 10mV ≤ V_{ISENSE} ≤ 100mV	●			±1.5	%
V_{OS}	Zero-Code Offset Voltage					±32	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			~~100~~ 90		ms

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current Readback							
N	Resolution LSB Step Size, Full-Scale Range = 16mV LSB Step Size, Full-Scale Range = 32mV LSB Step Size, Full-Scale Range = 64mV	(Note 5) 8x Gain, 0V ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 5mV 4x Gain, 0V ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 20mV 2x Gain, 0V ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 50mV			10 15.26 30.52 61		Bits µV µV µV
I_{IN_TUE}	Total Unadjusted Error (Note 8)	8x Gain, 2.5mV ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 5mV 4x Gain, 4mV ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 20mV 2x Gain, 6mV ≤ $\|I_{IN}^+ - I_{IN}^-\|$ ≤ 50mV	● ● ●			±1.6 ±1.3 ±1.2	% % %
V_{OS}	Zero-Code Offset Voltage					±50	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			~~100~~ 90		ms
Supply Current Readback							
N	Resolution LSB Step Size, Full-Scale Range = 256mV	(Note 5)			10 244		Bits µV
I_{CHIP_TUE}	Total Unadjusted Error	20mV ≤ $\|I_{IN}^+ - V_{IN}\|$ ≤ 200mV	●			±2.5	%
$t_{CONVERT}$	Conversion Time	(Note 6)			~~100~~ 90		ms
Temperature Readback (T0, T1)							
T_{RES_T}	Resolution				0.25		°C
T0_TUE	External TSNS TUE (Note 8) MFR_PWM_MODE_LTC3886[5] = 0 MFR_PWM_MODE_LTC3886[5] = 1	 ΔV_{TSNS} = 72mV (Note 17) V_{TSNS} ≤ 1.85mV (Note 17)	 ● ●			 ±3 ±7	 °C °C
TI_TUE	Internal TSNS TUE	V_{RUN} = 0.0V (Note 8)			±1		°C
$t_{CONVERT\_T}$	Update Rate	(Note 6)			~~100~~ 90		ms
$INTV_{CC}$ Regulator							
V_{INTVCC_VIN}	Internal V_{CC} Voltage No Load	6V < V_{IN} < 60V	●	4.8	5	5.2	V
V_{LDO_VIN}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	±2	%
V_{INTVCC_EXT}	Internal V_{CC} Voltage No Load	5.5V < $EXTV_{CC}$ < 14V	●	4.8	5	5.2	V
V_{LDO_EXT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, $EXTV_{CC}$ = 12V			0.5	±2	%
V_{EXT_THRES}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive	●	4.5	4.7	4.95	V
V_{EXT_HYS}	$EXTV_{CC}$ Hysteresis Voltage				80		mV
V_{DD33} Regulator							
V_{DD33}	Internal V_{DD33} Voltage	4.5V < V_{INTVCC}		3.2	3.3	3.4	V
I_{LIM}	V_{DD33} Current Limit	V_{DD33} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			100		mA
V_{DD33_OV}	V_{DD33} Overvoltage Threshold				3.5		V
V_{DD33_UV}	V_{DD33} Undervoltage Threshold				3.1		V
V_{DD25} Regulator							
V_{DD25}	Internal V_{DD25} Voltage				2.5		V
I_{LIM}	V_{DD25} Current Limit	V_{DD25} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			80		mA
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency Accuracy	100kHz < f_{SYNC} < 750kHz Measured Falling Edge-to-Falling Edge of SYNC with SWITCH_FREQUENCY = 100.0 and 750.0	●			±10	%
$V_{TH(SYNC)}$	SYNC Input Threshold	V_{CLKIN} Falling V_{CLKIN} Rising			1 1.5		V V
$V_{OL(SYNC)}$	SYNC Low Output Voltage	I_{LOAD} = 3mA	●		0.2	0.4	V
$I_{LEAK(SYNC}$	SYNC Leakage Current in Slave Mode	0V ≤ V_{PIN} ≤ 3.6V				±5	µA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
θSYNC-θ0	SYNC to Channel 0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG0	MFR_PWM_CONFIG_LTC3886[2:0] = 0,2,3 MFR_PWM_CONFIG_LTC3886[2:0] = 5 MFR_PWM_CONFIG_LTC3886[2:0] = 1 MFR_PWM_CONFIG_LTC3886[2:0] = 4,6			0 60 90 120		Deg Deg Deg Deg
θSYNC-θ1	SYNC to Channel 1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1	MFR_PWM_CONFIG_LTC3886[2:0] = 3 MFR_PWM_CONFIG_LTC3886[2:0] = 0 MFR_PWM_CONFIG_LTC3886[2:0] = 2,4,5 MFR_PWM_CONFIG_LTC3886[2:0] = 1 MFR_PWM_CONFIG_LTC3886[2:0] = 6			120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Note 13)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 13)	T_J < 125°C	●	10			Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, 0°C < T_J ≤ 85°C During EEPROM Write Operations	●		440	4100	ms
Digital Inputs SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*							
V_{IH}	Input High Threshold Voltage	SCL, SDA, RUN, $\overline{\text{FAULT}}$	●			2.0	V
V_{IL}	Input Low Threshold Voltage	SCL, SDA, RUN, $\overline{\text{FAULT}}$	●	1.4			V
V_{HYST}	Input Hysteresis	SCL, SDA			0.08		V
C_{PIN}	Input Capacitance					10	pF
Digital Input WP							
I_{PUWP}	Input Pull-Up Current	WP			10		µA
Open-Drain Outputs SCL, SDA, $\overline{\text{FAULT}}$*n*, $\overline{\text{ALERT}}$, RUN*n*, SHARE_CLK, PGOOD*n*							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
Digital Inputs SHARE_CLK, WP							
V_{IH}	Input High Threshold Voltage		●		1.5	1.8	V
V_{IL}	Input Low Threshold Voltage		●	0.6	1.0		V
Leakage Current SDA, SCL, $\overline{\text{ALERT}}$, RUN							
I_{OL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V	●			±5	µA
Leakage Current $\overline{\text{FAULT}}$*n*, PGOOD*n*							
I_{GL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			±2	µA
Digital Filtering of $\overline{\text{FAULT}}$*n*							
t_{FAULT}	Input Digital Filtering $\overline{\text{FAULT}}$*n*				3		µs
Digital Filtering of PGOOD*n*							
t_{PGOOD}	Output Digital Filtering PG00D*n*				60		µs
Digital Filtering of RUN*n*							
t_{RUN}	Input Digital Filtering RUN*n*				10		µs
PMBus Interface Timing Characteristics							
f_{SCL}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD(STA)}$	Hold Time After Start Condition. After This Period, the First Clock Is Generated		●	0.6			µs
$t_{SU(STA)}$	Repeated Start Condition Setup Time		●	0.6		10000	µs
$t_{SU(STO)}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 µs µs