Mask Change for all Spartan-6 FPGA Devices, Speed File Change for -3N Devices

XCN11012 (v1.0) April 18, 2011

Product Change Notice – For Information Only

Overview

The purpose of this notification is to communicate a mask change for all production Spartan®-6 FPGA devices and a speed file change for all Spartan-6 –3N speed devices.

Description

This description includes the following changes to be implemented:

Mask change

Production Spartan-6 FPGA devices will begin transitioning to a new mask revision. The new mask revision changes the IODELAY2 errata noted in EN148. The mask changes are limited to the IODELAY2 circuit within each I/O. This is considered a minor change and is drop-in compatible. There is no change to functionality relative to the software and documentation, other than the change to the IODELAY2 errata in EN148. The new silicon is bitstream compatible to the current silicon. The new mask revision is indicated by a change in the topmark circuit revision code and by a change in the JTAG IDCODE revision.

New speed file

A new speed file has been generated to make some small incremental delay changes in the IODELAY2 for -3N speed grades. Designs using IDELAY or ODELAY in fixed mode should be re-timed, otherwise no action is required. All other parameters remain unchanged. The new speed file is backward compatible and optional to the previous mask revision and therefore can be used for all Spartan-6 FPGA devices. The new speed file is available with ISE® Design Suite - 13.1 Product Update - April, 2011.

Products Affected

The mask change affects all production speed, package, and temperature variations of the XC commercial (C) and industrial (I) grade devices. The speed file change affects the -3N speed grades where offered. Affected part numbers are included in Table 1:

Table 1: **Product Changes for Affected Products[1]**

Xilinx Product	Circuit Revision Code		JTAG IDCODE Revision		Speed File Change[2]
	Previous	New	Previous	New	
XC6SLX4	A	B	0	2	N/A
XC6SLX9	A	B	0	2	-3N[3]
XC6SLX16	C	D	2/3	4	-3N
XC6SLX25	A	B	0	2	-3N
XC6SLX25T	A	B	0	2	-3N
XC6SLX45	C	D	2/3	4	-3N
XC6SLX45T	C	D	3	4	-3N
XC6SLX75	A	B	0	2	-3N
XC6SLX75T	A	B	0	2	-3N
XC6SLX100	A	B	0	2	--3N
XC6SLX100T	A	B	0	2	-3N
XC6SLX150	B	C	3	4	-3N
XC6SLX150T	B	C	3	4	-3N

[1] XA Automotive, XQ, Q grade, and XC Lower Power -1L devices are not affected by this Product Change Notice and will be released with the new mask revision.
[2] Xilinx recommends using a minimum of ISE 13.1 Product Update – April, 2011 for -3N.
[3] The ordering code for -3N speed devices is –N3, e.g. XC6SLX45-N3FGG484C.

Cross Shipping Information

Once Xilinx begins shipping new circuit revision code devices, customers may receive devices of either circuit revision code until inventory of previous circuit revision code devices is depleted.

Traceability

Affected devices are identified by the design circuit revision code as shown in the following package topmark.

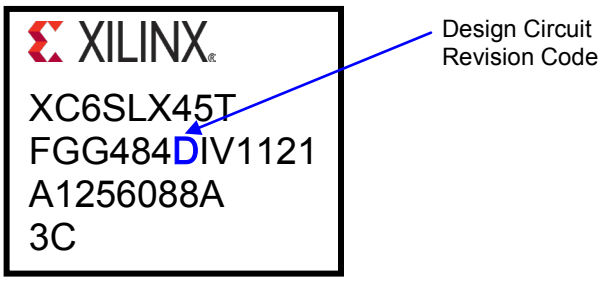

Figure 1: **Package Topmark**

Recommendations

Customers with –3N speed grade designs using IDELAY or ODELAY in fixed mode should re-time their design with ISE Design Suite – 13.1 Product Update – April, 2011.

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support.

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Additional Documentation

Spartan-6 FPGA Documentation:

http://www.xilinx.com/support/documentation/spartan-6.htm

Xilinx Answer Record Database:

http://www.xilinx.com/support/answers

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/18/11	1.0	Initial release.

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