High Current IGBT Gate Drivers

NCV5705B, NCD5705B

The NCV/NCD5705B is a high−current, high−performance stand−alone IGBT driver for high power automotive applications that include PTC heaters, traction inverters, high voltage DC−DC and other auxiliary subsystems. The device offers a cost−effective solution by eliminating external output buffer. Device's protection features include accurate Under−voltage−lockout (UVLO), desaturation protection (DESAT) and Active open−drain FAULT output. The driver also features an accurate 5.0 V output. The driver is designed to accommodate a wide voltage range of bias supplies including unipolar and even bipolar voltages. NCV5705B is available in 8−pin SOIC package.

Features

- High Current Output (+4/−6 A) at IGBT Miller Plateau Voltages
- Low Output Impedance for Enhanced IGBT Driving
- Short Propagation Delay with Accurate Matching
- Direct Interface to Digital Isolator/Opto−coupler/Pulse Transformer for Isolated Drive, Logic Compatibility for Non−isolated Drive
- DESAT Protection with Programmable Delay
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range
- This Device is Pb−Free, Halogen−Free and RoHS Compliant
- Negative Output Voltage for Enhanced IGBT Driving

Typical Applications

- PTC Heaters
- Traction Inverters
- HV DC−DC
- OBC

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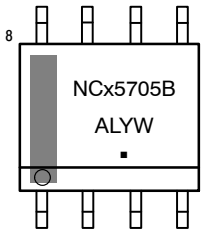
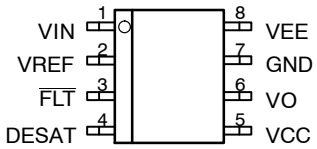
SOIC−8 NB
CASE 751−07

MARKING DIAGRAM



NCx5705B	= Specific Device Code x = D or V
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



NCV5705B, NCD5705B

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

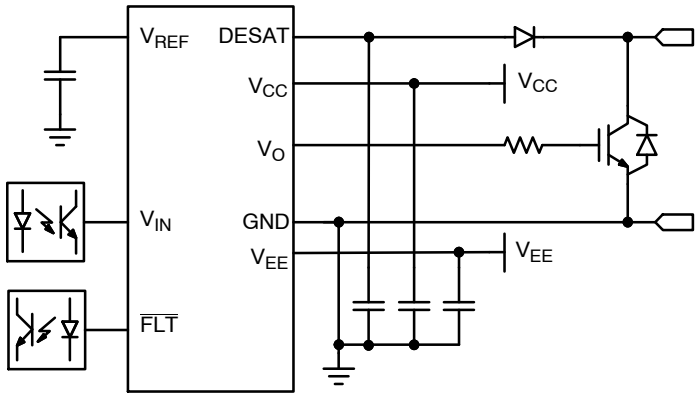


Figure 1. Simplified Application Schematics

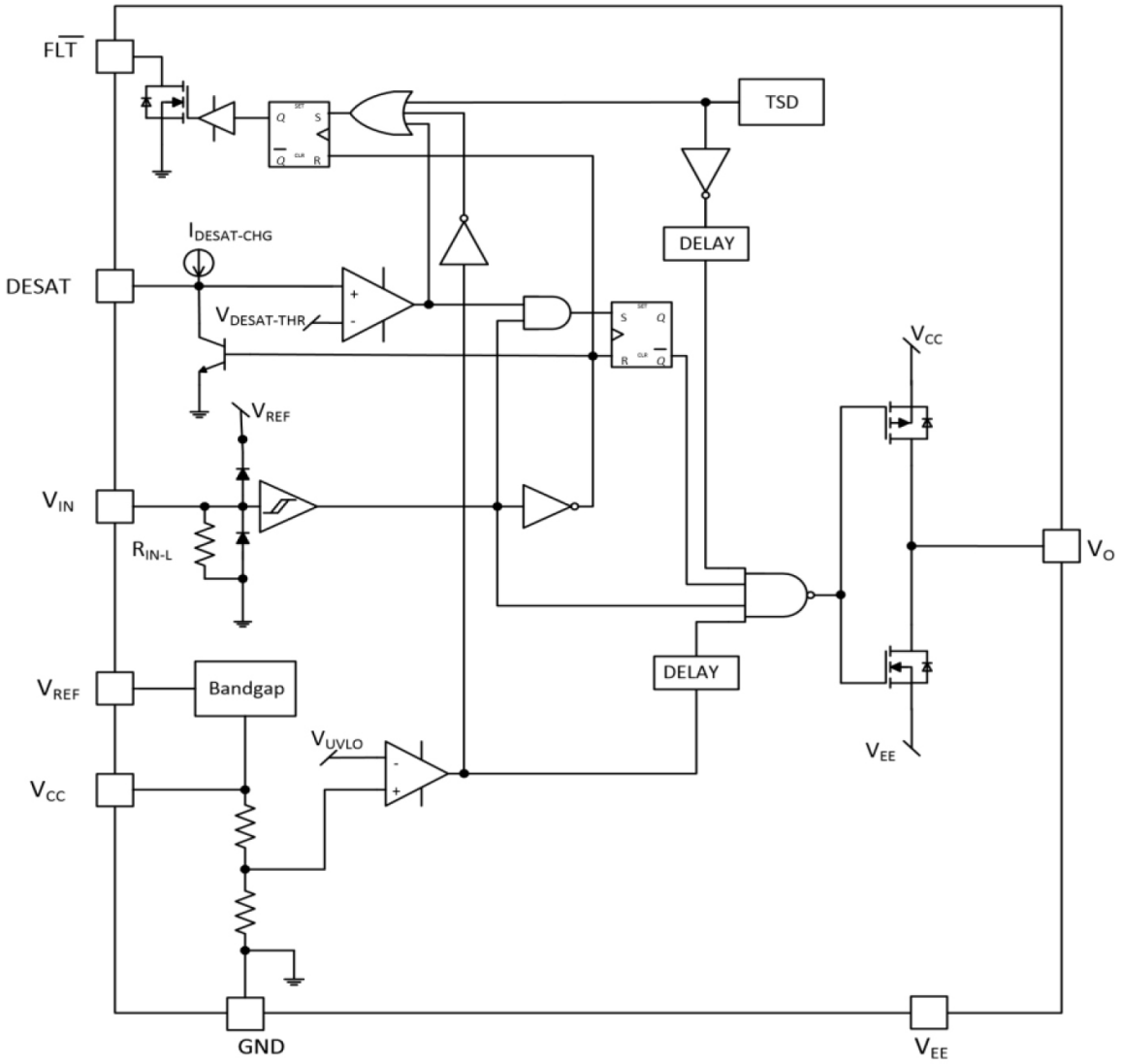


Figure 2. Detailed Block Diagram NCV5705B

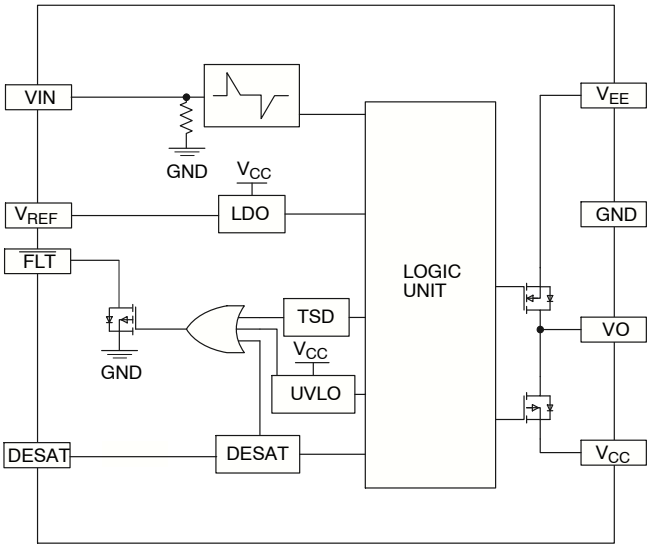


Figure 3. Simplified Block Diagram NCV5705B

Table 1. PIN FUNCTION DESCRIPTION

Pin Name	No.	I/O/x	Description
VIN	1	I	Input signal to control the output. In applications which require galvanic isolation, VIN is generated at the opto output, the pulse transformer secondary or the digital isolator output. VO (VOH/ VOL) signal is in phase with VIN. VIN is internally clamped to GND and has a pull− down resistor of 1 M to ensure that an output is low in the absence of an input signal. A minimum pulse−width is required at VIN before VO (VOH/VOL) is activated.
VREF	2	O	5 V Reference generated within the driver is brought out to this pin for external bypassing and for powering low bias circuits (such as digital isolators).
$\overline{\text{FLT}}$	3	O	Fault open drain output (active low) that allows communication to the main controller that the driver has encountered a fault condition and has deactivated the output. Open drain allows easy setting of (inactive) high level and parallel connection of multiple fault signals. Connect to 10k pull−up resistor recommended. Truth Table is provided in the datasheet to indicate conditions under which this signal is asserted. Capable of driving optos or digital isolators when isolation is required.
DESAT	4	I	Input for detecting the desaturation of IGBT due to a fault condition. A capacitor connected to this pin allows a programmable blanking delay every ON cycle before DESAT fault is processed, thus preventing false triggering.
VCC	5	x	Positive bias supply for the driver. The operating range for this pin is from UVLO to the maximum. A good quality bypassing capacitor is required from this pin to GND and should be placed close to the pins for best results.
VO	6	O	Driver output that provides the appropriate drive voltage, source and sink current to the IGBT gate. VO is actively pulled low during start−up and under Fault conditions.
GND	7	x	This pin should connect to the IGBT Emitter with a short trace. All power pin bypass capacitors should be referenced to this pin and kept at a short distance from the pin.
VEE	8	x	A negative voltage with respect to GND can be applied to this pin and that will allow VO to go to a negative voltage during OFF state. A good quality bypassing capacitor is needed from VEE to GND. If a negative voltage is not applied or available, this pin must be connected to GND.

Table 2. ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Minimum	Maximum	Unit
Differential Power Supply	V_{CC} – V_{EE} (V_{max})	0	36	V
Positive Power Supply	V_{CC} – GND	−0.3	22	V
Negative Power Supply	V_{EE} – GND	−18	0.3	V
Gate Output High	(V_O,V_{OH}) – GND		V_{CC} + 0.3	V
Gate Output Low	(V_O,V_{OL}) – GND	V_{EE} − 0.3		V
Input Voltage	V_{IN} – GND	−0.3	5.5	V
DESAT Voltage	V_{DESAT} – GND	−0.3	V_{CC} + 0.3	V
$\overline{FLT}$ Current Sink	I – SINK		20	mA
Power Dissipation SO−8 package	PD		700	mW
Maximum Junction Temperature	TJ(max)		150	°C
Storage Temperature Range	TSTG		−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESDHBM		4	kV
ESD Capability, Machine Model (Note 2)	ESDMM		200	V
Moisture Sensitivity Level	MSL		1	–
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	TSLD		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115).
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78, 25°C.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 3. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 (Note 4) Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	176	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 100 mm^2 (or 0.16 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Note 6)

Parameter	Symbol	Min	Max	Unit
Differential Power Supply	V_{CC} – V_{EE} (V_{max})		30	V
Positive Power Supply	V_{CC}	UVLO	20	V
Negative Power Supply	V_{EE}	−15	0	V
Input Voltage	V_{IN}	0	5	V
Input pulse width	t_{on}	40		ns
Ambient Temperature	T_A	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, V_{EE} = 0 V, Kelvin GND connected to V_{EE}. For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LOGIC INPUT AND OUTPUT						
Input Threshold Voltages High−state (Logic 1) Required Low−state (Logic 0) Required No state change	Pulse−Width = 150 ns, V_{EN} = 5 V Voltage applied to get output to go low Voltage applied to get output to go high Voltage applied without change in output state	 V_{IN-H1} V_{IN-L1} V_{IN-NC}	 4.3 1.2		 0.75 3.7	V
Input Current High−state Low−state	 V_{IN-H} = 4.5 V V_{IN-L} = 0.5 V	 I_{IN-H} I_{IN-L}			 10 1	A
Input Pulse−Width No Response at the Output Guaranteed Response at the Output	Voltage thresholds consistent with input specs	 $t_{on-min1}$ $t_{on-min2}$	 30		10	ns
Threshold Voltage Low State High State	 (I_{SINK} = 15 mA) External pull−up	 V_{FLT-L} V_{FLT-H}		0.5	1.0 V_{CC} + 0.3	V
DRIVE OUTPUT						
Output Low State	I_{sink} = 200 mA, T_A = 25°C I_{sink} = 200 mA, T_A = −40°C to 125°C I_{sink} = 1.0 A, T_A = 25°C	V_{OL1} V_{OL2} V_{OL3}		0.1 0.2 0.8	0.2 0.5 1.2	V
Output High State	I_{src} = 200 mA, T_A = 25°C I_{src} = 200 mA, T_A = −40°C to 125°C I_{src} = 1.0 A, T_A = 25°C	V_{OH1} V_{OH2} V_{OH3}	14.5 14.2 13.8	14.8 14.7 14.1		V
Peak Driver Current, Sink (Note 7)	R_G = 0.1 , V_{CC} = 15 V, V_{EE} = −8 V V_O = 13 V V_O = 9 V (near Miller Plateau)	 $I_{PK-snk1}$ $I_{PK-snk2}$		 6.8 6.1		A
Peak Driver Current, Source (Note 7)	R_G = 0.1 , V_{CC} = 15 V, V_{EE} = −8 V V_O = −5 V V_O = 9 V (near Miller Plateau)	 $I_{PK-src1}$ $I_{PK-src2}$		 7.8 4.0		A
DYNAMIC CHARACTERISTICS						
Turn−on Delay (see timing diagram)	Negative input pulse width = 10 s	t_{pd-on}	45	59	75	ns
Turn−off Delay (see timing diagram)	Positive input pulse width = 10 s	t_{pd-off}	45	54	75	ns
Propagation Delay Distortion (=t_{pd-on} − t_{pd-off})	For input or output pulse width > 150 ns, T_A = 25°C T_A = −40°C to 125°C	 $t_{distort1}$ $t_{distort2}$	 −5 −25	 5	 15 25	ns
Prop Delay Distortion between Parts (Note 7)		$t_{distort\ -tot}$	−30	0	30	ns
Rise Time (Note 7) (see timing diagram)	C_{load} = 1.0 nF	t_{rise}		9.2		ns
Fall Time (Note 7) (see timing diagram)	C_{load} = 1.0 nF	t_{fall}		7.9		ns
Delay from FLT under UVLO/TSD to VO/VOL		t_{d1-OUT}	10	12	15	μs
Delay from DESAT to VO/VOL (Note 7)		t_{d2-OUT}		220		ns
Delay from UVLO/TSD to FLT (Note 7)		t_{d3-FLT}		7.3		μs

Table 5. ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, V_{EE} = 0 V, Kelvin GND connected to V_{EE}. For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DESAT PROTECTION						
DESAT Threshold Voltage		$V_{DESAT-THR}$	6.0	6.35	7.0	V
Blanking Charge Current		$I_{DESAT-CHG}$	0.20	0.24	0.28	mA
Blanking Discharge Current		$I_{DESAT-DIS}$		30		mA
UVLO						
UVLO Startup Voltage		$V_{UVLO-OUT-ON}$	7.5	8.0	8.5	V
UVLO Disable Voltage		$V_{UVLO-OUT-OFF}$	6.5	7.0	7.5	V
UVLO Hysteresis		$V_{UVLO-HYST}$	0.45	1.0	1.2	V
VREF						
Voltage Reference	I_{REF} = 10 mA	V_{REF}	4.85	5.00	5.15	V
Reference Output Current (Note 7)		I_{REF}			20	mA
Recommended Capacitance		C_{VREF}	100			nF
SUPPLY CURRENT						
Current Drawn from V_{CC}	V_{CC} = 15 V Standby (No load on output, FLT, VREF)	I_{CC-SB}		0.9	1.5	mA
Current Drawn from V_{EE} (NCV5705B ONLY)	V_{EE} = −10 V Standby (No load on output, FLT, VREF)	I_{EE-SB}	−0.2	−0.14		mA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 7)		T_{SD}		188		°C
Thermal Shutdown Hysteresis (Note 7)		T_{SH}		33		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Values based on design and/or characterization.

ORDERING INFORMATION

Device	Package	Shipping†
NCD5705BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV5705BDR2G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

APPLICATIONS AND OPERATING INFORMATION

This section lists the details about key features and operating guidelines for the NCV5705B.

High Drive Current Capability

The NCV5705B driver is equipped with many features which facilitate a superior performance IGBT driving circuit. Foremost amongst these features is the high drive current capability. The drive current of an IGBT driver is a function of the differential voltage on the output pin (VCC−VOH/VO for source current, VOL/VO−VEE for sink current) as shown in Figure 4. Figure 4 also indicates that for a given VOH/VOL value, the drive current can be increased by using higher VCC/VEE power supply). The drive current tends to drop off as the output voltage goes up (for turn−on event) or goes down (for turn−off event). As explained in many IGBT application notes, the most critical phase of IGBT switching event is the Miller plateau region where the gate voltage remains constant at a voltage (typically in 9−11 V range depending on IGBT design and the collector current), but the gate drive current is used to charge/discharge the Miller capacitance (C_{GC}). By providing a high drive current in this region, a gate driver can significantly reduce the duration of the phase and help reducing the switching losses. The NCV5705B addresses this requirement by providing and specifying a high drive current in the Miller plateau region. Most other gate driver ICs merely specify peak current at the start of switching – which may be a high number, but not very relevant to the application requirement. It must be remembered that other considerations such as EMI, diode reverse recovery performance, etc., may lead to a system level decision to trade off the faster switching speed against low EMI and reverse recovery. However, the use of NCV5705B does not preclude this trade−off as the user can always tune the drive current by employing external series gate resistor. Important thing to remember is that by providing a high internal drive current capability, the NCV5705B facilitates a wide range of gate resistors. Another value of the high current at the Miller plateau is that the initial switching transition phase is shorter and more controlled. Finally, the high gate driver current (which is facilitated by low impedance internal FETs), ensures that even at high switching frequencies, the power dissipation from the drive circuit is primarily in the external series resistor and more easily manageable. Experimental results have shown that the high current drive results in reduced turn−on energy (E_{ON}) for the IGBT switching.

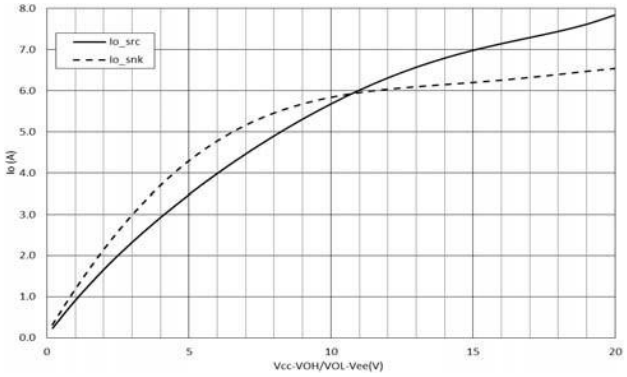


Figure 4. Output Current vs. Output Voltage Drop

When driving larger IGBTs for higher current applications, the drive current requirement is higher, hence lower R_G is used. Larger IGBTs typically have high input capacitance. On the other hand, if the NCV5705B is used to drive smaller IGBT (lower input capacitance), the drive current requirement is lower and a higher R_G is used. Thus, for most typical applications, the driver load RC time constant remains fairly constant. Caution must be exercised when using the NCV5705B with a very low load RC time constant. Such a load may trigger internal protection circuitry within the driver and disable the device. Figure 4 shows the recommended minimum gate resistance as a function of IGBT gate capacitance and gate drive trace inductance.

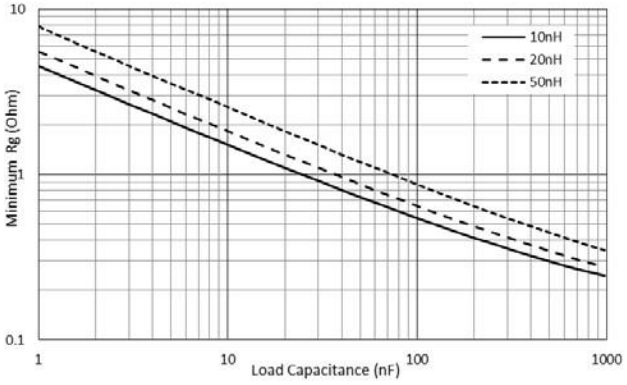


Figure 5. Recommended Minimum Gate Resistance as a Function of IGBT Gate Capacitance

Gate Voltage Range

The negative drive voltage for gate (with respect to GND, or Emitter of the IGBT) is a robust way to ensure that the gate voltage does not rise above the threshold voltage due to the Miller effect. In systems where the negative power supply is available, the VEE option offered by NCV5705B allows not only a robust operation, but also a higher drive current for turn−off transition. Adequate bypassing between VEE pin and GND pin is essential if this option is used.

The V_{CC} range for the NCV5705B is quite wide and allows the user the flexibility to optimize the performance or use available power supplies for convenience.

Under Voltage Lock Out (UVLO)

This feature ensures reliable switching of the IGBT connected to the driver output. At the start of the driver's operation when V_{CC} is applied to the driver, the output remains turned−off. This is regardless of the signals on V_{IN} until the V_{CC} reaches the UVLO Output Enabled ($V_{UVLO-OUT-ON}$) level. After the V_{CC} rises above the $V_{UVLO-OUT-ON}$ level, the driver is in normal operation. The state of the output is controlled by signal at V_{IN}.

If the V_{CC} falls below the UVLO Output Disabled

($V_{UVLO-OUT-OFF}$) level during the normal operation of the driver, the Fault output is activated and the output is shut−down (after a delay) and remains in this state. The driver output does not start to react to the input signal on VIN until the VCC rises above the $V_{UVLO-OUT-ON}$ again. The waveform showing the UVLO behavior of the driver is in Figure 6.

A UVLO event (V_{CC} voltage going below $V_{UVLO-OUT-OFF}$) also triggers activation of FLT output after a delay of td3−FLT. This indicates to the controller that the driver has encountered an issue and corrective action needs to be taken. However, a nominal delay td1−OUT = 12 μs is introduced between the initiation of the FLT output and actual turning off of the output. This delay provides adequate time for the controller to initiate a more orderly/sequenced shutdown. In case the controller fails to do so, the driver output shutdown ensures IGBT protection after t_{d1-OUT}.

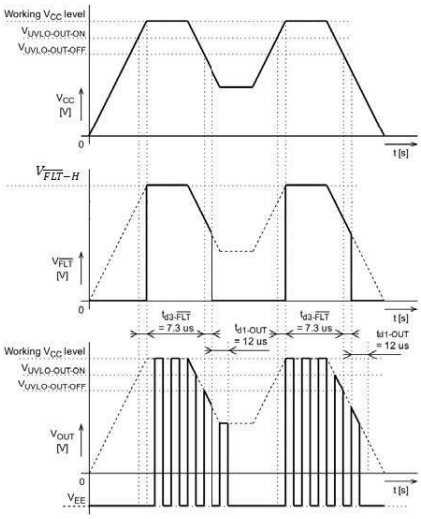


Figure 6. UVLO Function and Limits

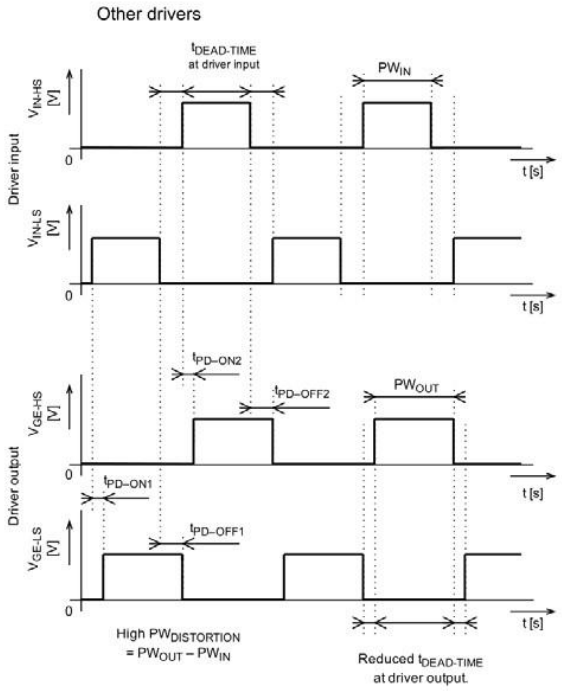


Figure 7. Timing Waveforms (Other Drivers)

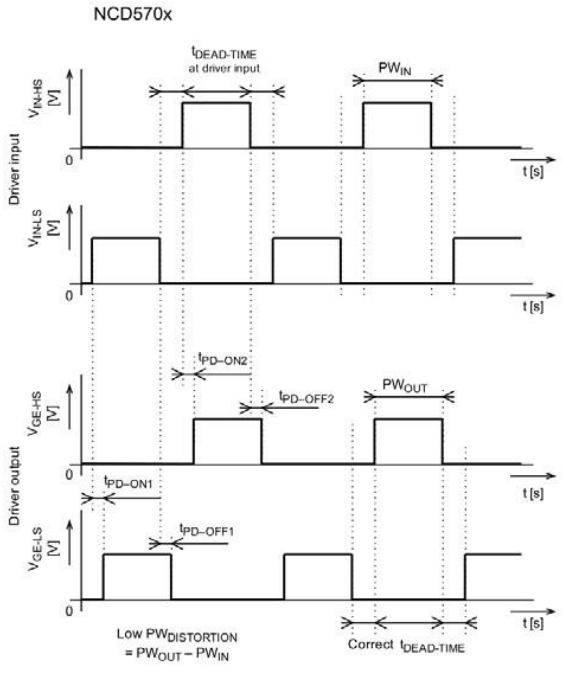


Figure 8. NCV5705B Timing Waveforms

Timing Delays and Impact on System Performance

The gate driver is ideally required to transmit the input signal pulse to its output without any delay or distortion. In the context of a high−power system where IGBTs are typically used, relatively low switching frequency (in tens of kHz) means that the delay through the driver itself may not be as significant, but the matching of the delay between different drivers in the same system as well as between different edges has significant importance. With reference to Figure 7, two input waveforms are shown. They are typical complementary inputs for high−side (HS) and low−side (LS) of a half−bridge switching configuration. The dead−time between the two inputs ensures safe transition between the two switches. However, once these inputs are through the driver, there is potential for the actual gate voltages for HS and LS to be quite different from the intended input waveforms as shown in Figure 8. The end result could be a loss of the intended dead−time and/or pulse−width distortion. The pulse−width distortion can create an imbalance that needs to be corrected, while the loss of dead−time can eventually lead to cross−conduction of the switches and additional power losses or damage to the system.

Desaturation Protection (DESAT)

This feature monitors the collector−emitter voltage of the IGBT in the turned−on state. When the IGBT is fully turned on, it operates in a saturation region. Its collector−emitter voltage (called saturation voltage) is usually low, well below 3 V for most modern IGBTs. It could indicate an overcurrent or similar stress event on the IGBT if the collector−emitter voltage rises above the saturation voltage, after the IGBT is fully turned on. Therefore the DESAT protection circuit compares the collector−emitter voltage with a voltage level $V_{DESAT-THR}$ to check if the IGBT didn't leave the saturation region. It will activate FLT output and shut down driver output (thus turn−off the IGBT), if the saturation voltage rises above the $V_{DESAT-THR}$. This protection works on every turn−on phase of the IGBT switching period.

At the beginning of turning−on of the IGBT, the collector−emitter voltage is much higher than the saturation voltage level which is present after the IGBT is fully turned on. It takes almost 1 μs between the start of the IGBT turn−on and the moment when the collector−emitter voltage falls to the saturation level. Therefore the comparison is delayed by a configurable time period (blanking time) to prevent false triggering of DESAT protection before the IGBT collector−emitter voltage falls below the saturation level. Blanking time is set by the value of the capacitor CBLANK.

The exact principle of operation of DESAT protection is described with reference to Figure 9.

At the turned−off output state of the driver, the DESAT pin is shorted to ground via the discharging transistor (Q_{DIS}). Therefore, the inverting input holds the comparator output at low level.

At the turned−on output state of the driver, the current $I_{DESAT-CHG}$ from current source starts to flow to the blanking capacitor CBLANK, connected to DESAT pin. Appropriate value of this capacitor has to be selected to ensure that the DESAT pin voltage does not rise above the threshold level $V_{DESAT-THR}$ before the IGBT fully turns on. The blanking time is given by following expression. According to this expression, a 47 pF CBLANK will provide a blanking time of (47p *6.5/0.25m =) 1.22 s.

$$t_{BLANK} = C_{BLANK} \times \frac{V_{DESAT-THR}}{I_{DESAT-CHG}} \quad \text{(eq. 1)}$$

After the IGBT is fully turned−on, the $I_{DESAT-CHG}$ flows through the DESAT pin to the series resistor RS−DESAT and through the high voltage diode and then through the collector and IGBT to the emitter. Care must be taken to select the resistor RS−DESAT value so that the sum of the saturation voltage, drop on the HV diode and drop on the $R_{S-DESAT}$ caused by current $I_{DESAT-CHG}$ flowing from DESAT source current is smaller than the DESAT threshold voltage. Following expression can be used:

$$V_{DESAT-THR} > R_{S-DESAT} \times I_{DESAT-CHG} + V_{F\_HV\_diode} + V_{CESAT\_IGBT} \quad \text{(eq. 2)}$$

Important part for DESAT protection to work properly is the high voltage diode. It must be rated for at least same voltage as the low side IGBT. The safety margin is application dependent.

The typical waveforms for IGBT overcurrent condition are outlined in Figure 10.

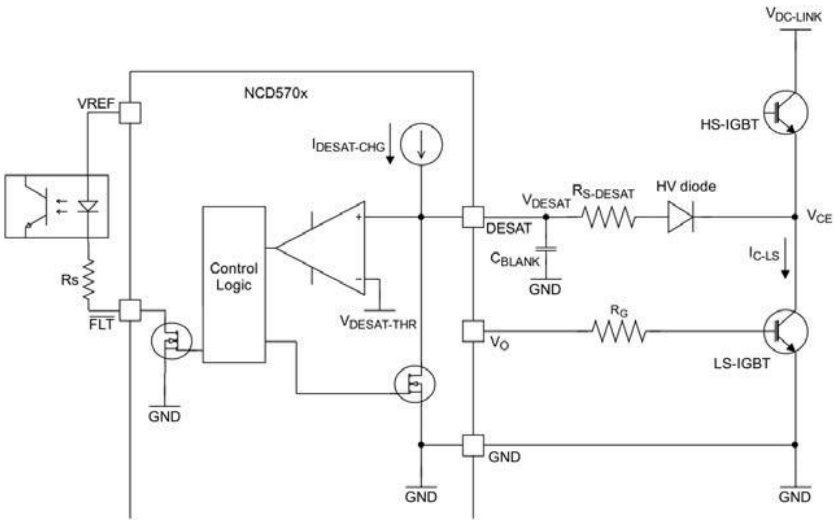


Figure 9. Desaturation Protection Schematic

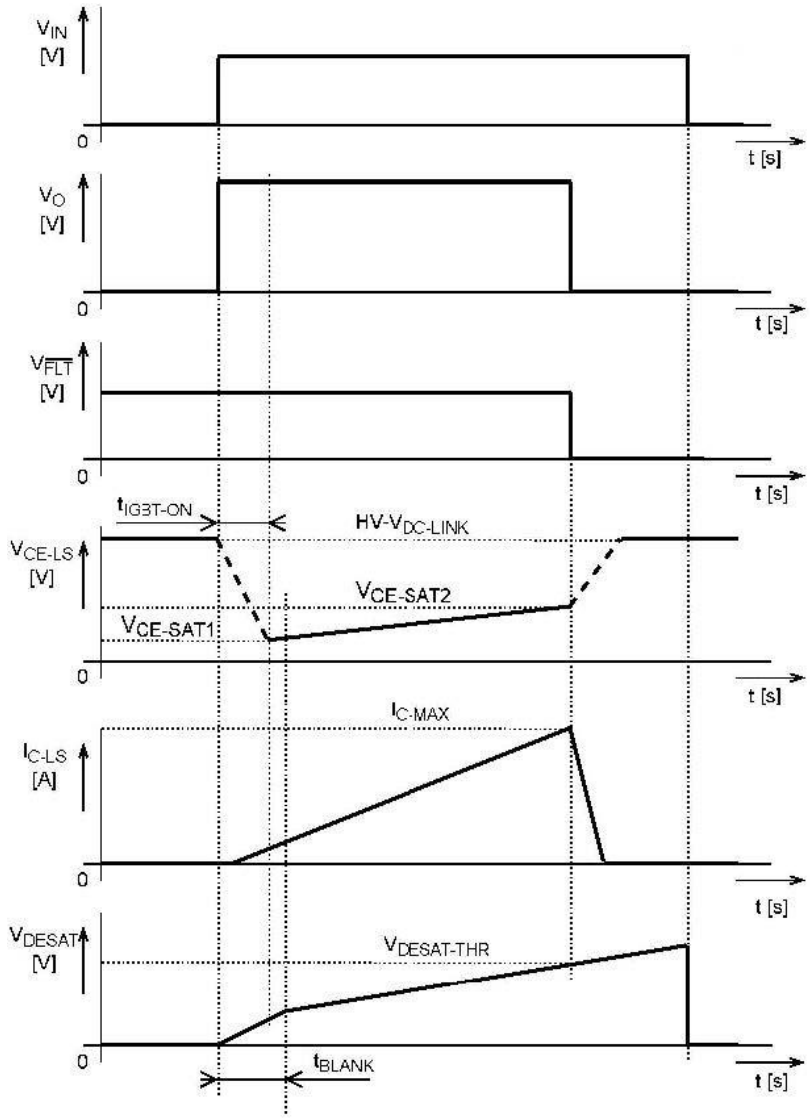


Figure 10. Desaturation Protection Waveforms

Input Signal

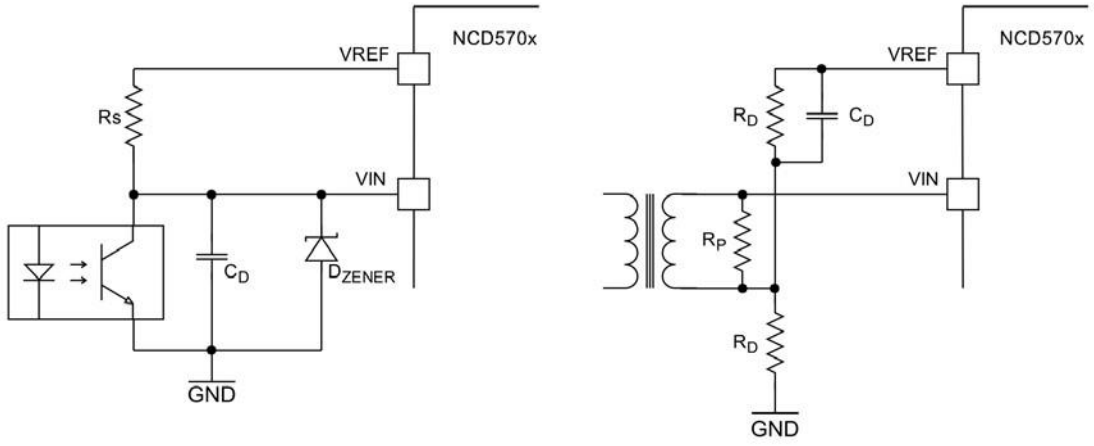


Figure 11. Opto−coupler or Pulse Transformer At Input

The input signal controls the gate driver output. Figure 11 shows the typical connection diagrams for isolated applications where the input is coming through an opto−coupler or a pulse transformer.

The relationship between gate driver input signal from a pulse transformer (Figure 12) or opto−coupler (Figure 13) and the output is defined by many time and voltage values. The time values include output turn−on and turn−off delays (t_{pd-on} and t_{pd-off}), output rise and fall times (t_{rise} and t_{fall}) and minimum input pulse−width (ton−min). Note that the delay times are defined from 50% of input transition to first 10% of the output transition to eliminate the load dependency. The input voltage parameters include input high (VIN−H1) and low (V_{IN-L1}) thresholds as well as the input range for which no output change is initiated (VIN−NC).

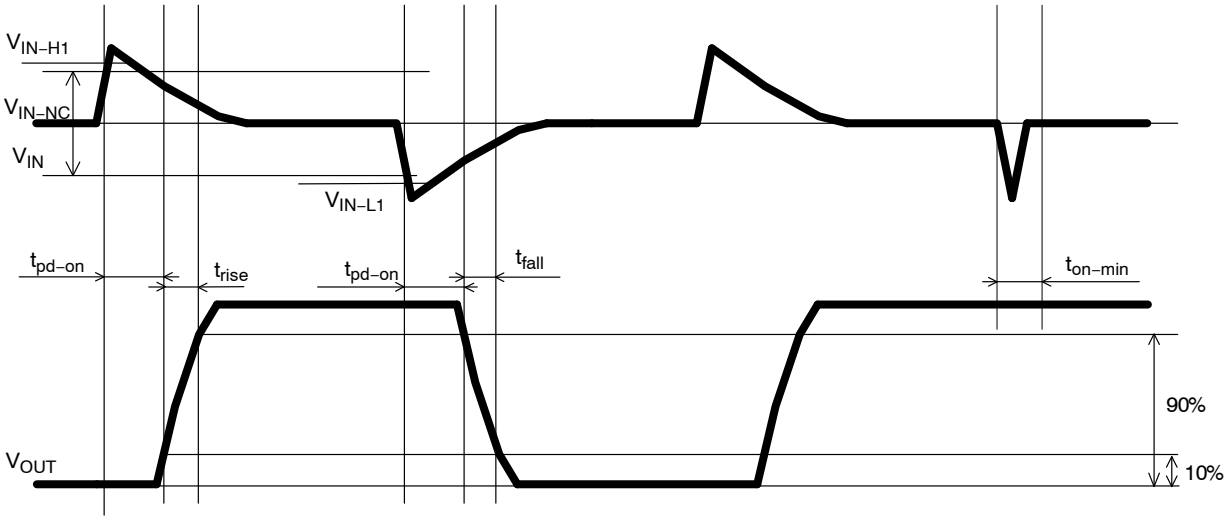


Figure 12. Input and Output Signal Parameters for Pulse Transformer

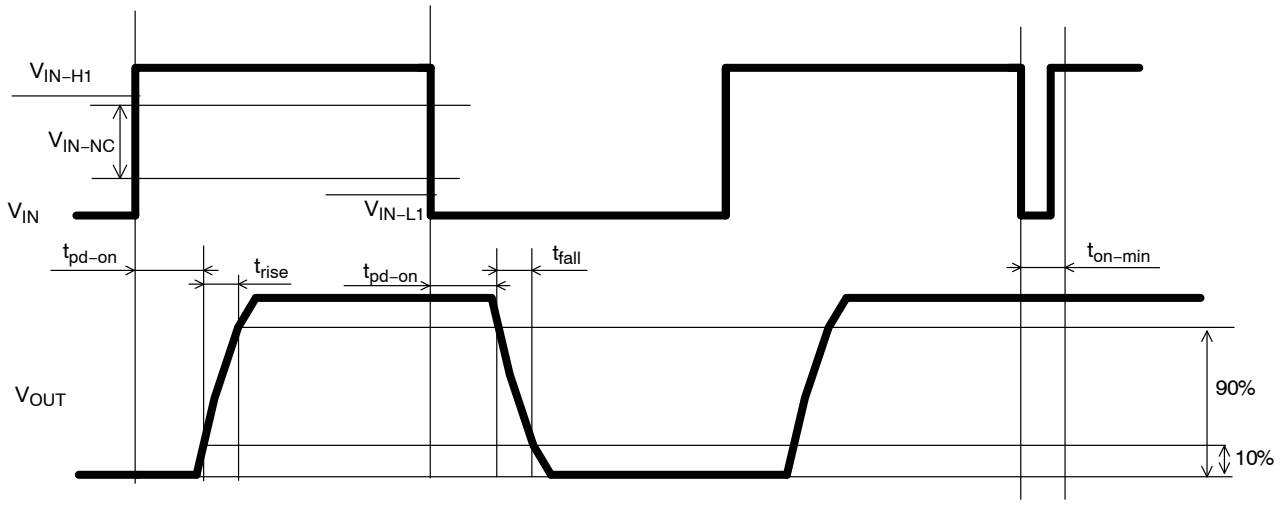


Figure 13. Input and Output Signal Parameters for Opto−coupler

Use of VREF Pin

The NCV5705B provides an additional 5.0 V output (VREF) that can serve multiple functions. This output is capable of sourcing up to 10 mA current for functions such as opto−coupler interface or external comparator interface. The VREF pin should be bypassed with at least a 100 nF capacitor (higher the better) irrespective of whether it is being utilized for external functionality or not. VREF is highly stable over temperature and line/load variations

Fault Output Pin

This pin provides the feedback to the controller about the driver operation. The situations in which the signal becomes active(low value) are summarized in the Table 6.

Table 6. FLT LOGIC TRUTH TABLE

VIN	UVLO	DESAT	Internal TSD	VOUT	FLT	Notes
L	Inactive	L	L	L	Open drain	Normal operation − Output Low
H	Inactive	L	L	H	Open drain	Normal operation − Output High
X	Active	X	L	L	L	UVLO activated − FLT Low ($t_{d3\text{-}FLT}$), Output Low ($t_{d3\text{-}FLT} + t_{d1-OUT}$)
L	Inactive	H	L	L	L	DESAT activated (only when V_{IN} is low) − Output Low (t_{d2_OUT}), FLT Low
X	Inactive	X	H	L	L	Internal Thermal Shutdown − FLT Low ($t_{d3\text{-}FLT}$), Out−put Low ($t_{d3\text{-}FLT} + t_{d1-OUT}$)

Thermal Shutdown

The NCV5705B also offers thermal shutdown function that is primarily meant to self−protect the driver in the event that the internal temperature gets excessive. Once the temperature crosses the T_{SD} threshold, the FLT output is activated after a delay of $t_{d3\text{-}FLT}$. After a delay of t_{d1-OUT} (12 μs), the output is pulled low and many of the internal circuits are turned off. The 12 μs delay is meant to allow the controller to perform an orderly shutdown sequence as appropriate. Once the temperature goes below the second threshold, the part becomes active again.

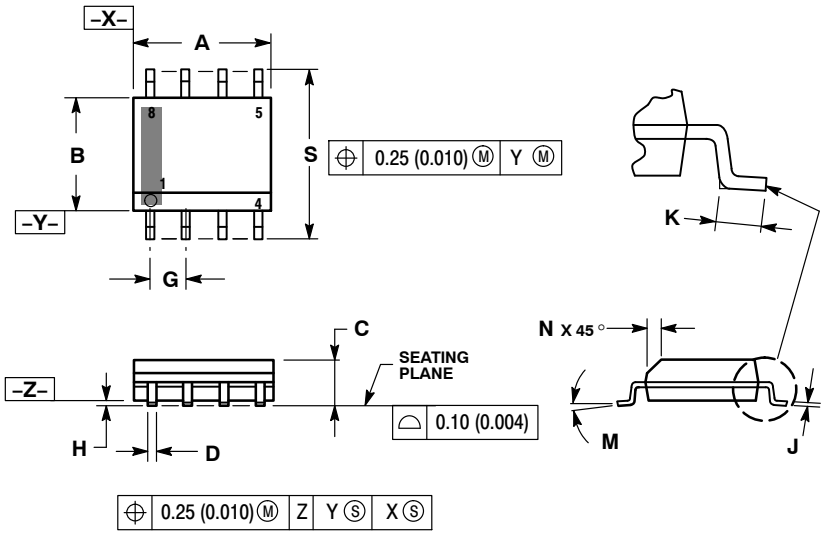
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

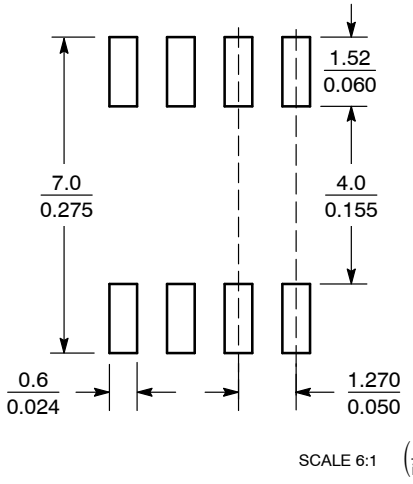
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

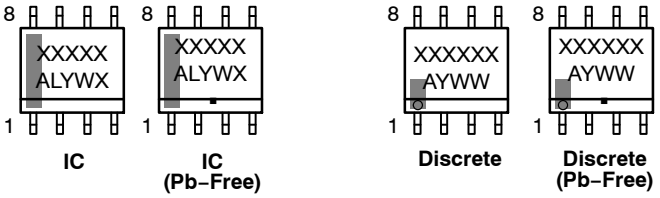
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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