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Devices Connected/Referenced	
AD5560	1.2 A Programmable Device Power Supply
AD7685	16-Bit, 250 kSPS PulSAR® ADC
ADR435	5 V Ultralow Noise XFET® Voltage Reference

Integrated Device Power Supply (DPS) for ATE with Output Voltage Range 0 V to 25 V

CIRCUIT FUNCTION AND BENEFITS

In the past, DPS (device power supply) solutions were designed from discrete amplifiers, switches, DACs, resistors, etc. New silicon processes and shrinking silicon now allow highly integrated solutions, but it's rarely possible to put everything onto one single piece of silicon. Even with its high level of integration, the AD5560 DPS requires a few well chosen external components to provide a complete system solution. The goal of this circuit note is to describe in more detail what is required and why it was selected and to provide a more complete device power supply solution.

This product is used primarily in the automatic test equipment (ATE) industry as the power supply that drives the device under test (DUT). As such, there are many different requirements placed on the DPS, including voltage and current specifications (depending on the type of DUT it will drive), and other factors, such as stability, accuracy, etc.

As a device power supply, it is of utmost importance that the AD5560 can deliver the voltage and currents required by the DUT in a timely manner.

The AD5560 is designed to achieve a peak-to-peak voltage span of 25 V that can be placed anywhere within the range of −22 V to +25 V, limited by the maximum allowable voltage of |AVDD − AVSS| ≤ 33 V.

In addition, the current range that the AD5560 can deliver can be as high as ±1.2 A. Note that 1.2 A isn't practical at the higher output voltages because of the power dissipation limitations of the package.

The 1.2 A capability is primarily intended for supplying a low voltage rail no greater than approximately 3.5 V, but this depends greatly on the cooling abilities and other conditions. Therefore, in reviewing the voltage/current requirements, many factors need to be taken into account, such as headroom, footroom, power dissipation under worst case conditions, supply rails, thermal performance, etc.

This circuit is designed to deliver three DUT rails:

0 V to 25 V @ 5 µA to 25 mA

0 V to 7 V @ 500 mA

0 V to 3 V @ 1.2 A

The selection of components and configuration of the circuit will be tailored specifically for the above combinations.

For alternative use or just for more detailed information on the part itself, refer to the AD5560 data sheet.

CIRCUIT DESCRIPTION

The AD5560 DPS covers the voltage supply and the measuring functions that the DUT needs, but to complete the rest of the circuit, there are a few more components required: a reference voltage, an ADC to digitize the measured result, and a thermal monitor to measure the temperature of the internal sense diodes, allowing users to view the thermal gradient across the die or, alternatively, across their PC board.

The ADC is used to digitize the measurement output. The measurement output (MEASOUT pin) can deliver different output ranges, depending on the voltage reference and on where the OFFSET DAC is set.

The OFFSET DAC is what is used to offset the Force Voltage output range to achieve different output ranges. The particular output range we are concerned about here is 0 V to 25 V. As a result, the default MEASOUT output range (MEASOUT GAIN = 1) will also be 0 V to 25 V. There are no ADCs with input ranges that can handle this directly, so there needs to be some external signal conditioning to match this range to that of any bipolar or unipolar ADC.

There is an alternative MEASOUT setting (MEASOUT GAIN = 0.2), which scales and offsets the MEASOUT output range to 0 V to 5.125 V. (Some slight overrange is included here for calibration, etc.)

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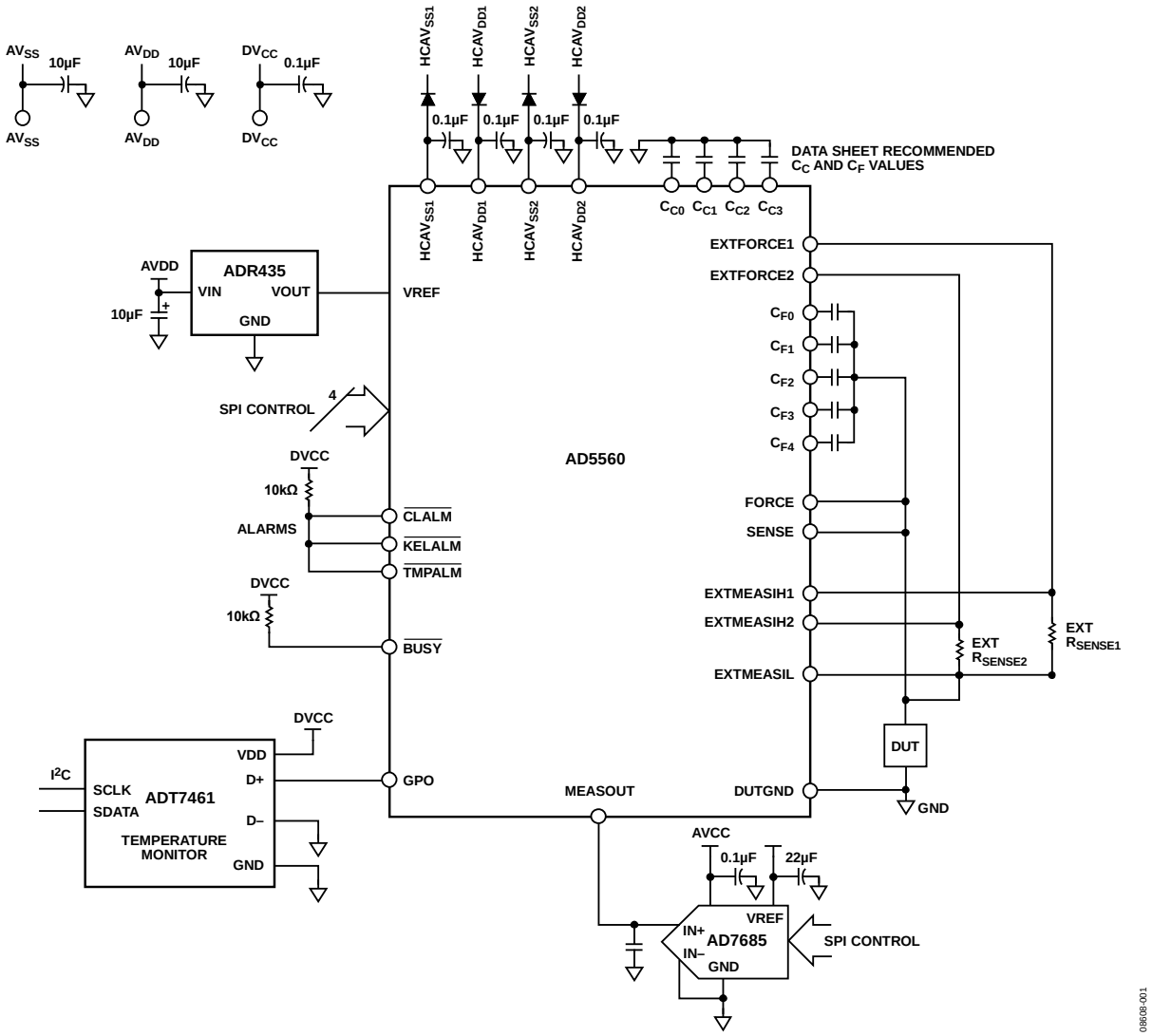

Figure 1. Device Power Supply (DPS) for ATE (Simplified Schematic: Decoupling and All Connections Not Shown)

For this example, we will use the 0 V to 5.125 V range; this will allow us to easily use a unipolar input ADC.

The 16-bit 250 kSPS AD7685 ADC was chosen for this application due to its ability to handle the 0 V to 5 V output range on the MEASOUT path. In addition to this, the availability of other ADCs with faster speeds in the same footprint (AD7686, 500 kSPS) also makes it very attractive for upgrade paths.

ADC Considerations

An ADC can be dedicated to each individual DPS channel, providing the fastest throughput; or an ADC can be shared across multiple channels. In many typical applications, a single ADC is shared across 8 or 16 channels.

Sharing an ADC across multiple channels can be accomplished using the internal "Disable" feature of each MEASOUT pin. This requires a write command to the DPS register to enable/disable the appropriate switch. If this method is chosen, note that no more than one MEASOUT should be selected at any one time.

Alternatively, an external 4:1 or 8:1 multiplexer can be used to control the measurement channel selection. In this way, all MEASOUT paths can be enabled, and the multiplexer takes care of the selection. Similarly, a 16:1 multiplexer allows more measurement paths to share a single ADC. The choice of this multiplexer will depend on the ADC used and its input voltage range. (For bipolar input ADCs, the ADG1404/ADG1204 would be ideal; while for single-supply usage, the ADG706 or ADG708 would be more suited.) The output impedance of the MEASOUT path is typically 60 Ω; in addition to the switch impedance, an ADC buffer should be considered to drive the

ADC (the ADA4898-1 is an example of an op amp that would be suitable).

Voltage Reference

The ADR435 5 V X-FET reference was chosen because a 25 V output voltage range was required. This reference has excellent temperature drift performance and low noise and is capable of driving multiple PMU channels.

Thermal Monitor

The AD5560 has an array of 16 thermal monitoring diodes placed at various points on the chip. These diodes must be driven with a current to produce a voltage, which is an indicator of the temperature in that area of the die. The reason for having so many thermal diodes on chip is to allow users to measure the temperature gradient across the chip or, alternatively, across their board under their specific conditions. For this purpose, ON Semiconductor's ADT7461A temperature monitor was chosen to interface with the on-chip thermal diodes. The ADT7461A has series resistance cancellation, which is important in this case because each of the diodes are muxed to the GPO pin of the AD5560. The multiplexer on-resistance would produce measurement errors without the series resistance cancellation feature. Note that the ADT7461A has a two-wire interface.

Compensation and Feedforward Capacitors

As a device power supply, the AD5560 can see a wide range of capacitive loads depending on the DUT bypassing and decoupling requirements. This design handles capacitive loads from 0 µF up to 160 µF. The external capacitors shown in Table 1 are required in order that the internal compensation algorithm will achieve optimum stability and settling into this load range.

Table 1. Suggested Compensation Capacitor Selection for DUT Capacitance of 0 µF to 160 µF

Capacitor	Value
C_{C0}	100 pF
C_{C1}	100 pF
C_{C2}	330 pF
C_{C3}	3.3 nF
C_{F0}	4.7 nF
C_{F1}	22 nF
C_{F2}	100 nF
C_{F3}	470 nF
C_{F4}	2.2 µF

Although there are four compensation input pins (C_{CX}) and five feedforward capacitor inputs pins (C_{FX}), the user may need to use all capacitor inputs only if large variations in DUT load capacitances are expected. If the DUT load capacitance is known and doesn't change for all combinations of voltage ranges and test conditions, then it is possible only one set of C_{CX} and C_{FX} capacitors are required. More details on the compensation algorithm are described in the AD5560 data sheet.

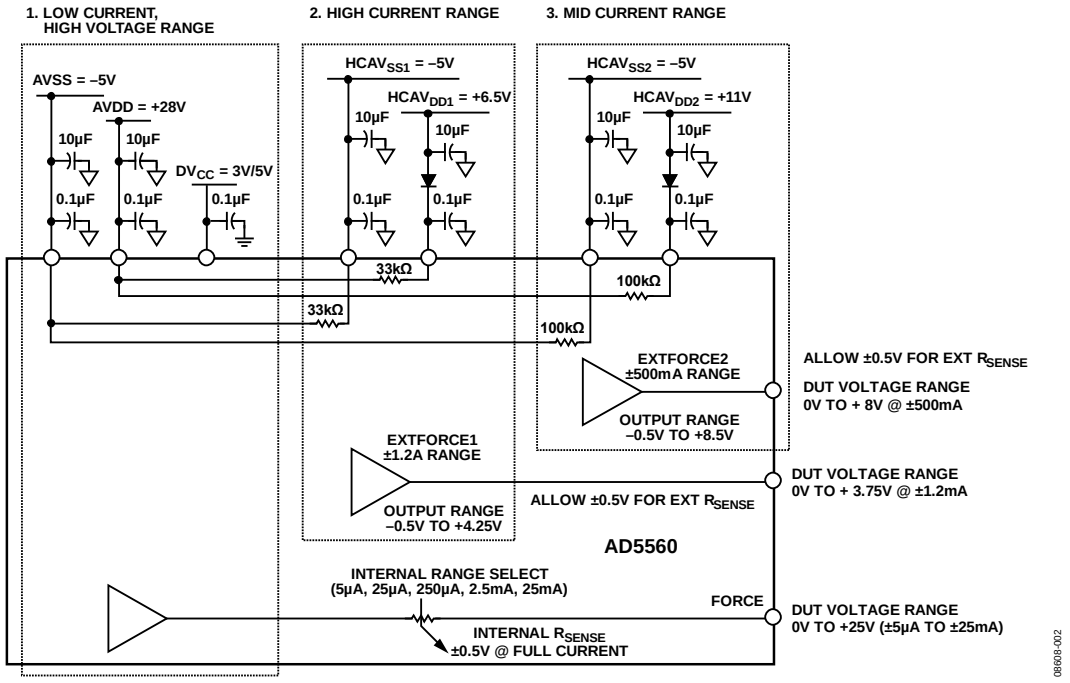

Figure 2. One Example of Using the Extra Supply Rails Within the AD5560 to Achieve Multiple Voltage/Current Ranges and Minimize Power Dissipation (Simplified Schematic: Decoupling and All Connections Not Shown).

The voltage range for the C_{CX} and C_{FX} pins is the same as the voltage range expected on FORCE; therefore, choice of capacitors should take this into account. C_{FX} capacitors can have 10% tolerance; this extra variation directly affects settling times, especially when measuring current in the low current ranges. C_{CX} should be at ≤5% tolerance.

Output Voltage Range

The output voltage ranges for this design are as follows:

0 V to 25 V @ 5 µA to 25 mA

0 V to 7 V @ 500 mA

0 V to 3 V @ 1.2 A

To configure these combinations of rails, we need to adjust the OFFSET DAC setting from the default. A suggested value of 0xD1D would achieve the ranges above. The diagram in Figure 2 shows an example of how the AD5560 is partitioned to achieve these output ranges.

High Current (HC) Supply Path Diodes

Because the AD5560 can output high power, offering current ranges up to 1.2 A, the power supply rails are broken out into three different power rails: the low current range (5 µA to 25 mA) is powered from AVDD/AVSS; the medium current range, named EXT2, is powered from HCAVDD2/HCAVSS2; the high current range, named EXT1, is powered from HCAVDD1/HCAVSS1. The HC supplies should always be equal to or less than the AVDD/AVSS rails. The purpose of the HC rails is to allow the user to choose lower voltage supplies to reduce the power dissipated in the AD5560. The design of the EXT1 and EXT2 output stage requires them to be supplied by a voltage higher than the voltage present at the DUT; if the HC supplies are lower than the AVDD/AVSS supplies, then there are situations where this might not be the case. As a result, we recommend that a diode be added into the path between the HC supply and the HC package pin (as shown in Figure 1). When either the EXT1 or EXT2 stages are off, we want to keep them off and keep them from leaking onto the DUT, so this diode, in conjunction with the internal bleed resistor, will allow the HC package pin voltage to increase (close to the AVDD/AVSS rail), thereby keeping the EXT1/EXT2 output stages in the off condition. Now, in the example we have shown here, the AVSS, HCVSS1, and HCVSS2 pins are all at –5V, therefore, there is no need for the diode in the HCVSS paths for these particular conditions. Details of the diode circuits for the EXT1 and EXT2 ranges are shown in Figure 3 and Figure 4, respectively.

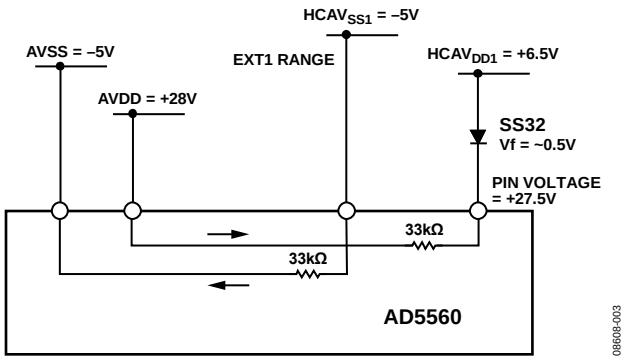

Figure 3. Example of Diodes Used for EXT1 Range

The diode needs to be able to carry the highest current that the stage can deliver (including instantaneous current/fault conditions). The EXT1 range will likely have much higher current requirements than that of the EXT2 stage; therefore, when choosing diodes, it will likely work best (in terms of board size) to choose separate diodes for EXT1 and EXT2.

The voltage drop should be as low as possible to minimize the overall power dissipation and supply overheads.

The leakage or reverse current when the diode is off should be low enough to ensure that the HC pin voltage can support the DUT output voltage range. The reverse current of the diode develops a voltage drop across the internal bleed resistor (33 kΩ for EXT1 and 100 kΩ for EXT2); the HC pin voltage will be lower as a result.

Suitable diodes are available from many vendors, such as ON Semiconductor, Vishay, etc.

An alternative to a diode would be a low on-resistance power MOSFET instead, as shown in Figure 5. Using a MOSFET has the advantage of reducing the overall power dissipation because the drop across the FET would be much less than that of a diode.

Note that discrete power MOS devices have a parasitic body diode between drain and source. The direction of this diode must be in the same direction as the normal diodes the MOS devices are replacing. A suitable driver for the MOS gate must also be provided.

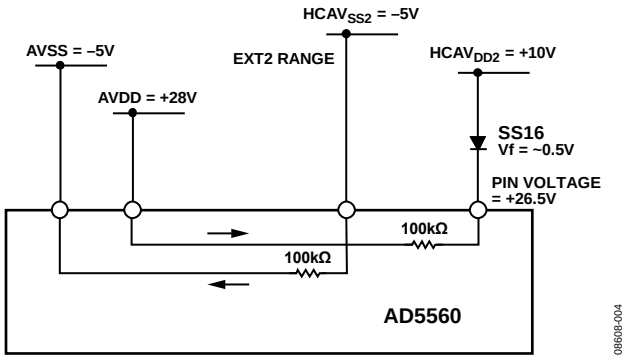

Figure 4. Example of Diodes Used for EXT2 Range.

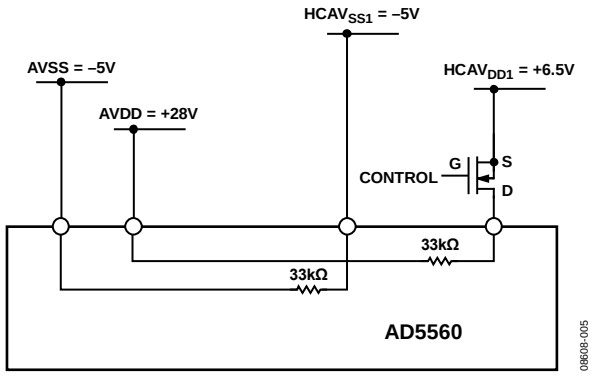

Figure 5. Example of Using MOSFET Instead of a Diode

The circuit must be constructed on a multilayer PC board with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"* and Tutorial MT-101, *Decoupling Techniques*). Note that Figure 1 is a simplified schematic and does not show all the necessary decoupling. Careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the printed circuit board (PCB) on which the AD5560 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5560 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. Establish the star ground point as close as possible to the device.

Linearity Measurements

Linearity measurements on the system in the FVMV (force voltage, measure voltage) mode are shown in Figure 6 and Figure 7. Figure 6 shows linearity for skewed power supplies (+28 V, −5 V). Linearity performance for this particular gain setting (MEASOUT GAIN = 0.2) degrades with skew supply conditions. Figure 7 shows improved linearity for symmetrical power supplies (±15 V). Both measurements were made with the AD7685 ADC using the circuit shown in Figure 1. Linearity measurements in the FVMI (force voltage, measure current) mode are shown in Figure 8 for symmetrical power supplies.

Thermal Measurements

An example of the thermal gradients measured using the ADT7461A is shown in Figure 9. The heat sink used here is just a simple heat sink with no air flow present. The intent is to give an idea of the thermal gradient across the die using the on-chip thermal diodes under a load of 1 A, power dissipated approximately 5.4 W. The diodes are numbered (per the data sheet), and this example cycles through some of the diodes at different points in time. Even with this simple heat sink, temperature differences of 17°C can be seen across the die.

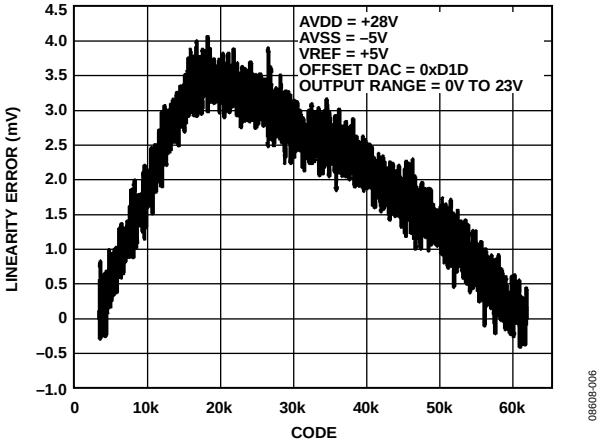

Figure 6. Typical Linearity Performance Using the AD7685 to Measure FVMV (Force Voltage, Measure Voltage) Linearity Error Referred to the DUT. +28 V, −5 V Skewed Power Supplies. Note That This Includes FV Error.

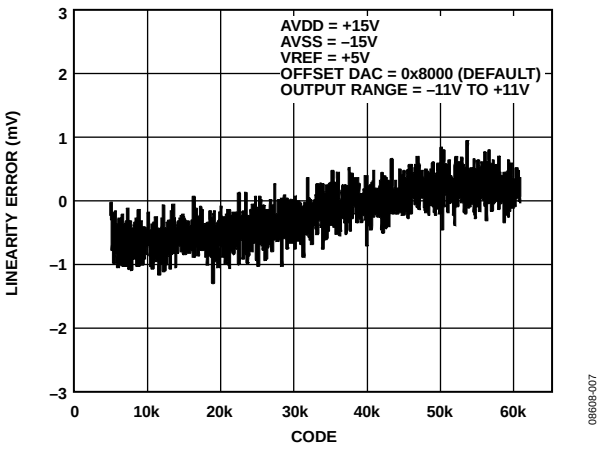

Figure 7. Typical Linearity Performance Using the AD7685 to Measure FVMV Linearity Error Referred to the DUT, ±15 V Symmetrical Power Supplies. Note That This Includes FV Error (Linearity Performance Under These Supply Conditions is Superior to That of Skewed Supply Shown in Figure 6).

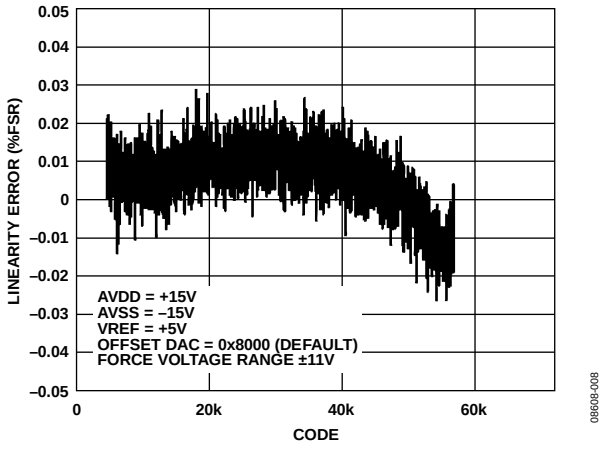

Figure 8. Typical Linearity Performance Using AD7685 to Measure FVMI (Force Voltage, Measure Current) Linearity Error, ±15 V Symmetrical Power Supplies .

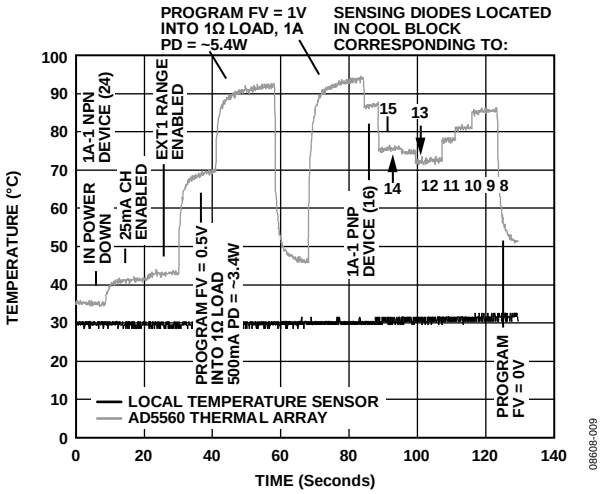

Figure 9. Example of Using the ADT7461A as the Thermal Monitor (X-Axis Is Time in Seconds).

COMMON VARIATIONS

Depending on the type of DUT being driven, DPS circuits don't always need to use a full 25 V range. For example, the use of the ADR421 (2.5 V) voltage reference allows the user to achieve a lower output voltage range (±6.4 V nominally). This can be scaled to suit the DUT requirements by using the on-chip OFFSET DAC (see the ADR421 data sheet for more detail). If the voltage range required is even smaller than this, simply use the gain setting "m" register to shrink the range even further. It's possible to use a scaling factor of ¼ for "m" and still retain 16-bit resolution. For these low voltage applications, there is no need for AVDD/AVSS to be high voltage rails, since the AD5560 is designed to work with a much smaller supply differential such that |AVDD – AVSS| ≥ 16 V. This helps by reducing the power dissipated in the AD5560. See the AD5560 data sheet for further details.

Variations in partitioning of DPS measurement channels per ADC channel might mean that one ADC channel is shared among more PMU channels (sometimes 8:1 or 16:1 ratios). The on-chip MEASOUT disable feature can be used. Alternatively, an analog multiplexer can be used for this function. This adds additional series resistance into the measurement path, so consideration should be given to buffering the measurement path prior to the ADC input. Many of the ADC data sheets include recommendations for suitable ADC drivers.

The 16-bit 250 kSPS AD7685 ADC was chosen for this application due to its ability to handle the 0 V to 5 V output range on the MEASOUT path. In addition to this, the availability of other ADCs with faster speeds in the same footprint (AD7686, 500 kSPS) also makes it very attractive for upgrade paths.

Other ADCs can also be selected, such as those with bipolar ranges or faster sampling rates. If external multiplexers are used, the ADG1404/ADG1204 are ideal for bipolar input ADCs; while for single-supply usage, the ADG706 or ADG708 would be more suited.

The output impedance of the MEASOUT path is typically 60 Ω; in addition to the switch impedance, an ADC buffer should be considered to drive the ADC (the ADA4898-1 is an example of an op amp that would be suitable).

Selecting the Right Supplies for an Output Voltage Range of ±10V Device Power Supply (DPS) for ATE

In the example shown in Figure 10 the AD5560 is supplied with symmetrical supply rails, and the design must deliver three DUT rails:

–10 V to +10 V @ ±5 µA to ±25 mA

–5 V to +5 V @ ±500 mA

0 V to 3 V @ +1.2 A

To configure these combinations of rails, we can use the default OFFSET DAC setting with a VREF = 5 V. This will achieve a nominal ±10 V output with plenty of over-range.

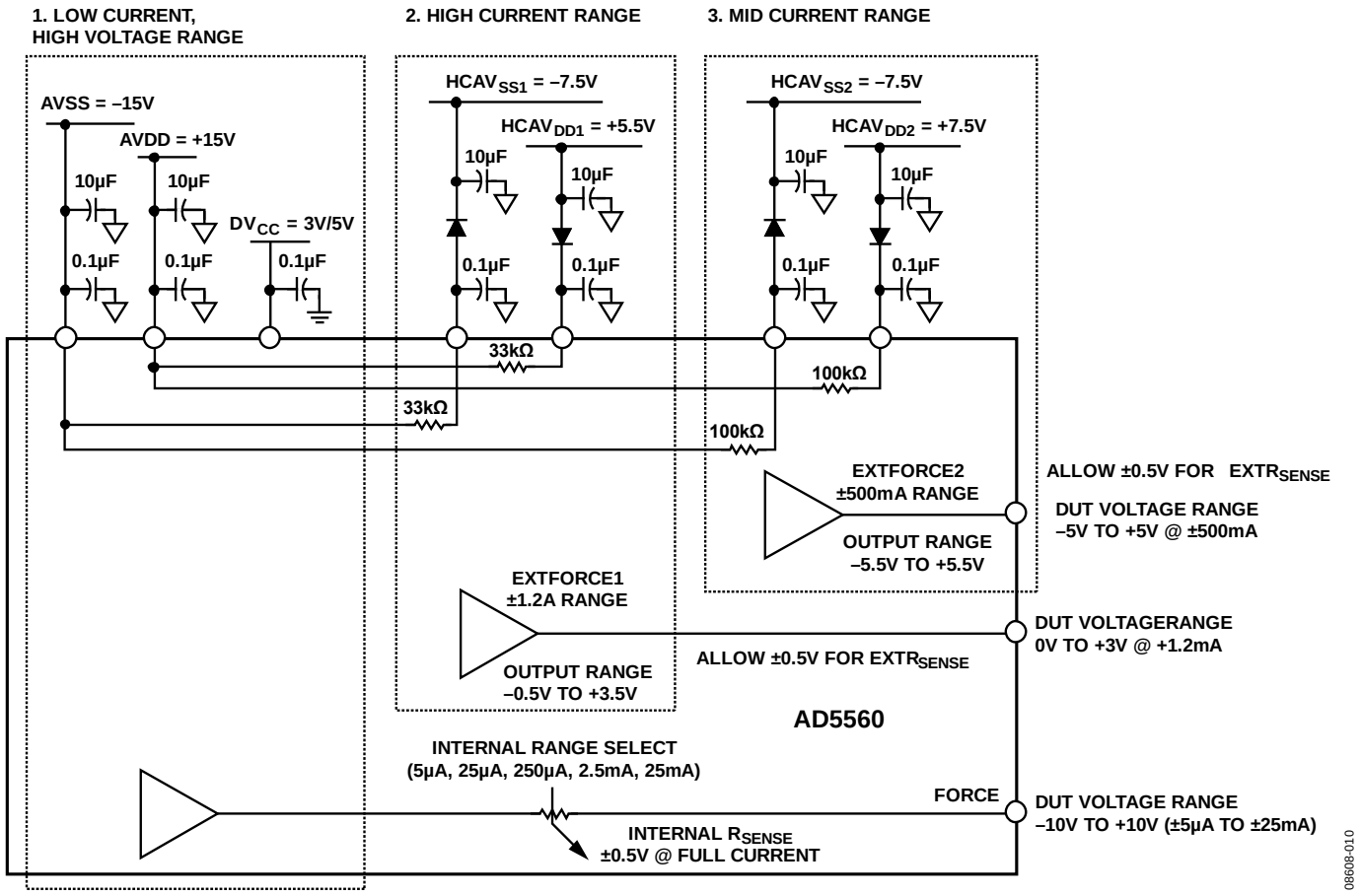

Figure 10. One Example of Using the Extra Supply Rails Within the AD5560 to Achieve Multiple Voltage/Current Ranges and Minimize Power Dissipation

High Current (HC) Supply Path Diodes

For the voltage conditions above, we now need to use a diode in both paths (HCVSS, HCAVDD) which is different from the previous discussion which used asymmetrical supply rails. Details of the diode circuits for the EXT1 and EXT2 ranges are shown in Figure 11 and Figure 12.

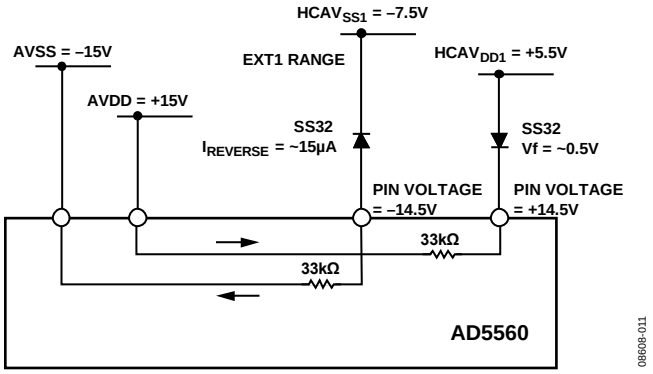

Figure 11. Example of Diodes Used for EXT1 Range

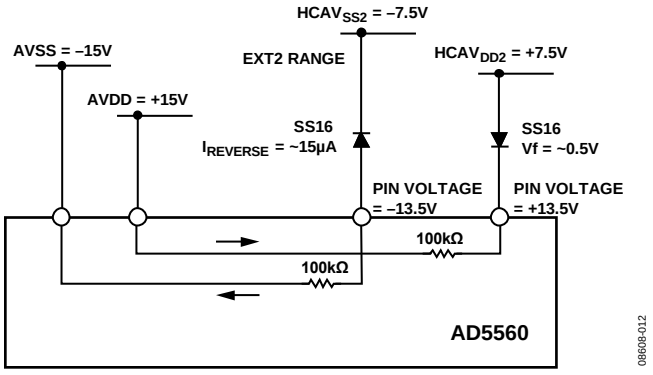

Figure 12. Example of Diodes Used for EXT2 Range.

Similarly, if using FETs in place of diodes, for these supply conditions, we will again need to use them in both supply paths as shown in Figure 13.

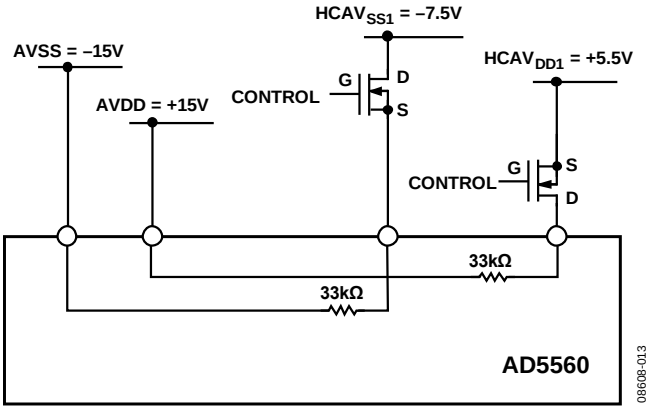

Figure 13. Example of Using MOSFET Instead of a Diode

Choosing $HCAV_{SSX}$ and $HCAV_{DDX}$ Supply Rails

Selection of $HCAV_{SSX}$ and $HCAV_{DDX}$ supplies is determined by the EXTFORCE1 and EXTFORCE2 output ranges. The supply rails chosen must take into account headroom and footroom, DUTGND voltage range, cable loss, supply tolerance, and V_{RSENSE}. If diodes are used in series with the $HCAV_{SSX}$ and $HCAV_{DDX}$ supplies pins, the diode voltage drop should also be factored into the supply rail calculation.

The AD5560 is designed for fast settling into large capacitive loads in high current ranges; therefore, when slewing, the device draws two to three times the nominal current from the $HCAV_{SSX}$ and $HCAV_{DDX}$ supplies. When choosing supply rails, ensure that they are capable of supplying each DPS channel with sufficient current to slew.

All output stages of the AD5560 are symmetrical; they can source and sink the rated current. Supply design and bypassing should account for this.

Figure 10 shows an example of how the AD5560 is partitioned to achieve these output ranges. In order to confine the number of supplies rails required in the system, the HCAVSS rails are both tied to −7.5V, because in this example, the HCAVSS1 rail is not required to deliver much current, therefore the power dissipation will not be high.

LEARN MORE

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MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND.* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques.* Analog Devices.

Voltage Reference Wizard Design Tool.

Data Sheets and Evaluation Boards

AD5560 Data Sheet

AD5560 Evaluation Board

AD7685 Data Sheet

AD7685 Evaluation Board

ADR435 Data Sheet

REVISION HISTORY

6/11—Rev. A to Rev. B

Changes to Common Variations 6

2/11—Rev. 0 to Rev. A

Changes to Circuit Function and Benefits 1
Changes to Figure 2 through Figure 5 3
Changes to Circuit Description 4

10/09—Revision 0: Initial Version