Vol 54 No 2, June 2020

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™
AnalogDialogue

StudentZone—ADALM2000 Activity: Common Emitter Amplifier

Doug Mercer, Consulting Fellow
and **Antoniu Miclaus**, System Applications Engineer

Objective

The purpose of this activity is to investigate the common emitter configuration of the bipolar junction transistor (BJT).

Background

The common emitter amplifier is one of three basic single-stage amplifier topologies. The BJT version functions as an inverting voltage amplifier. The base terminal of the transistor serves as the input, the collector is the output, and the emitter is common to both input and output (it may be tied to the ground reference or the power supply rail), which gives rise to its common name.

Materials

- ADALM2000 active learning module
- Solderless breadboard
- Five resistors
- One 50 kΩ variable resistor, potentiometer
- One small signal NPN transistor (2N3904)

Directions

The configuration, shown in Figure 1, demonstrates the NPN transistor used as the common emitter amplifier. Output load resistor R_L is chosen such that for the desired nominal collector current, I_C, approximately one half of the V_P (5 V) voltage appears at V_{CE}. Adjustable resistor RPOT, along with RB, sets the nominal bias operating point for the transistor (I_B) to set the required I_C. Voltage divider R1/R2 is chosen to provide a sufficiently large attenuation of the input stimulus from waveform generator W1. This is done to more easily view the generator W1 signal, given the rather small signal that will appear at the base of the transistor, V_{BE}. The attenuated waveform generator W1 signal is ac-coupled into the base of the transistor by the 4.7 µF capacitor so as not to disturb the dc bias condition.

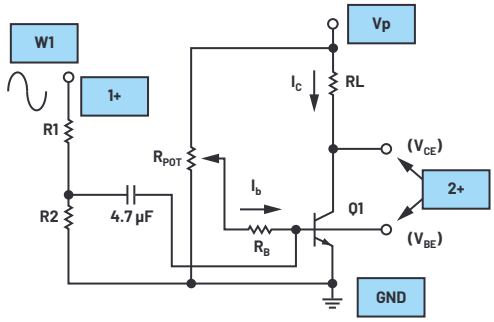

Figure 1. Common emitter amplifier test configuration.

Hardware Setup

The waveform generator output W1 should be configured for a 1 kHz sine wave with 3 V amplitude peak-to-peak and 0 V offset. The setup should be configured with Scope Channel 1+ connected to display the output W1. Scope Channel 2 (2+) is used to measure alternately the waveform at the base and collector of Q1.

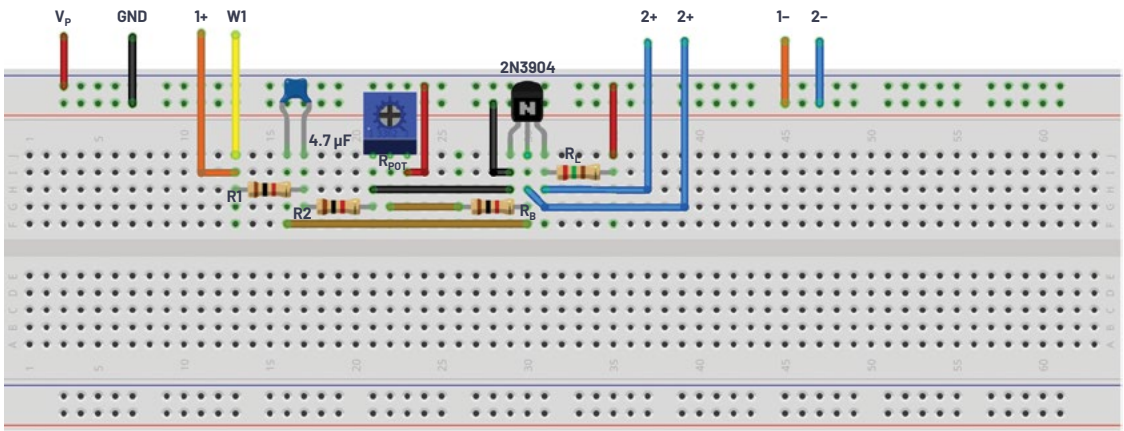

Figure 2. Common emitter amplifier test configuration breadboard connection.

Procedure

Turn on the power supplies connected to the collector (V_P = 5 V) of the BJT transistor.

Configure the oscilloscope instrument to capture several periods of the input signal and the output signal.

Plot examples of the simulated circuit using LTspice® are presented in Figure 3 and Figure 4.

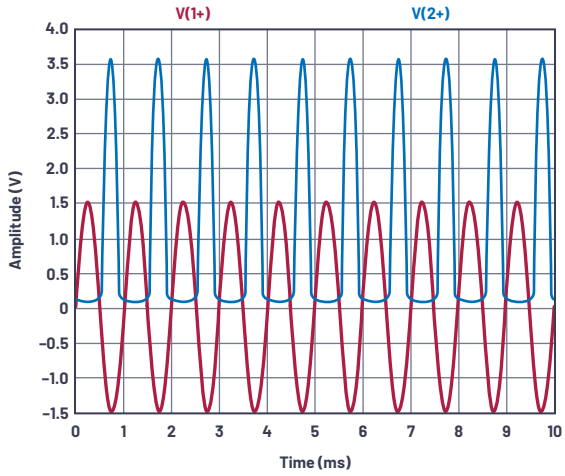

Figure 3. Common emitter amplifier test configuration, V_{IN} and V_{CE}.

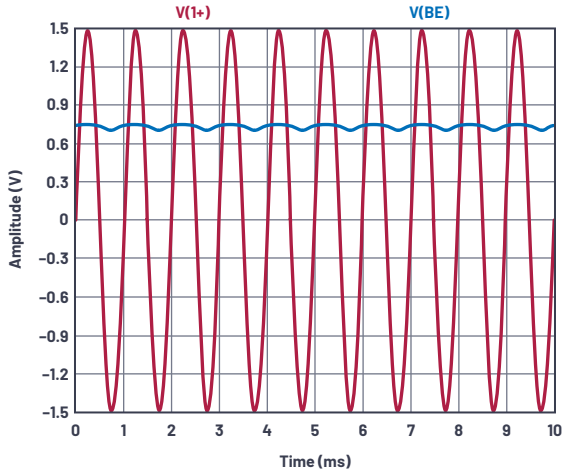

Figure 4. Common emitter amplifier test configuration, V_{IN} and V_{BE}.

The voltage gain, A, of the common emitter amplifier can be expressed as the ratio of load resistor R_L to the small signal emitter resistance, r_e. The transconductance, g_m, of the transistor is a function of the collector current I_C and the so-called thermal voltage, kT/q, which can be approximated by around 25 mV or 26 mV at room temperature.

$$g_m = \frac{1}{r_e} = \frac{-qI_C}{kT} \quad (1)$$

The small signal emitter resistance is $1/g_m$ and can be viewed as being in series with the emitter. Now with a signal applied to the base, the same current (neglecting base current) flows in r_e and the collector load R_L. Thus, gain A is given by the ratio of R_L to r_e.

$$A = \frac{-R_L}{r_e} = \frac{-qI_cR_L}{kT} \quad (2)$$

An alternative to produce a common emitter amplifier test circuit is shown in Figure 5. All the attributes are basically the same with two slight advantages. One is that the base current bias is no longer dependent on the exponential base voltage (V_{BE}). The second is that the summation of the small ac signal from the attenuated AWG 1 output is independent of the base bias circuit and does not need to be ac-coupled. The small signal ac input is applied to the noninverting terminal of the operational amplifier (op amp), and thus, due to the negative feedback, also appears at the base of the transistor (inverting op amp input).

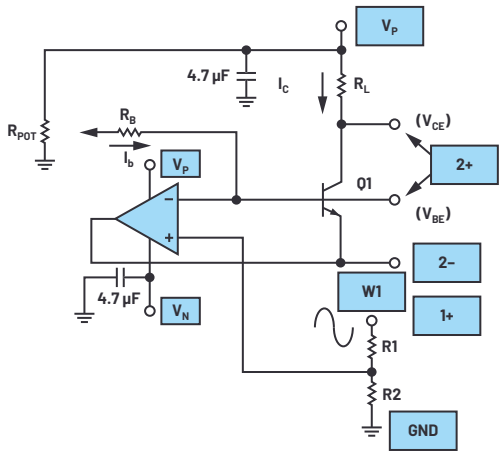

Figure 5. Alternate common emitter amplifier test configuration.

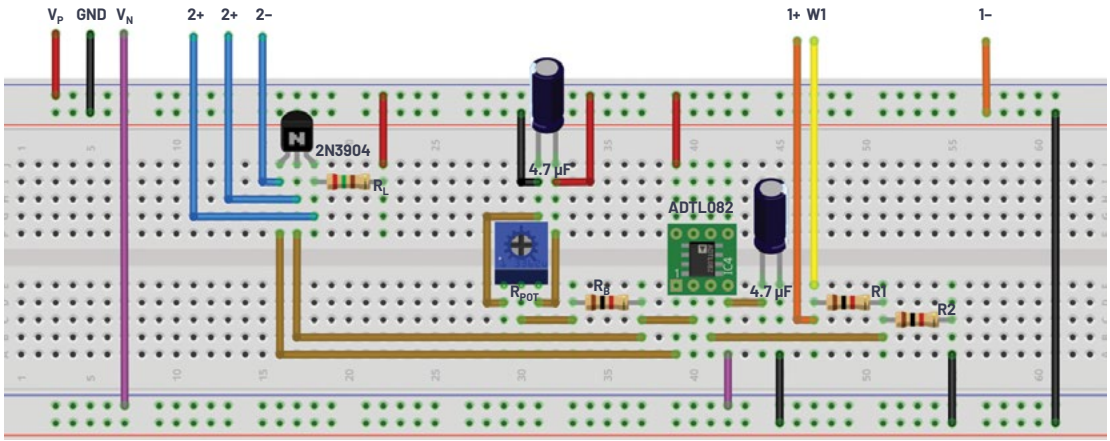

Figure 6. Alternate common emitter amplifier test configuration breadboard connection.

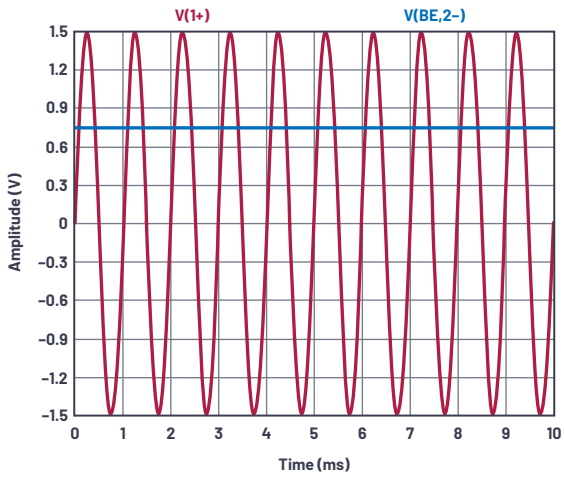

Figure 7. Alternate common emitter amplifier test configuration, V_{IN} and V_{BE}.

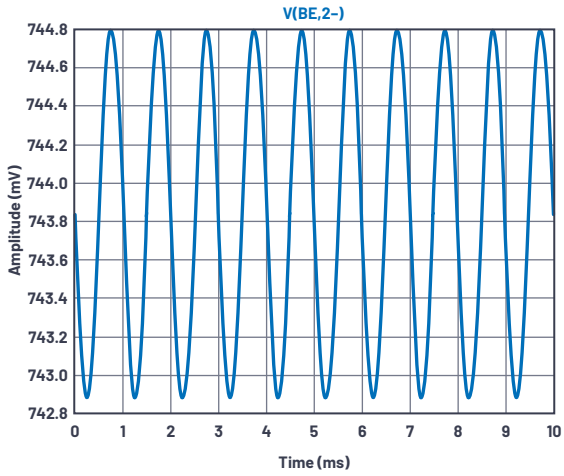

Figure 8. Alternate common emitter amplifier test configuration V_{BE} zoom.

Self-Biased Configuration with Negative Feedback

Objective

The purpose of this section is to investigate the effect of adding negative feedback to stabilize the dc operating point. One of the most frequently used biasing circuits for a transistor circuit is the self-biasing of the emitter-bias circuit where one or more biasing resistors are used to set up the initial dc values for the three transistor currents, I_B, I_C, and I_E.

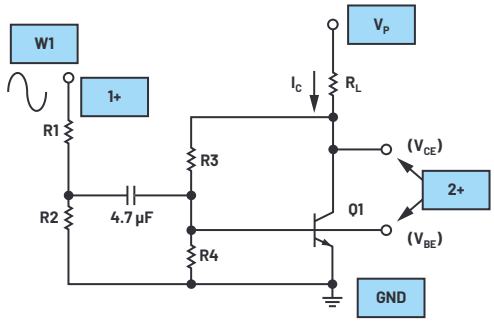

Figure 9. Self-biased configuration.

Hardware Setup

The waveform generator output W1 should be configured for a 1 kHz sine wave with 3 V amplitude peak-to-peak and 0 V offset. The setup should be configured with Scope Channel 1+ connected to display the output W1. Scope Channel 2 (2+) is used to alternately measure the waveform at the base and collector of Q1.

Procedure

Turn on the power supplies connected to the collector (V_P = 5 V) of the BJT transistor.

Configure the oscilloscope instrument to capture several periods of the input signal and the output signal.

Plot examples of the simulated circuit (using LTspice) are presented in Figure 11 and Figure 12.

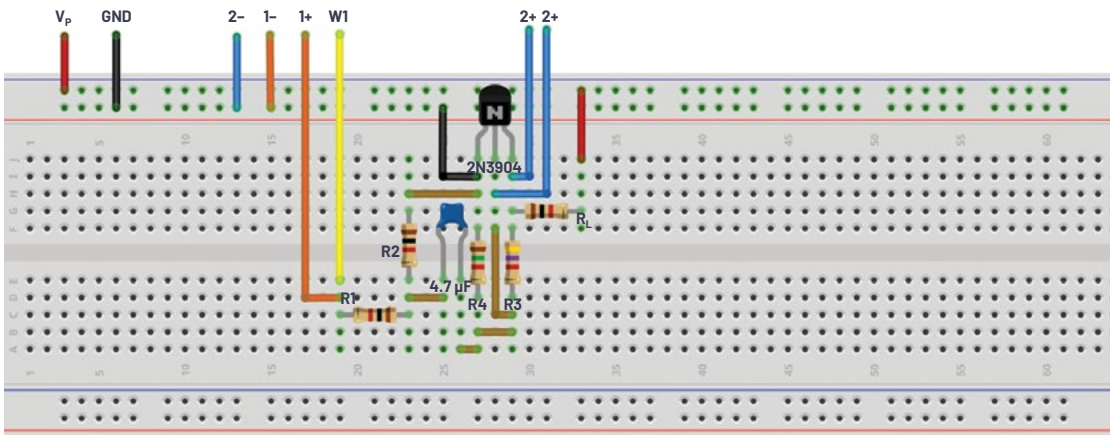

Figure 10. Self-biased configuration breadboard connection.

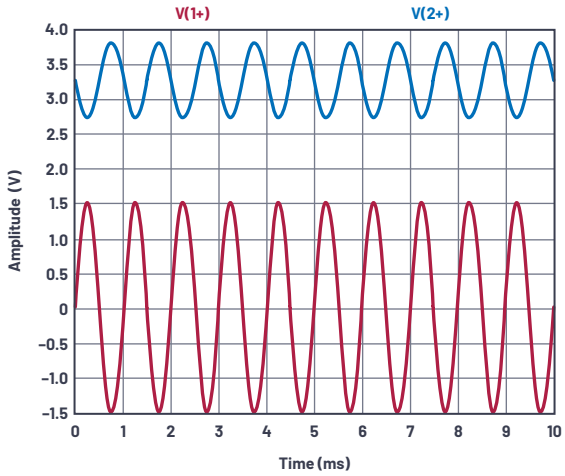

Figure 11. Self-biased configuration, V_{IN} and V_{CE}.

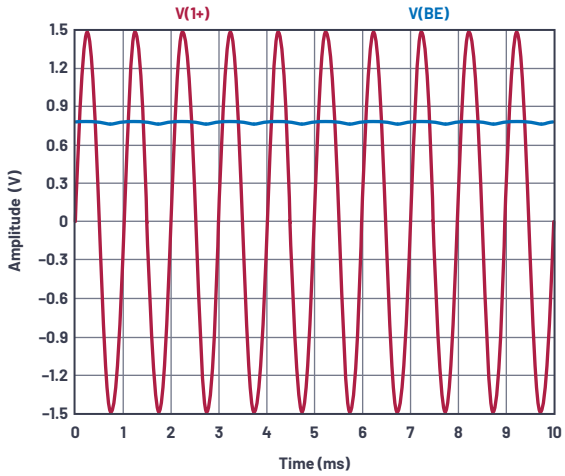

Figure 12. Self-biased configuration, V_{IN} and V_{BE}.

Adding Emitter Degeneration

Objective

The purpose of this activity is to investigate the effect of the addition of emitter degeneration.

Background

Common emitter amplifiers give the amplifier an inverted output and can have a very high gain and can vary widely from one transistor to another. Additionally, the gain is somehow unpredictable due to temperature and bias current dependence. By introducing a small value feedback resistor in the amplifier stage, the performance of the circuit can be improved.

Additional Materials

One 5 kΩ variable resistor, potentiometer

Directions

Disconnect the emitter of Q1 from ground and insert R_E, a 5 kΩ potentiometer, as shown in Figure 13. Adjust R_E while noting the output signal seen at the collector of the transistor.

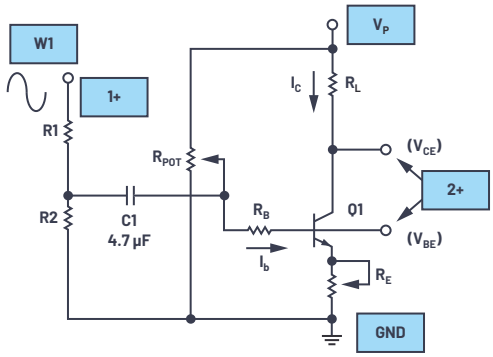

Figure 13. Emitter degeneration added.

Hardware Setup

The waveform generator output W1 should be configured for a 1 kHz sine wave with 3 V amplitude peak-to-peak and 0 V offset. The setup should be configured with Scope Channel 1+ connected to display output W1. Scope Channel 2 (2+) is used to alternately measure the waveform at the base and collector of Q1.

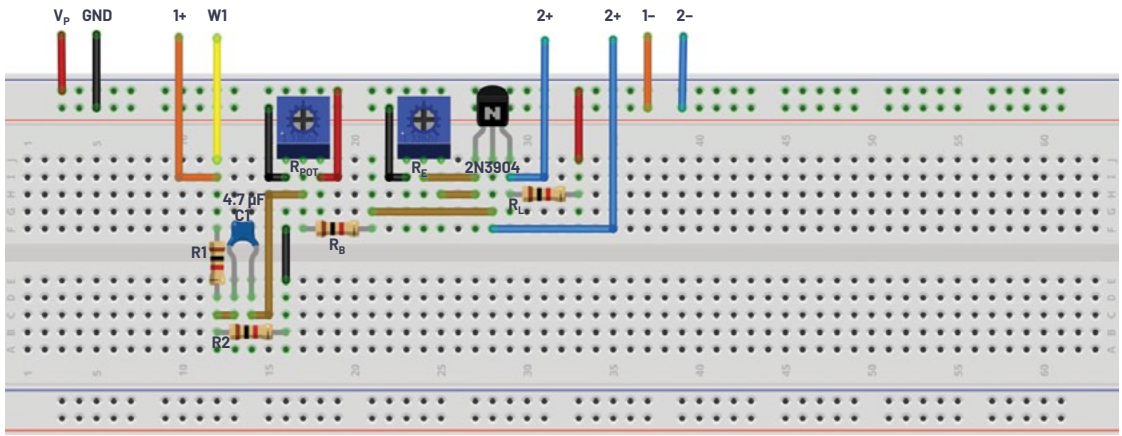

Figure 14. Emitter degeneration added breadboard connection.

Procedure

Turn on the power supplies connected to the collector (V_P = 5 V) of the BJT transistor.

Configure the oscilloscope instrument to capture several periods of the input signal and the output signal.

Plot examples of the simulated circuit (using LTspice) are presented in Figure 15 and Figure 16.

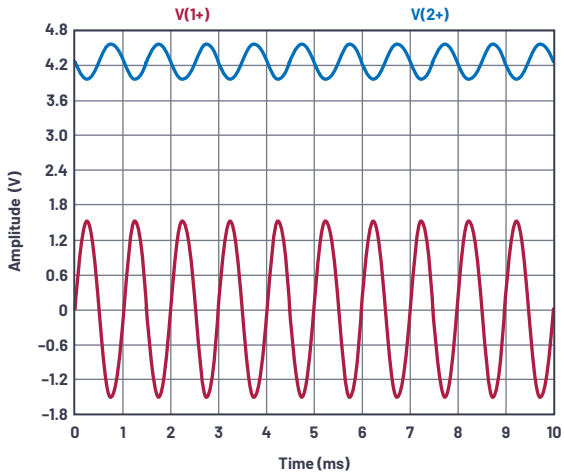

Figure 15. Emitter degeneration added, V_{IN} and V_{CE}.

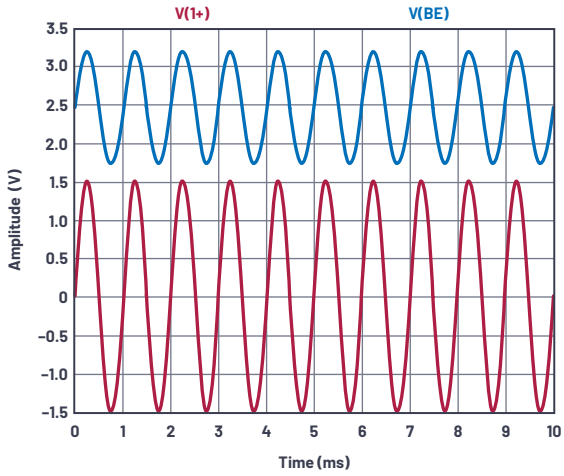

Figure 16. Emitter degeneration added, V_{IN} and V_{BE}.

Increasing AC Gain of an Emitter Degenerated Amplifier

Adding the emitter degeneration resistor has improved the stability of the dc operating point at the lower cost amplifier gain. A higher gain for ac signals can be restored to some extent by adding capacitor C2 across the degeneration resistor R_E, as shown in Figure 17.

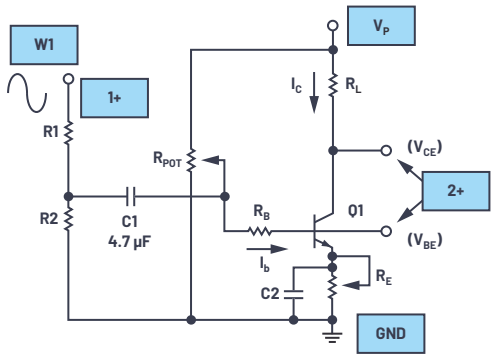

Figure 17. C2 added to increase ac gain.

Hardware Setup

The waveform generator output W1 should be configured for a 1 kHz sine wave with 3 V amplitude peak-to-peak and 0 V offset. The setup should be configured with Scope Channel 1+ connected to display the output W1. Scope Channel 2 (2+) is used to alternately measure the waveform at the base and collector of Q1.

Procedure

Turn on the power supplies connected to the collector (V_P = 5 V) of the BJT transistor.

Configure the oscilloscope instrument to capture several periods of the input signal and the output signal.

Plot examples of the simulated circuit (using LTspice) are presented in Figure 19 and Figure 20.

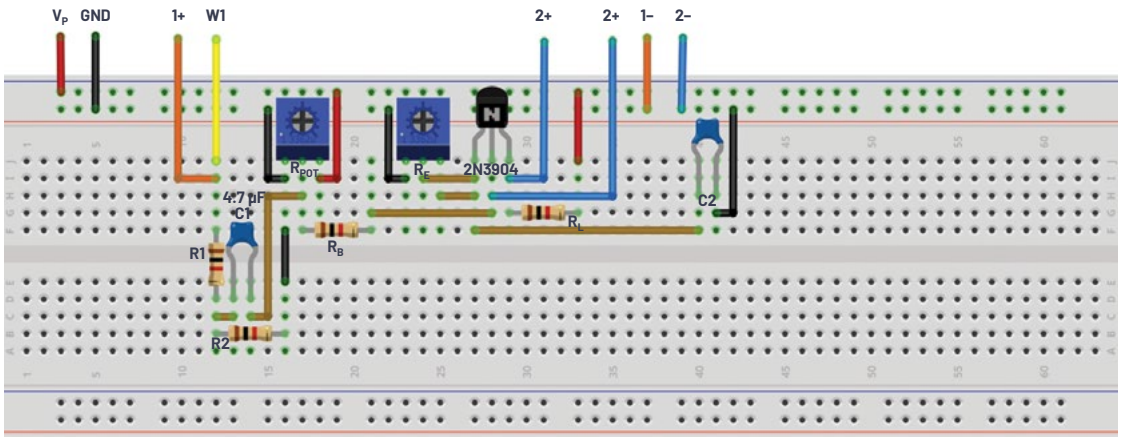

Figure 18. Breadboard connection with C2 added to increase the ac gain.

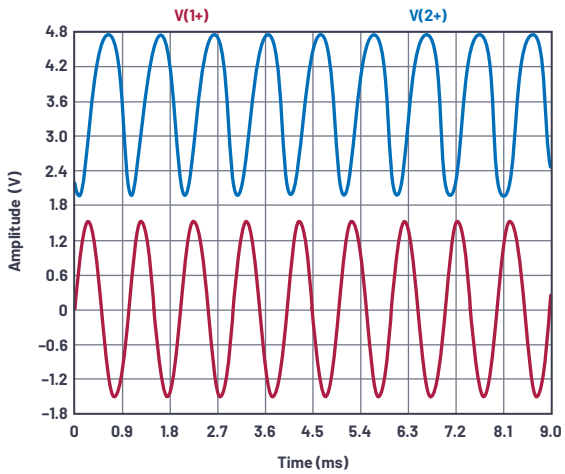

Figure 19. C2 added to increase the ac gain, V_{IN} and V_{CE}.

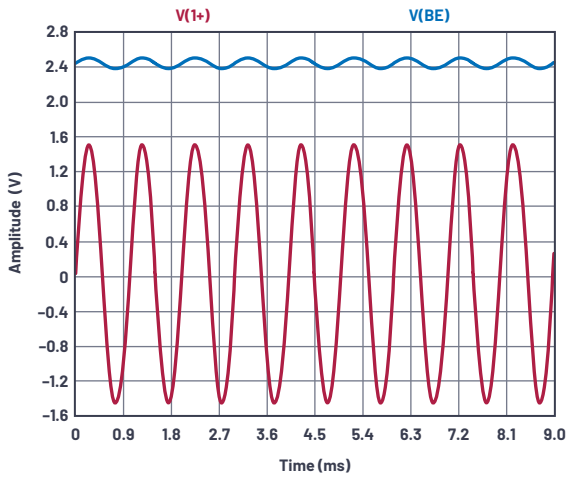

Figure 20. C2 added to increase the ac gain, V_{IN} and V_{BE}.

Questions

- For the common emitter amplifier circuit setup, what is the effect on the voltage gain, A, by increasing R_L?

You can find the answer at the StudentZone blog.

About the Author

Doug Mercer received his B.S.E.E. degree from Rensselaer Polytechnic Institute (RPI) in 1977. Since joining Analog Devices in 1977, he has contributed directly or indirectly to more than 30 data converter products and he holds 13 patents. He was appointed to the position of ADI Fellow in 1995. In 2009, he transitioned from full-time work and has continued consulting at ADI as a Fellow Emeritus contributing to the Active Learning Program. In 2016 he was named Engineer in Residence within the ECSE department at RPI. He can be reached at doug.mercer@analog.com.

About the Author

Antoniu Miclaus is a system applications engineer at Analog Devices, where he works on ADI academic programs, as well as embedded software for Circuits from the Lab®, QA automation, and process management. He started working at Analog Devices in February 2017 in Cluj-Napoca, Romania. He is currently an M.Sc. student in the software engineering master's program at Babes-Bolyai University and he has a B.Eng. in electronics and telecommunications from Technical University of Cluj-Napoca. He can be reached at antoniu.miclaus@analog.com.