

Product Datasheet

QSFP-100G-AOC3M-C

Cisco® Compatible 100GBASE-SR4 QSFP28 to QSFP28 Active Optical Cable, Active, 3m

FEATURES

- Compliant with 100GBASE-SR4 and CAUI-4 specification per IEEE 802.3bm
- Compliant to SFF-8665 (QSFP28 Solution) Revision 1.8
- Supports 100 Gbps data rate links up to 70m/100 m via OM3/OM4, respectively.
- VCSEL array transmitter and PIN array receiver
- Low power consumption of max 3.5W
- Hot pluggable electrical interface
- Using standard 12/8 lane optical fiber with 3-mm round cable
- 0 to 70°C case temperature operating range
- RoHS-6 Compliant (lead-free)

APPLICATIONS

- Ethernet for 100GBASE-SR4
- InfiniBand EDR, FDR, & QDR
- HPC Interconnects
- Proprietary Interconnections

DESCRIPTION

ATGBICS QSFP-100G-AOC3M-C QSFP28 active optical cables are high-performance active optical cable with bi-directional signal transmission and aggregate 100-Gbps bandwidth for both InfiniBand EDR and Ethernet 100G-SR4 applications. Compared to conventional copper cables, longer and lighter optical cables enable the ease of complicated data-center cabling. The AOCs utilize multimode fiber with 850-nm VCSELs and PIN PDs. The certificated cables have superior signal integrity and bit- error-rate, which enables reliable operation performance.

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Absolute Maximum Ratings

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

| Parameter | Min | Max | Unit | Note |
|--|------|-----|----------------------|------|
| Storage Temperature | 0 | 70 | °C | 1 |
| 3.3V Power Supply Voltage | -0.5 | 3.6 | V | |
| Data Input Voltage-Single Ended | -0.5 | | V _{cc} +0.5 | |
| Control Input Voltage | -0.5 | 3.6 | V | |
| Relative Humidity | 5 | 85 | % | 2 |

Note:

1. Limited by the fiber cable jacket, not the active ends
2. Non-condensing

Recommended Operating Conditions

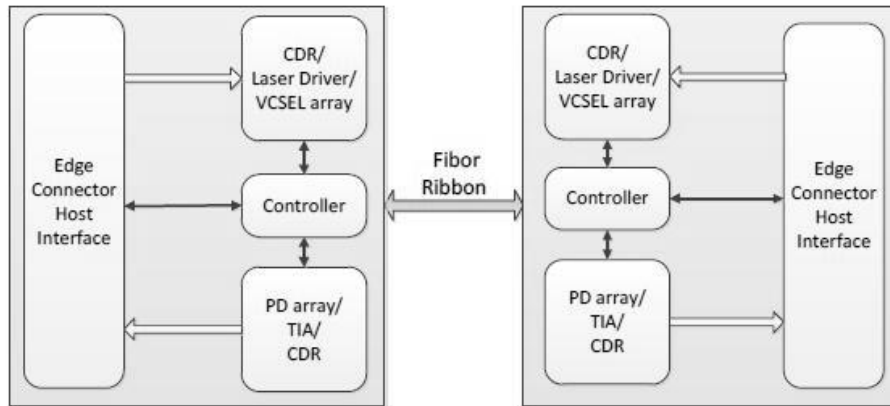
| Parameter | Min | Typical | Max | Unit | Note |
|---|-------|---------|----------------------|------|---------|
| Case Operating Temperature | 0 | | 70 | °C | |
| Power Supply Voltage | 3.135 | 3.3 | 3.465 | V | |
| Data Rate per Channel | | | 25.78125 | Gbps | |
| Bit Error Ratio (BER) | | 10-12 | | | 1, 2 |
| Control Input Voltage High | 2 | | V _{cc} +0.3 | V | |
| Control Input Voltage Low | -0.3 | | 0.8 | V | |
| Two Wire Serial (TWS) Interface Clock Rate | | | 400 | kHz | |
| Differential Data Input / Output Load | | 100 | | Ohms | +/- 10% |
| Standard Cable Lengths | | | 100 | m | 3 |

Note:

1. Bit-Error-Rate (BER) is tested with PRBS 2³¹-1 pattern
2. 100G QSFP28 AOC cable requires an electrical connector compliant with SFF-8662 or SFF-8672 which is used on the host board in order to guarantee its electrical interface specification.
3. Per 100GBASE-SR4 Standard, cable length supports up to 70m / 100m via OM3 / OM4, respectively. Different cable length within this range upon customization.

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Functional Description of Transceiver



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Electrical Specifications

| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|---|--------|------|-----------|------|------|------|
| Transceiver Electrical Characteristics | | | | | | |
| TRx Power Consumption | | | 2.5 | 3.5 | W | |
| TRx Power-on Initialization Time | | | | 2000 | ms | |
| CAUI-4 Module Electrical Input Characteristics (TP1) | | | | | | |
| Single Ended Input Voltage Tolerance | | -0.4 | | 3.3 | V | |
| Differential pk-pk input voltage tolerance | | 900 | | | mV | |
| Differential Input Return Loss | Sdd11 | | See Eq. 1 | | dB | 1 |
| Differential to Common-mode Input Return Loss | Sdc11 | | See Eq. 2 | | dB | 2 |
| DC common mode voltage | | -350 | | 2850 | mV | |

Notes:

$$1. \quad RL_d(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4 \log_{10} \left(\frac{f}{14} \right) & 8 \leq f < 19 \end{cases} \text{ (dB)} \quad \text{(Eq.1)}$$

where

f is the frequency in GHz

RL_d is the CAUI-4 Chip-to-module input differential return loss

$$2. \quad RL_{dc}(f) \geq \begin{cases} 22 - 20 \left(\frac{f}{25.78} \right) & 0.01 \leq f < 12.89 \\ 15 - 6 \left(\frac{f}{25.78} \right) & 12.89 \leq f < 19 \end{cases} \text{ (dB)} \quad \text{(Eq.2)}$$

where

f is the frequency in GHz

RL_{dc} is the CAUI-4 Chip-to-module input differential to common mode input return loss

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| Parameter | Symbol | Min | Typical | Max | Unit | Note |
|--|--------|------|-----------|------|------|------|
| CAUI-4 Module Electrical Output Characteristics (TP4) | | | | | | |
| AC Common-Mode Output Voltage (RMS) | | | | 17.5 | mV | |
| Differential Output Voltage | | | | 900 | mV | |
| Eye Width | | 0.57 | | | UI | |
| Eye Height, Differential | | 228 | | | mV | |
| Vertical Eye Closure | | | | 5.5 | dB | |
| Differential Output Return Loss | Sdd22 | | See Eq. 1 | | dB | 1 |
| Common to Differential Mode Conversion Return Loss | Scd22 | | See Eq. 2 | | dB | 2 |
| Transition Time (20% to 80%) | | 12 | | | ps | |
| DC Common Voltage | | -350 | | 2850 | mV | |

Notes:

$$1. \quad RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4 \log_{10} \left(\frac{f}{14} \right) & 8 \leq f < 19 \end{cases} \quad (\text{dB}) \quad (\text{Eq.1})$$

where

f is the frequency in GHz

RLd is the CAUI-4 Chip-to-module host output differential return loss

$$2. \quad RLdc(f) \geq \begin{cases} 22 - 20 \left(\frac{f}{25.78} \right) & 0.01 \leq f < 12.89 \\ 15 - 6 \left(\frac{f}{25.78} \right) & 12.89 \leq f < 19 \end{cases} \quad (\text{dB}) \quad (\text{Eq.2})$$

where

f is the frequency in GHz

$RLdc$ is the CAUI-4 Chip-to-module output common to differential mode conversion return loss

Optical Cable Specification

| Parameter | Specification | Notes |
|-------------------------------|-----------------------------------|-------|
| Minimum Cable Bending Radius | ~30 mm | |
| Cable Cross-Section Dimension | Round Cable with 3 mm in Diameter | |
| Cable Cover Type | LSZH | 1 |
| Standard Cable Length | 10, 20, 30, 50, 70, 100-m | 2 |
| Cable Length Tolerance | +100/-0 cm | |

Notes:

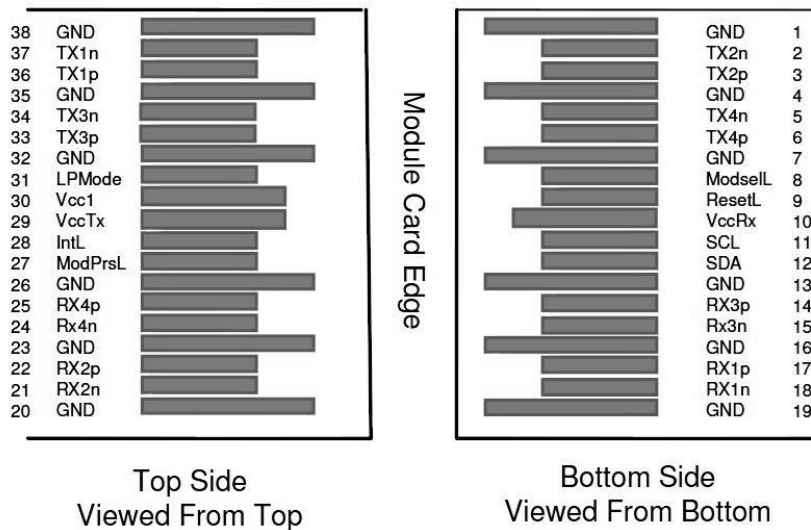
1. Cable cover type standard is LSZH. Other types can be available upon request.
2. Different cable length within this range upon customization.

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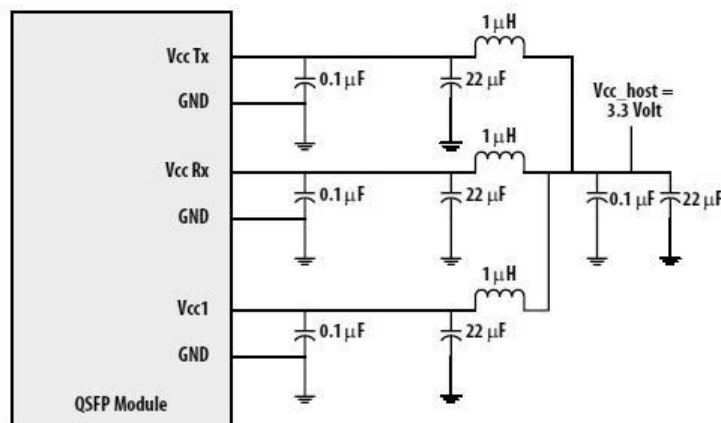
QSFP28 Module Pad Assignments and Descriptions

| Pin | Logic | Symbol | Description | Plug Sequence |
|-----|-------------|---------|-------------------------------------|---------------|
| 1 | | GND | Ground | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3 |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3 |
| 4 | | GND | Ground | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3 |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3 |
| 7 | | GND | Ground | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | 3 |
| 9 | LVTTL-I | ResetL | Module Reset | 3 |
| 10 | | Vcc Rx | +3.3V Power Supply Receiver | 2 |
| 11 | LVC MOS-I/O | SCL | 2-wire serial interface clock | 3 |
| 12 | LVC MOS-I/O | SDA | 2-wire serial interface data | 3 |
| 13 | | GND | Ground | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3 |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3 |
| 16 | | GND | Ground | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3 |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3 |
| 19 | | GND | Ground | 1 |
| 20 | | GND | Ground | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3 |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3 |
| 23 | | GND | Ground | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3 |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3 |
| 26 | | GND | Ground | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3 |
| 28 | LVTTL-O | IntL | Interrupt | 3 |
| 29 | | Vcc Tx | +3.3V Power supply transmitter | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2 |
| 31 | LVTTL-I | LPMODE | Low Power Mode | 3 |
| 32 | | GND | Ground | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3 |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3 |
| 35 | | GND | Ground | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3 |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3 |
| 38 | | GND | Ground | 1 |

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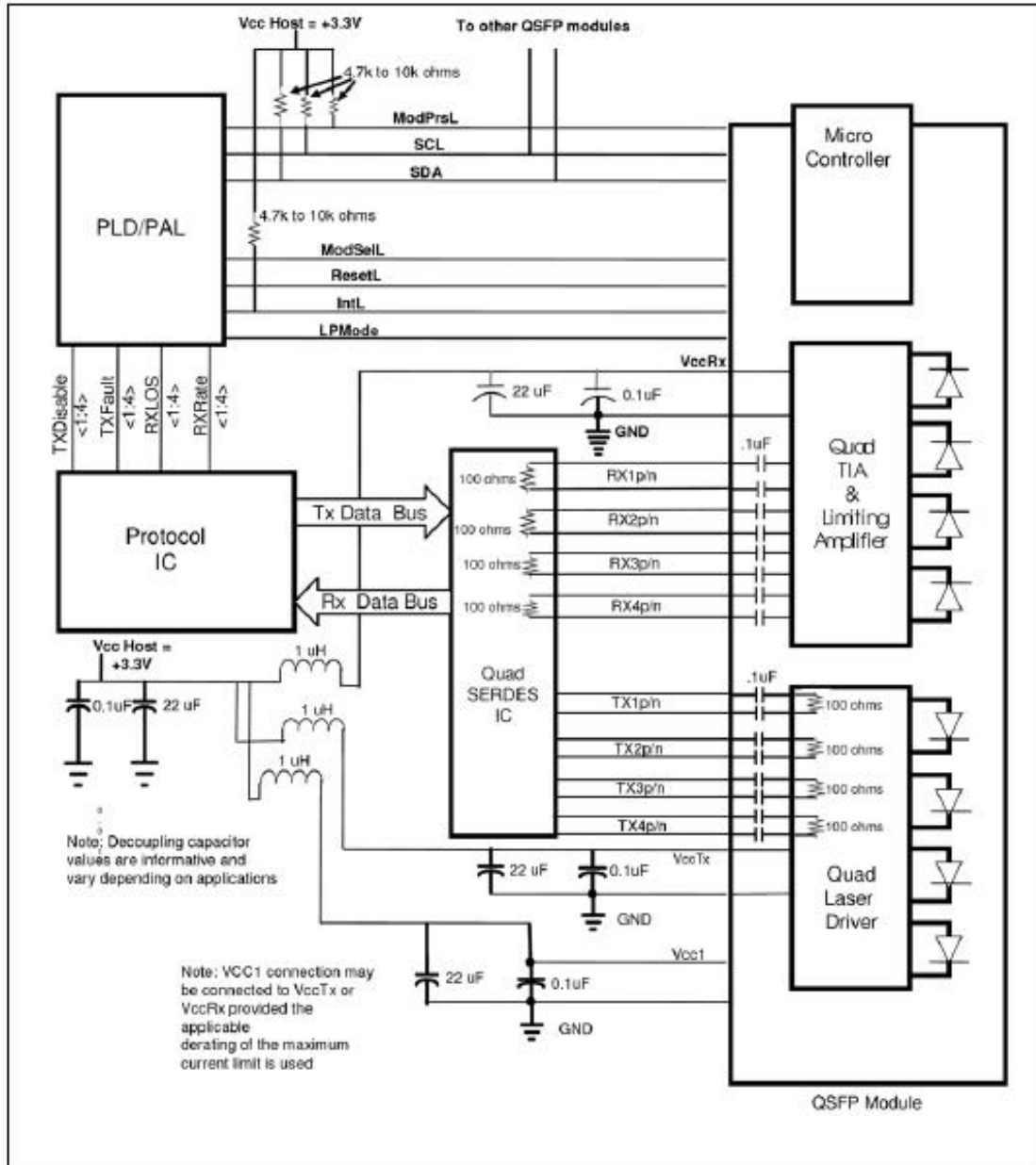


RECOMMENDED HOST BOARD POWER SUPPLY CIRCUIT



RECOMMENDED INTERFACE CIRCUIT

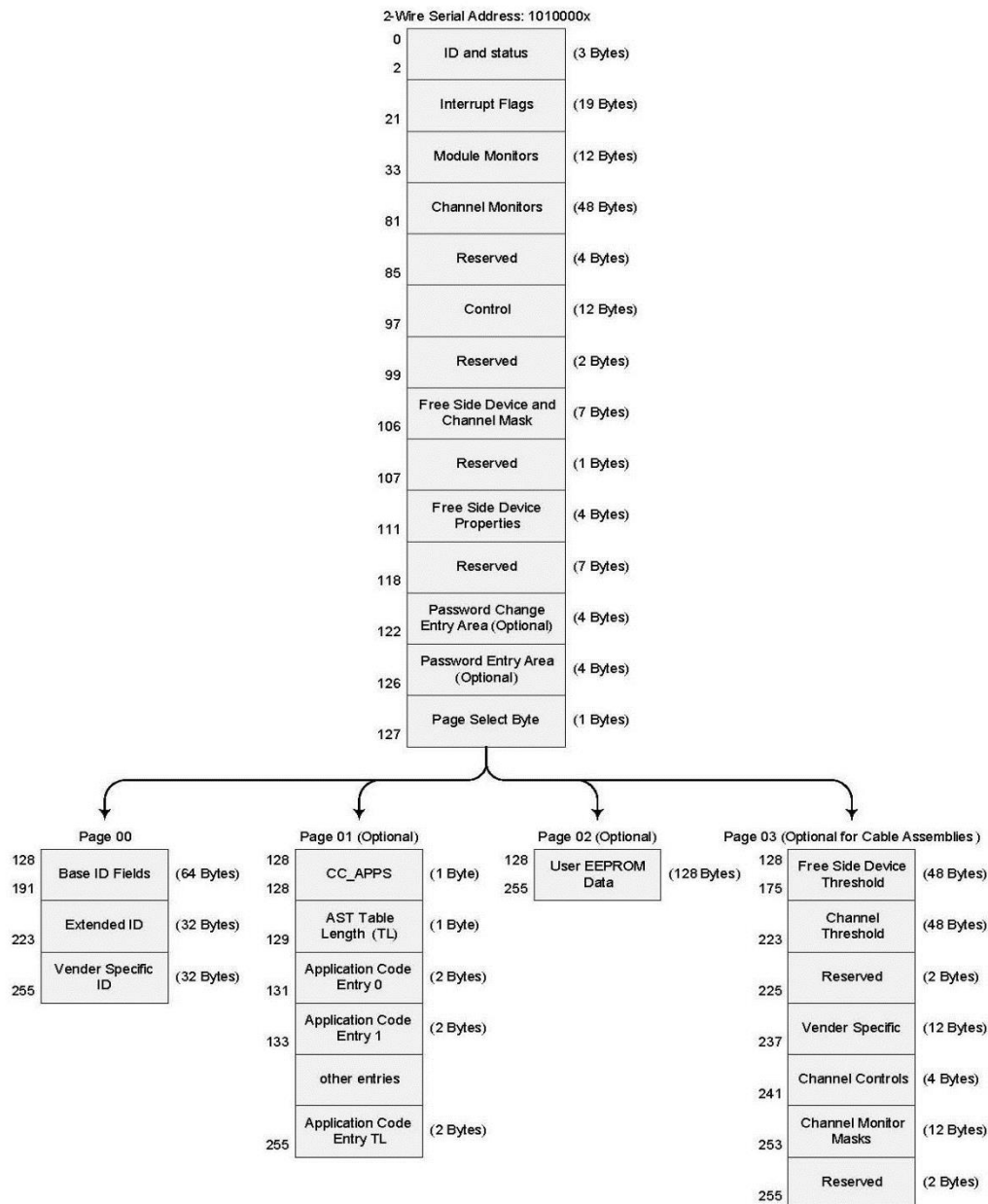
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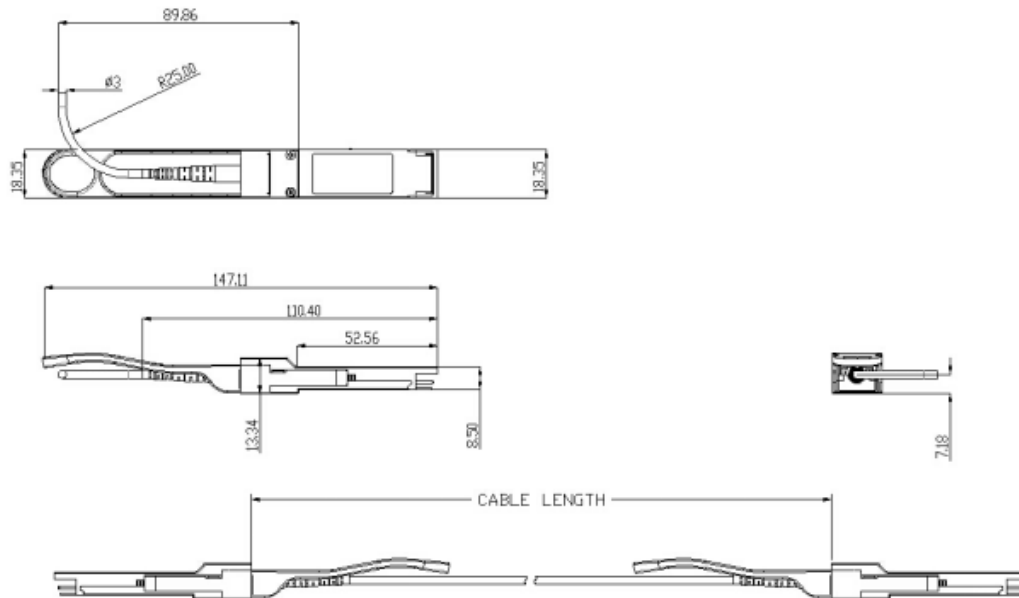
Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP28 SFF-8636 MSA specification as shown in the below. For a more detailed description of this memory map or lower pages, please see our memory map document with flexible customization settings.



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MECHANICAL DIMENSIONS



Ordering Information

| Length | Note |
|--------|-----------------|
| 3m | OM3 Round Cable |
| 5m | OM3 Round Cable |
| 10m | OM3 Round Cable |
| 20m | OM3 Round Cable |
| 30m | OM3 Round Cable |
| 50m | OM3 Round Cable |
| 70m | OM3 Round Cable |
| 100m | OM4 Round Cable |