Application Report
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How to use the LMK05318 as a jitter cleaner

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ABSTRACT

This application report outlines the advantages of using ultra-high performance clock synchronizers from Texas Instruments to generate reference clocks with ultra-low noise that is irrespective of the input jitter and exceeds the needs for communications and industrial applications. The application report explains two methods on how to clean input jitter with the LMK05318 are described with performance data.

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Trademarks

1 Introduction

TI's LMK05318 device is an ultra-high performance clock generator, jitter cleaner, and clock synchronizer with advanced reference clock selection and hitless switching feature to meet the stringent requirements of telecom and industrial applications. The device features a single channel synchronizer or digital PLL (DPLL) that can synchronize to one of two differential or single-ended reference clock inputs. The synchronizer is accompanied by an analog PLL (APLL) domain that features TI's proprietary Bulk Acoustic Wave (BAW) resonator as a VCO and generates 50-fs, rms jitter. There is an additional APLL domain that can be used to generate unrelated frequencies either locked to the reference clock input or the free-run XO input and generates 120-fs, rms jitter. The LMK05318 can generate up to eight high performance output clocks with up to six different frequencies. Apart from usage as a clock synchronizer in telecom applications, the LMK05318 can also be used a jitter cleaner in any application where single or multiple frequencies with low jitter needs to be generated from a dirty system clock. Utilizing the ability to set low loop bandwidth either on the DPLL or the APLL with BAW VCO, the LMK05318 offers the ability to clean reference clock jitter while simplifying the overall PCB design by relying on standard off-the-shelf inexpensive components around the device. The key features of the LMK05318 include:

- Single channel DPLL supporting programmable loop bandwidths in the range of 1 mHz to 4 kHz. When used with a TCXO or OCXO and less than 10-Hz loop bandwidth, wander filtering of a noisy reference input is supported. When used with any standard off-the-shelf XO and between 10-Hz and 100-Hz loop bandwidth, jitter filtering of a noisy reference input is supported.
- APLL1 with TI's proprietary BAW VCO technology generating ultra-low 50-fs RMS jitter and is independent of the jitter and frequency of both the reference clock and the XO clock. APLL1 also supports low loop bandwidths down to 100 Hz and can support cleaning high frequency noise present in a system clock that applied to the XO input pins. This use case can be employed while the front-end DPLL is powered down.
- APLL2 with conventional LC VCO generating low 120-fs RMS jitter that can either operate in free-run mode and locked to the XO clock or operate in DPLL mode and locked to the reference input.
- Industry leading phase transient (hitless switching) of ±50 ps using phase cancellation.
- Robust operation with PSRR of better than –80 dBc in the presence of supply noise of 50-mV ripple. This superior PSRR on all supply pins allows the LMK05318 to operate from a DC-DC converter and still generate ultra-low jitter performance.
- On-chip EEPROM, with re-writes up to 100 times, enables no in-system programming after power up.
- High level of programmability with multiple device monitoring options that can be read through I2C/SPI or by polling STATUS pins.
- Programmable output clock signal format: AC-LVPECL, AC-LVDS, AC-CML, HCSL, and LVCMOS

1.1 Bulk Acoustic Wave (BAW) Resonator

BAW resonator is a thin film resonator and is similar to a traditional quartz crystal. As shown in Figure 1, a piezoelectric film is sandwiched between two metal films and several other layers to confine mechanical energy. This structure traps the acoustic energy while creating a resonator element with very low loss and a high-quality factor. Historically, BAW resonators have been used for RF filters on the front-end of wireless transceivers in mobile devices. The LMK05318 is the industry's first commercial product using the BAW resonator as a low noise Voltage Controlled BAW Oscillator (VCBO) and integrated in a standard QFN package to generate ultra-low noise clocks.

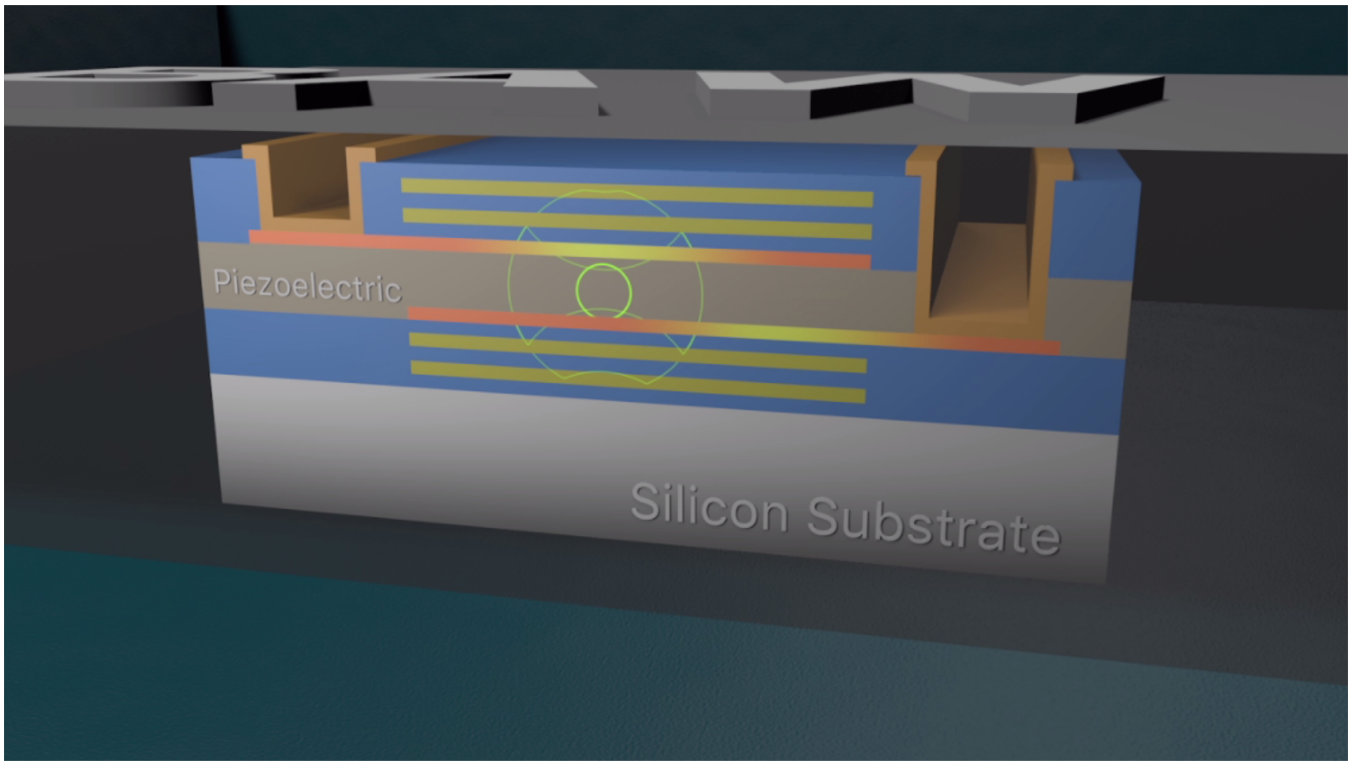

Figure 1. Basic Structure of a Bulk Acoustic Wave (BAW) Resonator

Table 1 outlines the key differences between BAW resonator, Surface Acoustic Wave (SAW) resonator, and LC tank resonators.

Table 1. BAW vs SAW vs LC

Technology	Strengths	Weaknesses
BAW	• High quality factor (approximately 1000 at 2.5 GHz) supports ultra-low jitter • High resonant frequency (2 – 3 GHz) supports divide down to achieve multiple clock frequencies (for example a 2.5-GHz BAW can be divided down to generate 156.25-MHz, 125-MHz and 100-MHz clocks) • Superior RMS jitter that has no impact from external sources and easy to design with – < 60 fs RMS (12 kHz – 20 MHz) at 156.25 MHz – < 30 fs RMS (12 kHz – 20 MHz) at 1.25 GHz – System-in-package provides standard QFN packages that are cost effective and easy to design around	• Narrow tuning range • Additional PLL with LC VCO can mitigate the effect
SAW		• Exotic substrate → not easy to integrate • Lower frequency (< 1 GHz)
LC	• Monolithic integration • Low cost	• Low-quality factor (approximately 20 at 1 GHz) results in worse jitter and phase noise and highly dependent on external sources

Figure 2 shows the phase noise performance of VCBO and couple of competitive LC VCOs at a carrier frequency of 625 MHz. As shown, the phase noise of VCBO at 10-kHz offset is 25 dB better than a best-in-class LC VCO.

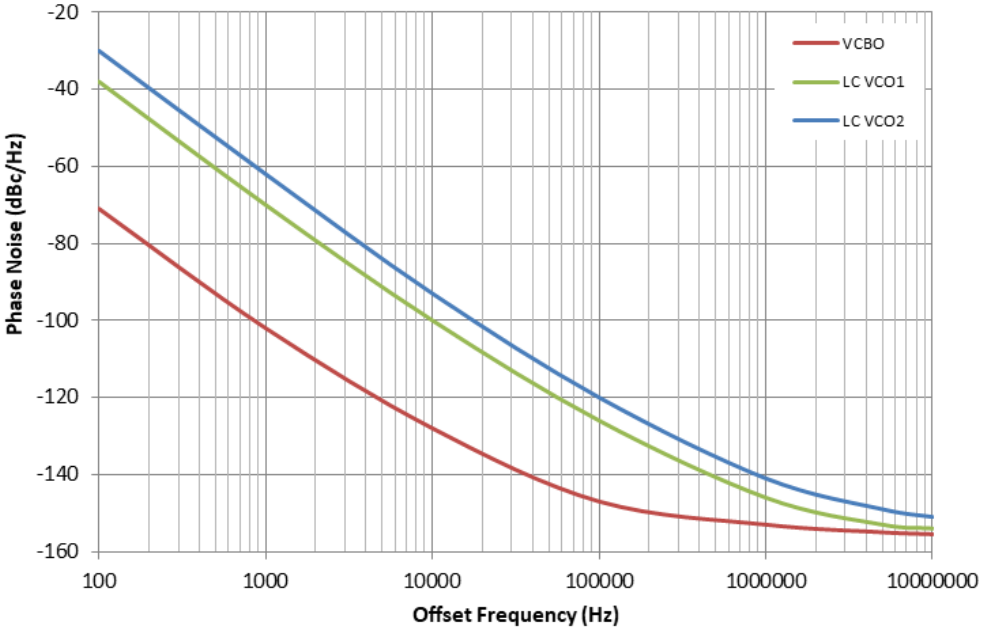

Figure 2. VCBO vs LC VCO Phase Noise

2 LMK05318 as a Jitter Cleaner

The LMK05318 can act as a jitter cleaner in either of the following configurations:

- The DPLL with a loop bandwidth of less than 10 Hz can be used to clean wander on the reference input clock when used with a TCXO or OCXO as reference to the APLLs. With a loop bandwidth of greater than 10 Hz, the reference input clock jitter can be cleaned with an XO as reference to the APLLs. The advantage of this configuration is the ability to clean excessive wander or low-frequency noise present on the reference input clock. In addition, if there is a phase noise requirement for the low offset frequencies, this mode of jitter cleaning with the DPLL provides lowest possible in-band phase noise. In this mode, APLL2 can also be utilized to generate free-run clocks with low jitter or can be locked to the divided clock from APLL1 to generate a second frequency domain with low jitter as per the application needs. Figure 3 shows the phase noise plot for a 156.25-MHz output from the LMK05318 that is locked to a dirty reference input clock of 25 MHz with a DPLL loop bandwidth of 10 Hz and TCXO frequency of 19.2 MHz.

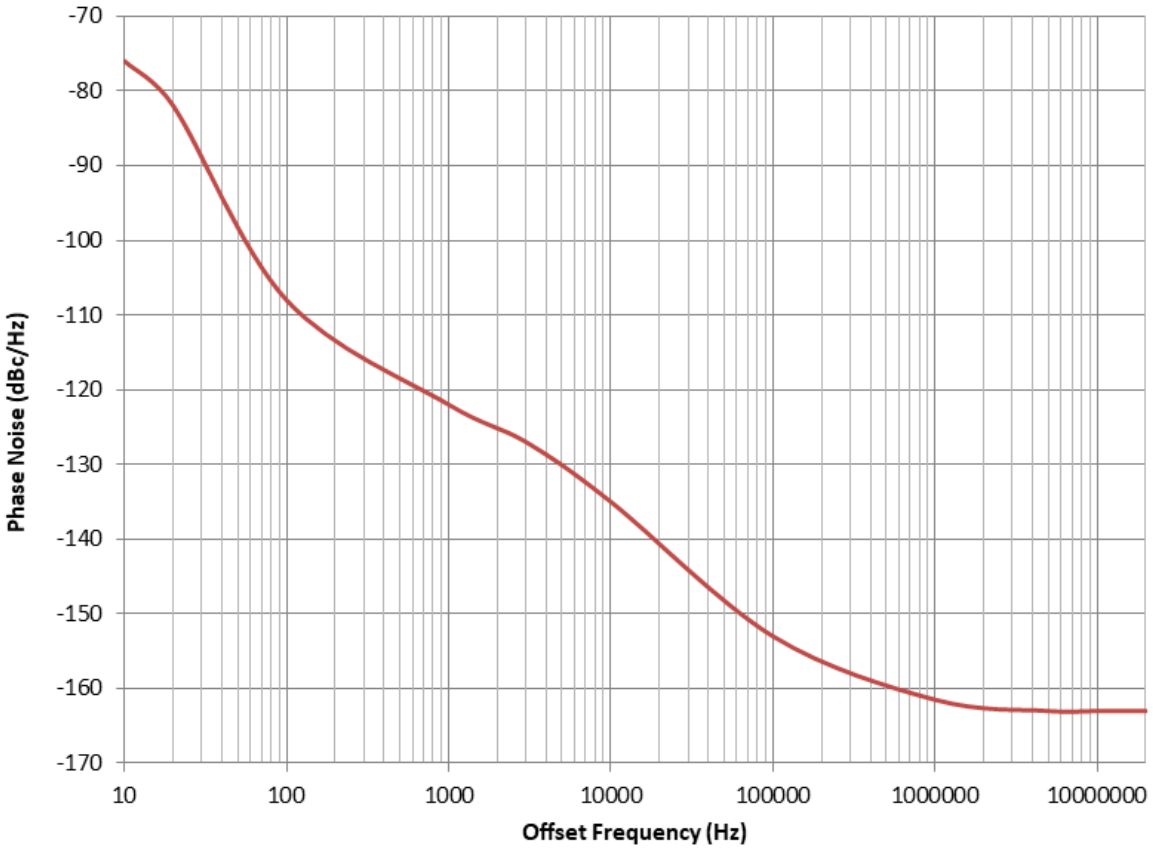

Figure 3. 156.25-MHz Output Phase Noise From LMK05318 With DPLL BW of 10 Hz, TCXO of 19.2 MHz and Reference Input of 25 MHz

- With the DPLL powered down, APLL1 with a loop bandwidth in the range of 100 Hz to 1 kHz can be used to clean high-frequency noise on the reference input clock. In this mode, APLL2 is recommended to be locked to the divided clock from APLL1 to generate a second frequency domain with low jitter as per the application needs. The advantage of this configuration is the ability of the LMK05318 to clean high-frequency noise without needing any external XO and when there is no explicit phase noise requirement for the close-in offset frequencies. This configuration enables a cost effective solution that also occupies smallest overall area and improved reliability, due to not needing any crystal based component, compared to other competing jitter cleaners. Figure 4 shows the phase noise plot for a 156.25-MHz output from the LMK05318 that is locked to a dirty reference input clock of 25 MHz with APLL1 loop bandwidth of 100 Hz (red line) and APLL1 loop bandwidth of 1 kHz (green line).

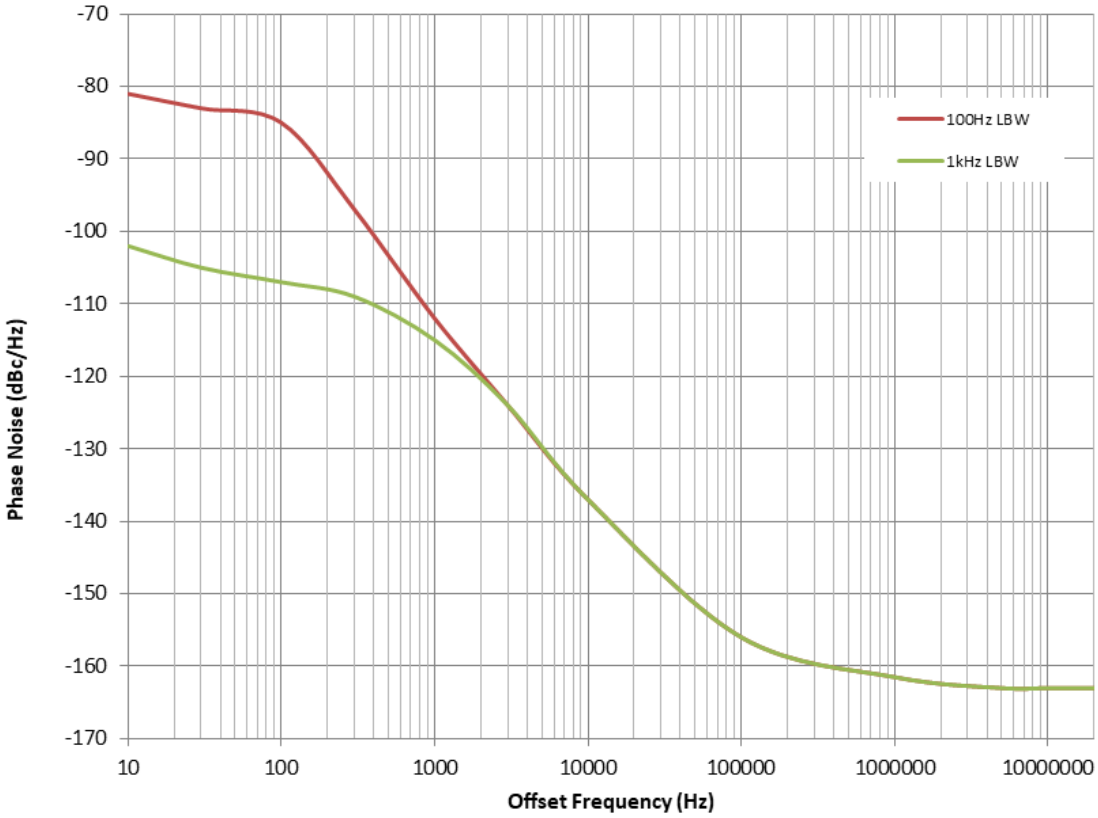

Figure 4. 156.25-MHz Output Phase Noise From LMK05318 With APLL1 BW of 100 Hz (Red Line) and APLL1 BW of 1 kHz (Green Line) and Reference Input of 25 MHz

3 Summary

Ultra-high performance clock synchronizers from TI, like the LMK05318, can outperform competing solutions, which suffer from various drawbacks that include prolonging the overall design cycle and increase overall system cost. The jitter cleaning ability of the LMK05318 in both supported modes simplify the overall system development, including design, prototyping and standards compliance. TI also offers WEBENCH Clock Architect Tool that helps the hardware engineers to select the appropriate settings for the LMK05318 that meet their requirements.

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