−2 V to 70 V Wide Input Voltage Range, 2.2 MHz High Bandwidth, Current-Sense Amplifier with PWM Rejection

FEATURES

- 2.2 MHz small signal, −3 dB bandwidth
- In-package Trim Core (DigiTrim™)
  - Precision without chopping and/or autozero
  - Typical ±0.21 µV/°C offset drift
  - Maximum ±200 µV voltage-offset over temperature range
  - Typical DC CMRR: 142 dB
  - Typical AC CMRR at 50 kHz: 96 dB
- Wide common-mode input voltage range
  - −2 V to +70 V, continuous operation
  - −20 V to +85 V, continuous survival
- Initial gain: 20 V/V
- Wide operating temperature range: −40°C to +125°C
- Bidirectional operation
- 2.9 V to 5.5 V power-supply operating range
- Available in 8-lead, SOIC_N package
- AEC-Q100 Automotive Qualified

APPLICATIONS

- In-phase or High-side current sensing in
  - Motor control in BLDC motors, Low-inductance motors
  - Bidirectional 48 V to 12 V DC-DC converters
  - Solenoid controls
  - Power rail monitoring
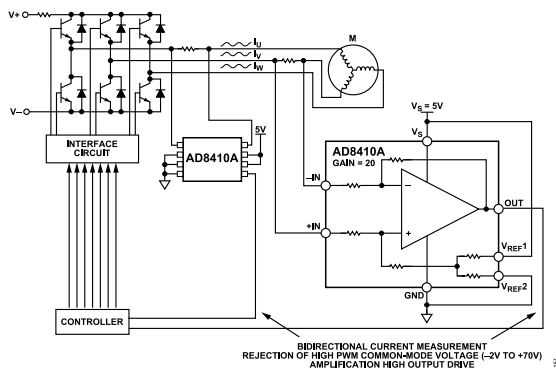- Low-side current sensing

TYPICAL APPLICATION CIRCUIT

Figure 1. AD8410A in BLDC Motor Control Application

GENERAL DESCRIPTION

The AD8410A[1] is a high voltage, high bandwidth current-sense amplifier. The device features an initial gain of 20 V/V, with a 2.2 MHz bandwidth with a maximum ±0.13% gain error over the entire temperature range. The buffered output voltage directly interfaces with any typical converter. The AD8410A has a minimum DC common-mode rejection ratio (CMRR) of 123 dB from −2 V to +70 V. The AD8410A performs bidirectional current measurements across a shunt resistor in a variety of industrial and automotive applications.

The AD8410A offers breakthrough performance throughout the −40°C to +125°C temperature range. The device features an in-package trim core, which leads to a typical offset drift of ±0.21 µV/°C (based on Box Method, see Figure 53) throughout the operating temperature range and the common-mode voltage range without the need for chopping and autozero clocks (which could lead to intermodulation in the application). The device includes circuitry to achieve a wide input common-mode range and balanced input bias currents, regardless of input differential voltage or common-mode voltage, and circuitry to achieve ultra-low CMRR drift. The device also includes circuitry to enable output accuracy in the presence of pulse-width modulation (PWM) type input common-mode voltages. The AD8410A is offered in 8-lead, SOIC_N.
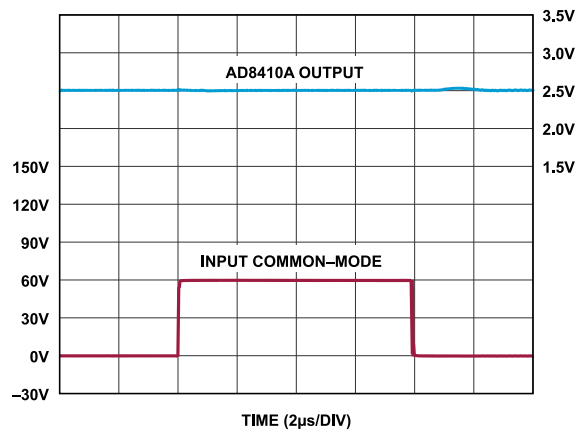

Figure 2. Input Common-Mode Step Response (0 V to 60 V), V_S = 5 V, Inputs Shorted

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[1] Protected by U.S. patent numbers 10,312,865 and 10,587,228.

Rev. 0

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REVISION HISTORY

2/2023—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

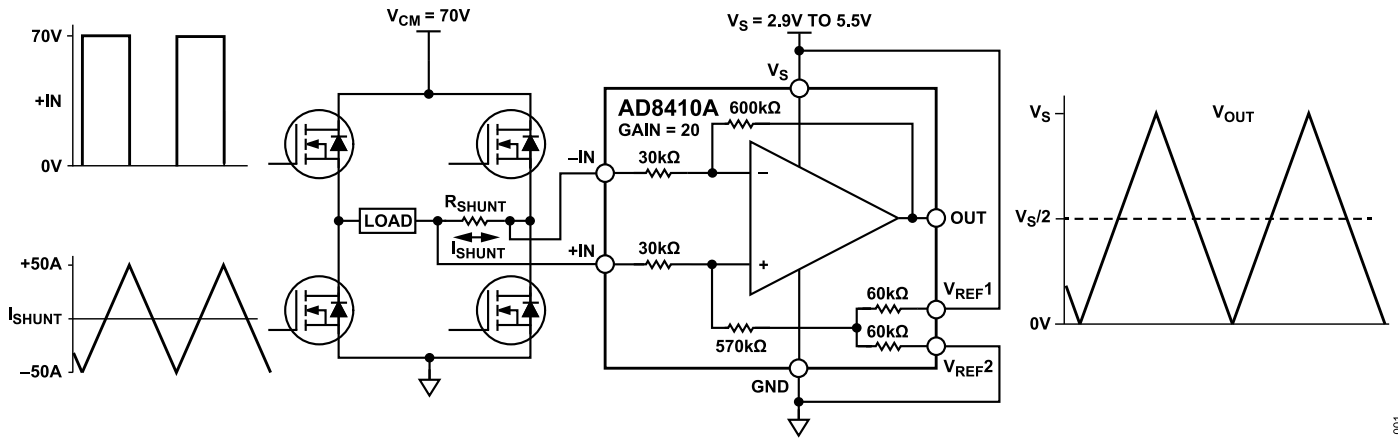*Figure 3. Functional Block Diagram*

SPECIFICATIONS

T_A = −40°C to +125°C (operating temperature range), supply voltage (V_S) = 5 V, ground (GND) = 0 V, Input Common-Mode Voltage (VCM) = -IN, +IN =12 V, and $V_{REF}1$ = $V_{REF}2$ = 2.5 V, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN					
Initial			20		V/V
Error Over Temperature	Specified temperature range			0.13	%
Gain vs. Temperature				±6	ppm/°C
VOLTAGE-OFFSET	Referred to input (RTI)				
Over Temperature	Specified temperature range[1]			±200	μV
Offset Drift	Box method (see Figure 53)		±0.21	±0.71	μV/°C
	Bowtie method (-40°C to 25°C) (see Figure 54)			±1.84	μV/°C
	Bowtie method (25°C to 125°C) (see Figure 54)			±1.51	μV/°C
INPUT					
Total Input-Bias Current[2]	+IN = −IN = 0 V, V_S = $V_{REF}1$ = 5 V, $V_{REF}2$ = 0 V	−10.0			μA
	+IN = −IN = 12 V, V_S = $V_{REF}1$ = $V_{REF}2$ = 0 V, T_A = 25°C		44		μA
	+IN = −IN = 12 V, V_S = $V_{REF}1$ = 5 V, $V_{REF}2$ = 0 V			175	μA
	+IN = −IN = 48 V, V_S = $V_{REF}1$ = $V_{REF}2$ = 0 V, T_A = 25°C		178		μA
	+IN = −IN = 48 V, V_S = $V_{REF}1$ = 5 V, $V_{REF}2$ = 0 V			484	μA
Input Offset Current	+IN = −IN = 0 V			1.0	μA
	+IN = −IN = 12 V			2.5	μA
	+IN = −IN = 48 V			2.7	μA
Input Voltage Range	Common mode, continuous	−2		+70	V
Common-Mode Rejection Ratio (CMRR)	Specified temperature range, DC, V_{CM} = −2 V to +70 V	123	142		dB
	T_A = 25°C, frequency = 10 kHz		110		dB
	T_A = 25°C, frequency = 50 kHz		96		dB
OUTPUT					
Voltage Swing to GND	Load resistance (R_L) = 10 kΩ			GND+0.005	V
Voltage Swing to V_S	Load resistance (R_L) = 10 kΩ			V_S − 0.016	V
Output Resistance	T_A = 25°C		0.2		Ω
Maximum Capacitive-Load	No continuous oscillation, T_A = 25°C		4.7		nF
DYNAMIC RESPONSE					
Small Signal, −3 dB Bandwidth	T_A = 25°C		2.2		MHz
Slew Rate	T_A = 25°C		10		V/μs
NOISE					
0.1 Hz to 10 Hz (RTI)	T_A = 25°C		8		μV p-p
Spectral Density, 1 kHz (RTI)	T_A = 25°C		47		nV/√Hz
Spectral Density, 10 kHz (RTI)	T_A = 25°C		38		nV/√Hz
OFFSET ADJUSTMENT					
Ratiometric Accuracy[3]	V_{REF} pins divider to supply	0.499		0.501	V/V
Accuracy, Referred to the Output (RTO)	V_{REF} error when using an external reference of 2.5 V applied to $V_{REF}1$ and $V_{REF}2$ in parallel			±1	mV/V
$V_{REF}1,2$ Input Voltage Range		GND		V_S	V
$V_{REF}1,2$ Divider Resistor Values			60		kΩ
POWER SUPPLY					
Operating Voltage Range		2.9		5.5	V
Quiescent Current	Output voltage (V_{OUT}) = 2.5 V DC, T_A = 25°C		7.8		mA
	V_{OUT} = 2.5 V DC			10.8	mA
Power Supply Rejection Ratio (PSRR)	V_S from 3 V to 5 V, Specified temperature range	84	120		dB

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE RANGE					
For Specified Performance	Operating temperature range	−40		+125	°C

[1] Guaranteed by test and characterization

[2] To see input bias current per pin, see Figure 13 and Figure 14.

[3] The offset adjustment is ratiometric to the power supply when $V_{REF}1$ and $V_{REF}2$ are used as dividers between the supplies.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_S to GND)	6 V
Input Voltage Range, Continuous	
Common-Mode	
+IN to GND	−20 V to +85 V
−IN to GND	−20 V to +85 V
Differential	
+IN to −IN	± 20 V
$V_{REF}1$, $V_{REF}2$	GND − 0.3 V to V_S + 0.3 V
Reverse Supply Voltage	0.3 V
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Output Short-Circuit Duration	Indefinite

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JB} is the junction-to-board thermal resistance. θ_{JCT} is the junction-to-case thermal resistance.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JB}	θ_{JCT}	Unit
R-8	142.8	140.6	64.1	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board for θ_{JA}, JEDEC 2S2P thermal impedance with ring style cold plate attached to PCB for θ_{JB}, and a JEDEC 1S0P thermal test board for θ_{JCT}. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field-induced robotic charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD8410A
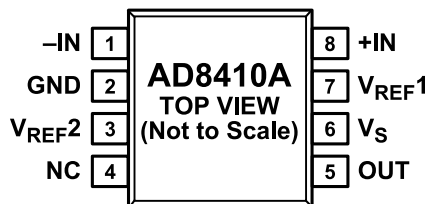
Table 4. AD8410A, 8-Lead SOIC_N

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±750	C2B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

```
         ┌─────────────────────┐
 −IN  │1│  AD8410A        │8│  +IN
 GND  │2│  TOP VIEW       │7│  V_REF1
V_REF2│3│ (Not to Scale)  │6│  V_S
  NC  │4│                 │5│  OUT
         └─────────────────────┘
```

NOTES
1. NC = NO CONNECT. THIS PIN IS
   CONNECTED INTERNALLY TO THE DIE. IT
   CAN BE LEFT FLOATING OR TIED TO GND.

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	−IN	Negative Input.
2	GND	Ground.
3	$V_{REF}2$	Reference Input 2.
4	NC	No Connect. This pin is connected internally to the die. It can be left floating or tied to GND.
5	OUT	Output.
6	V_S	Supply Voltage.
7	$V_{REF}1$	Reference Input 1.
8	+IN	Positive Input.

TYPICAL PERFORMANCE CHARACTERISTICS
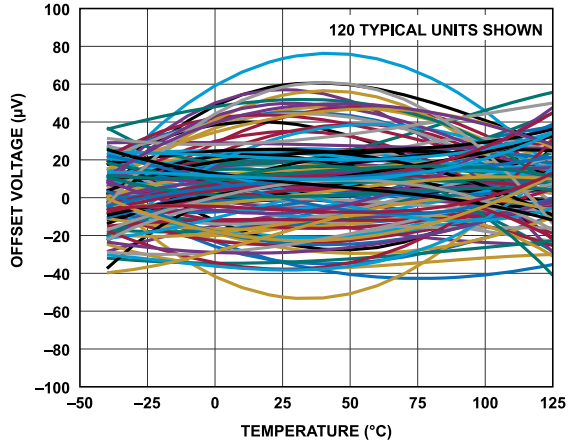
Figure 5. Offset Voltage vs. Temperature
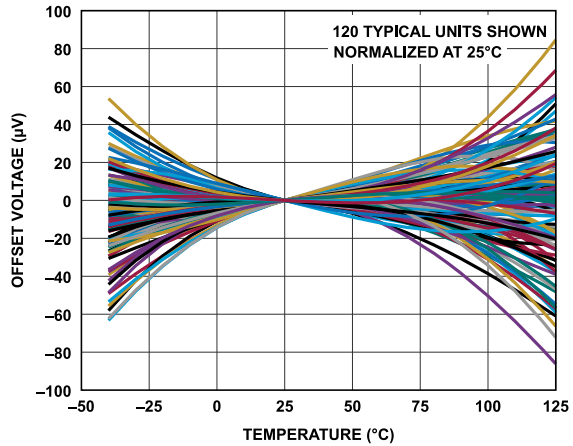
Figure 6. Offset Voltage vs. Temperature, Normalized at 25°C
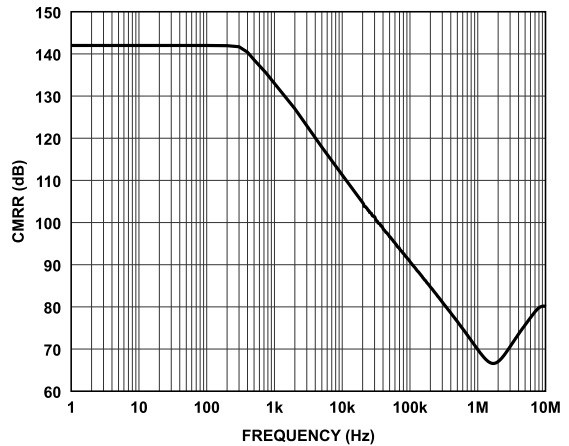
Figure 7. CMRR vs. Frequency
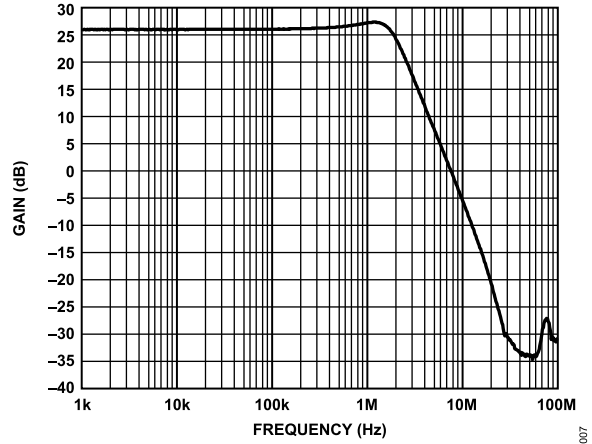
Figure 8. Typical Small Signal Bandwidth, V_{OUT} = 200 mV p-p
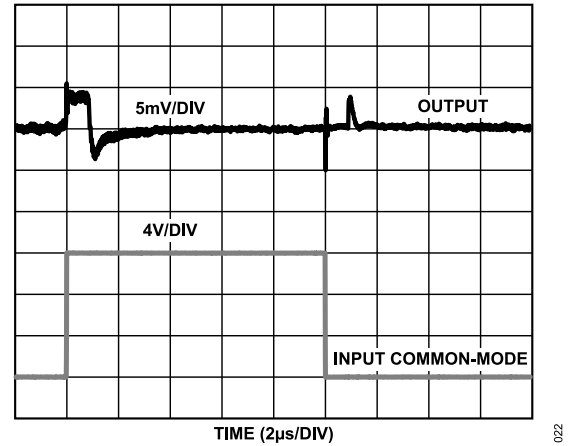
Figure 9. Input Common-Mode Step Response (0 V to 12 V), V_S = 5 V, Inputs Shorted
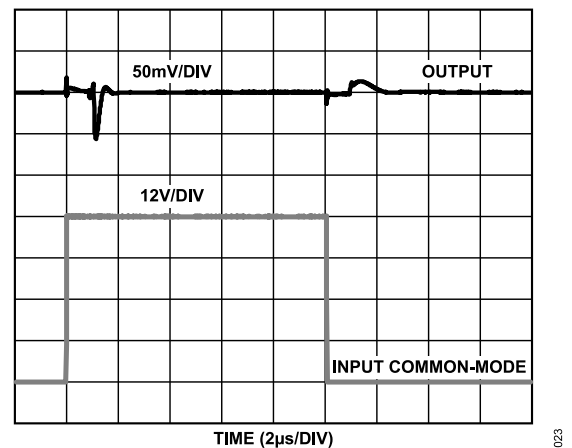
Figure 10. Input Common-Mode Step Response (0 V to 48 V), V_S = 5 V, Inputs Shorted

TYPICAL PERFORMANCE CHARACTERISTICS
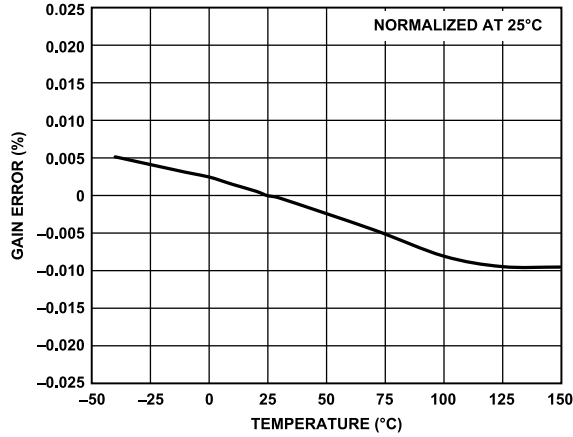
Figure 11. Gain Error vs. Temperature

Figure 12. Total Output Error vs. Differential Input Voltage

Figure 13. Bias Current Per Input Pin vs. V_{CM}, V_S = 5 V

Figure 14. Bias Current Per Input Pin vs. V_{CM}, V_S = 0 V, R_L = 10 kΩ

Figure 15. Input Offset Current vs. V_{CM} at Various Temperatures
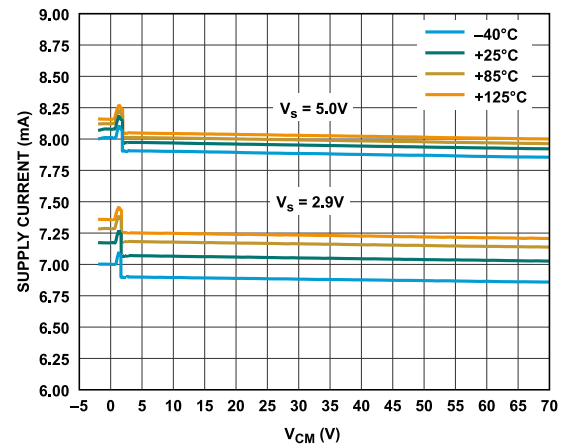
Figure 16. Supply Current vs. Input V_{CM} at Various Temperatures and Supply Voltages

TYPICAL PERFORMANCE CHARACTERISTICS
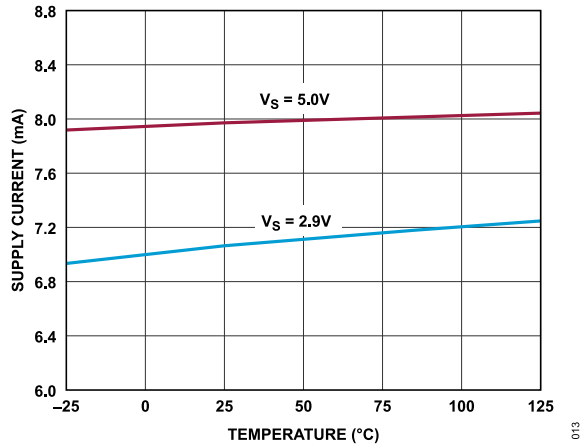
Figure 17. Supply Current vs. Temperature at Various Supply Voltages
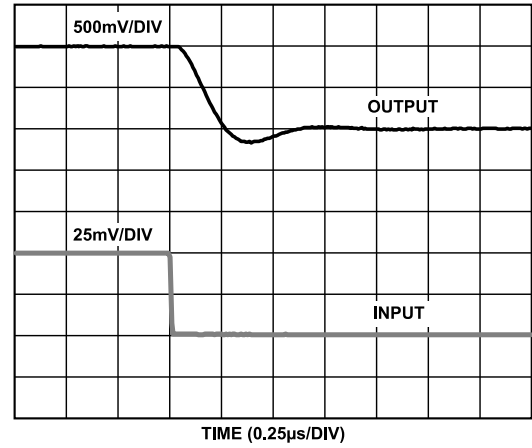
Figure 20. Fall Time, V_S = 2.9 V
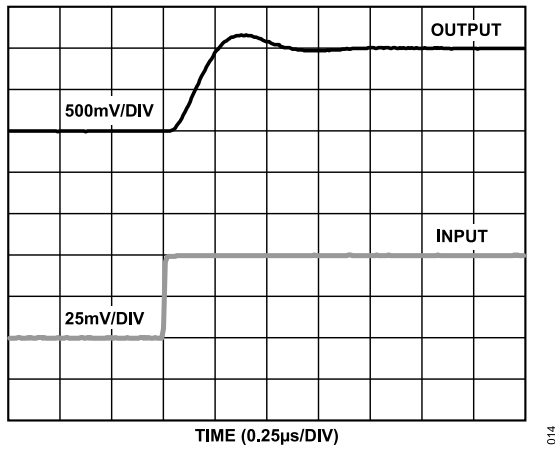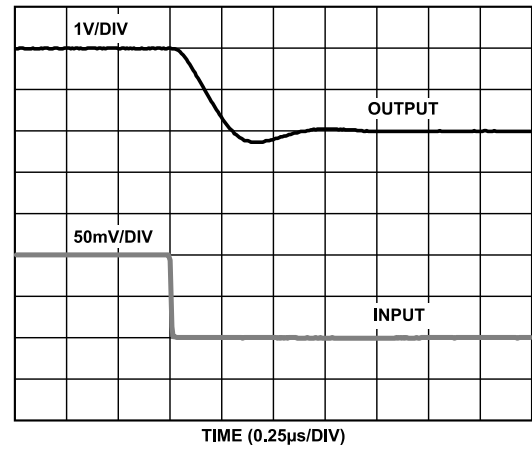

Figure 18. Rise Time, V_S = 2.9 V

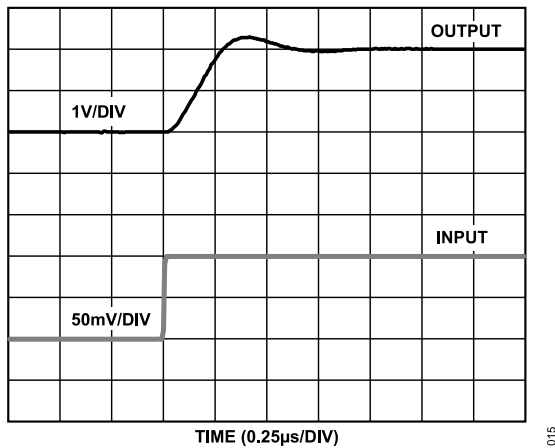*Figure 21. Fall Time, V_S = 5 V*
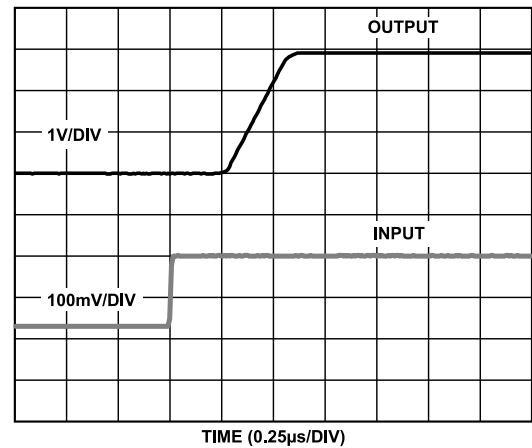

Figure 19. Rise Time, V_S = 5 V

Figure 22. Differential Overload Recovery, Rising, V_S = 2.9 V

TYPICAL PERFORMANCE CHARACTERISTICS
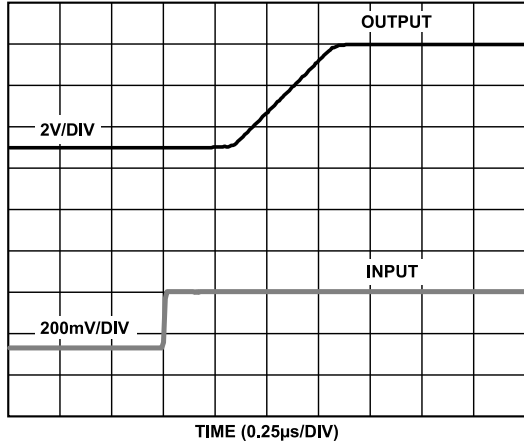

Figure 23. Differential Overload Recovery, Rising, V_S = 5 V
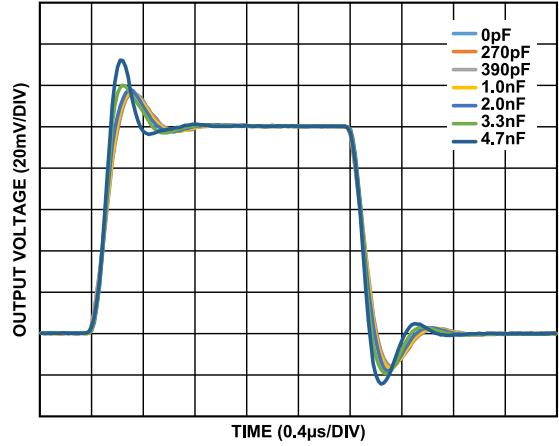

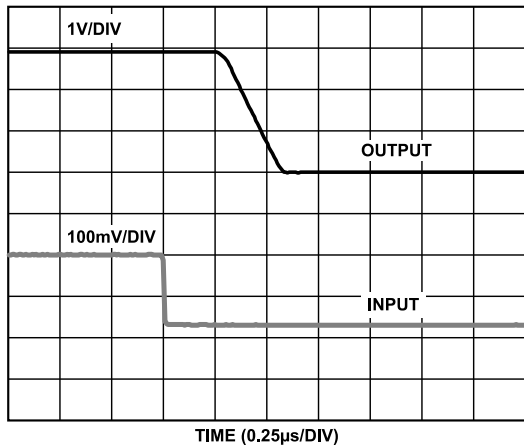Figure 26. Small Signal Response for Various Capacitive Loads

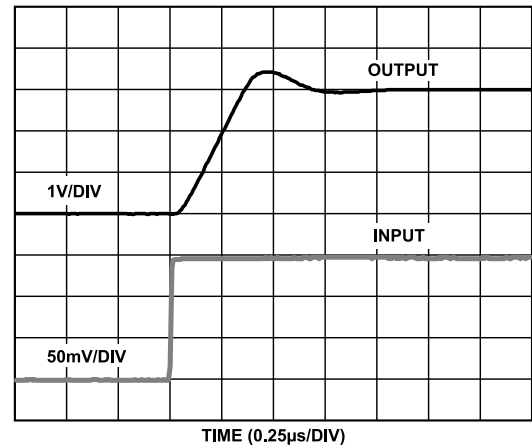Figure 24. Differential Overload Recovery, Falling, V_S = 2.9 V
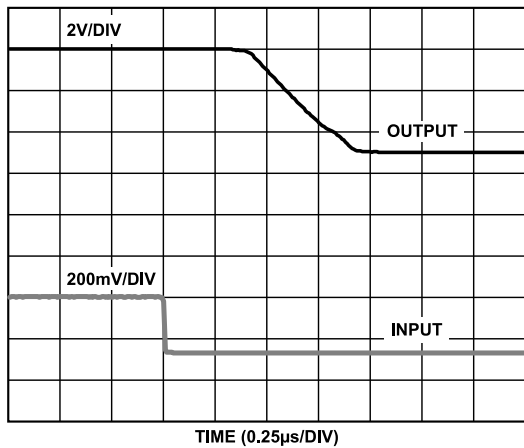

Figure 27. Large Signal Response, Rising, V_S = 5 V

Figure 25. Differential Overload Recovery, Falling, V_S = 5 V
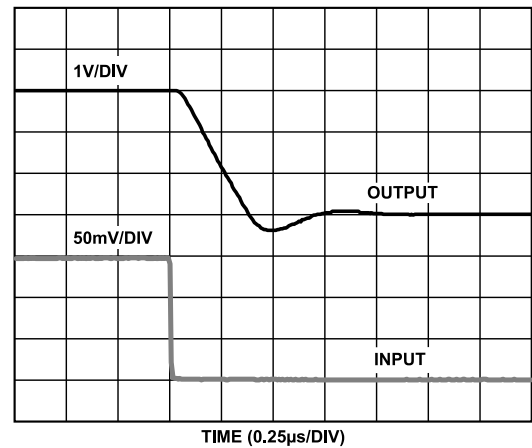
Figure 28. Large Signal Response, Falling, V_S = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 29. Maximum Output Sink Current vs. Temperature at Various Supply Voltages

Figure 30. Maximum Output Source Current vs. Temperature at Various Supply Voltages

Figure 31. Output Voltage Range from Positive Rail vs. Output Source Current

Figure 32. Output Voltage Range from Ground vs. Output Sink Current

Figure 33. Start-Up Response
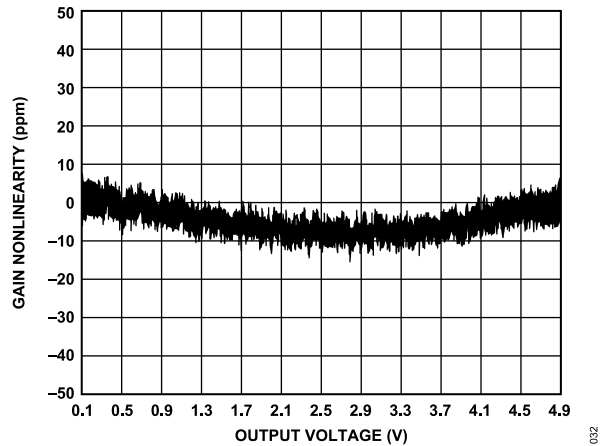
Figure 34. Gain Nonlinearity vs. Output Voltage, V_S = 5 V

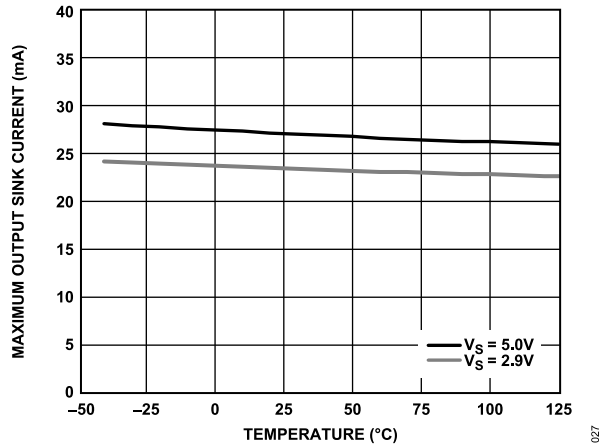## TYPICAL PERFORMANCE CHARACTERISTICS
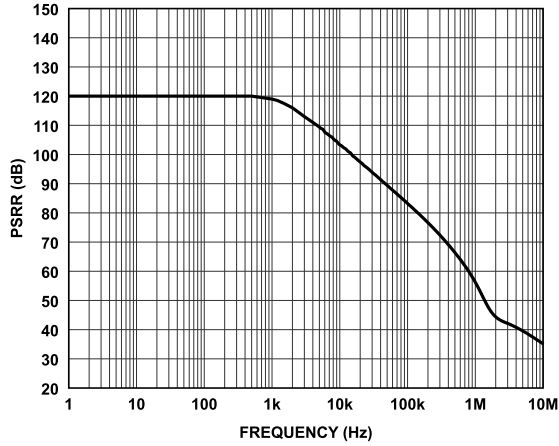
Figure 35. PSRR vs. Frequency
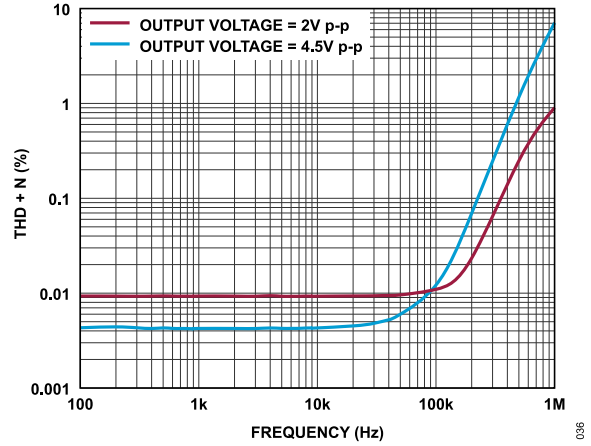
Figure 38. Total Harmonic Distortion + Noise (THD + N) vs. Frequency
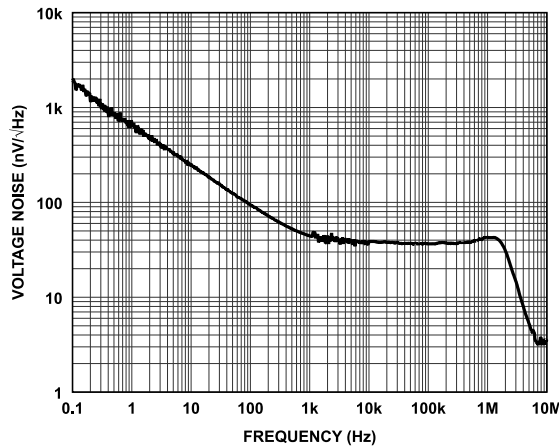
Figure 36. Spectral Density, RTI
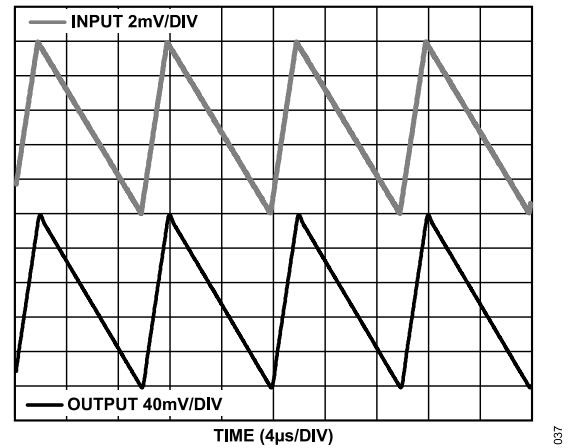
Figure 39. Output Response for 100 kHz, 20% Duty-Cycle, Sawtooth Waveform, Input Voltage (V_{IN}) = 10 mV p-p
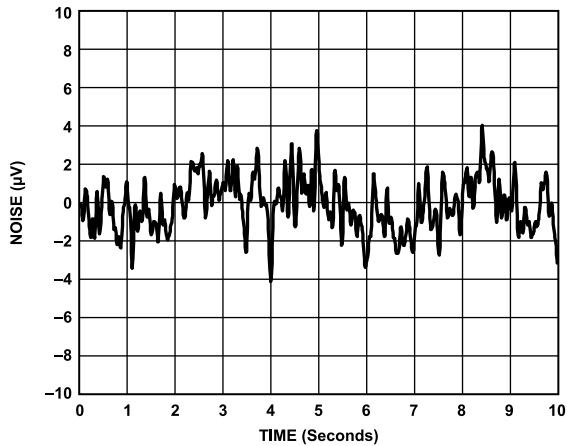
Figure 37. 0.1 Hz to 10 Hz Noise, RTI
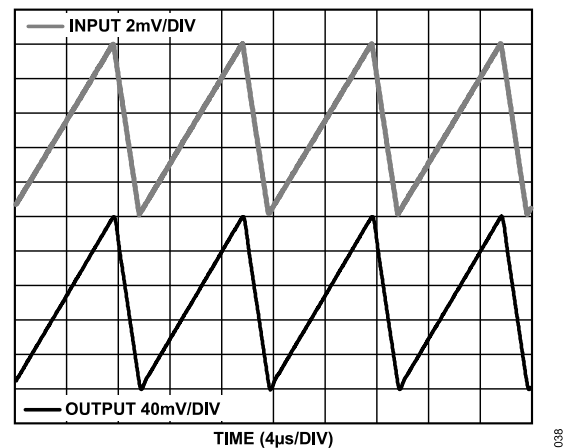
Figure 40. Output Response for 100 kHz, 80% Duty-Cycle, Sawtooth Waveform, Input Voltage (V_{IN}) = 10 mV p-p

TYPICAL PERFORMANCE CHARACTERISTICS
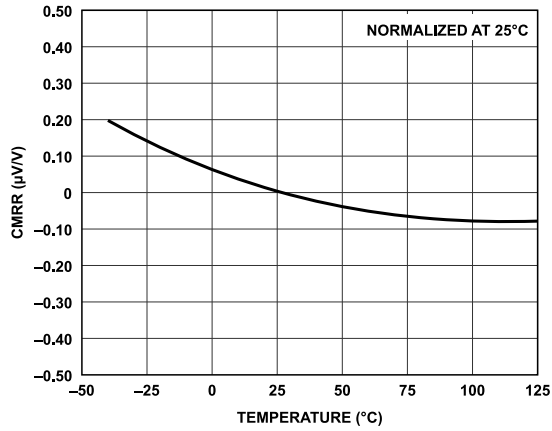
Figure 41. CMRR vs. Temperature

Figure 42. CMRR Distribution

Figure 43. Offset Voltage (V$_{OS}$) Distribution, RTI

Figure 44. Gain Error Distribution

Figure 45. Gain Error Drift Distribution

THEORY OF OPERATION

The AD8410A is a wide input voltage range, high bandwidth current-sense amplifier with PWM rejection that uses a unique architecture to accurately amplify the small differential current shunt voltages in the presence of rapidly changing common-mode voltages.

In typical applications, the AD8410A measures the current by amplifying the voltage across a shunt resistor connected to the inputs by a gain of 20 V/V (see Figure 46).

The AD8410A design provides excellent common-mode rejection, even with PWM common-mode inputs that can change at fast rates, such as 1 V/ns. The AD8410A has internal deglitch circuitry that helps to reduce the negative effects (such as the amplitude and settling time) of the output response in the prese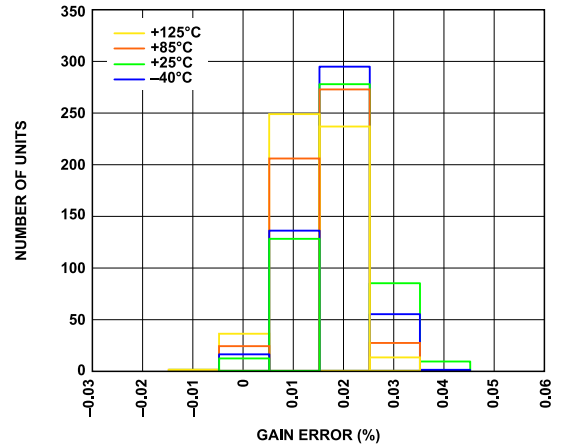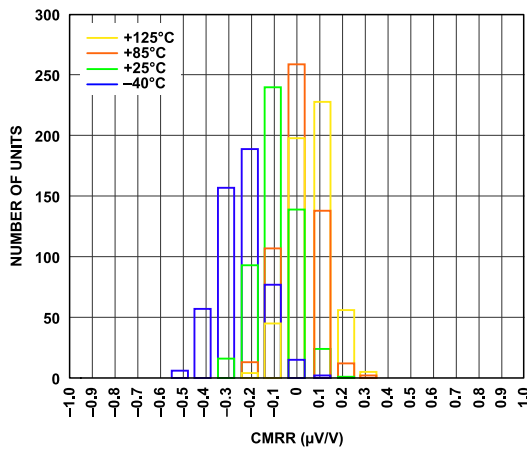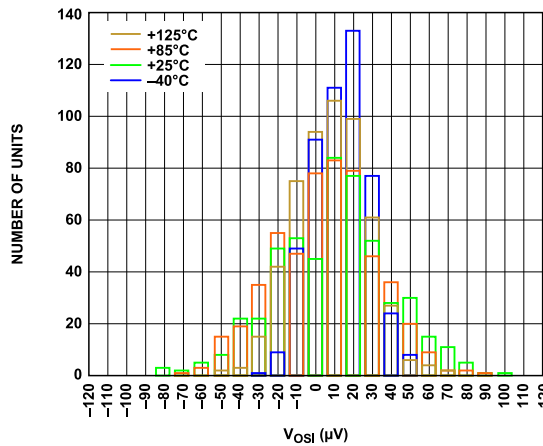nce of common-mode PWM input signals typically found in the applications for current-sense amplifiers. When there is a large common-mode transient at the input of the AD8410A, the output of the AD8410A is held at the last value for about 1 µs. This allows the change in the amplitude of the output of the AD8410A after a VCM step to remain low and undisturbed. After the typical 1 µs deglitch time, the output begins to settle to the appropriate value based on the differential voltage across the shunt resistor at the inputs (see Figure 9 and Figure 10).

The AD8410A features an in-package trim core, which leads to a typical offset drift of ±0.21 µV/°C throughout the operating temperature range and the common-mode voltage range without the need for chopping and autozero clocks (which could lead to intermodulation in the application). This architecture does not compromise bandwidth, which is typically rated at 2.2 MHz.

The reference input pins, $V_{REF}1$ and $V_{REF}2$, are tied through 60 kΩ resistors to the positive input of the main amplifier, which allows the output offset to be adjusted anywhere in the output operating range. The gain is 1 V/V from the reference pins to the output when the reference pins are used in parallel. When the reference pins are used to divide the supply, the gain is 0.5 V/V.

The AD8410A offers breakthrough performance without compromising the robust application needs typical of solenoid control, motor control, or DC-DC converters. The ability to reject PWM input common-mode voltages, and the DigiTrim architecture providing low offset and offset drift, allows the AD8410A to deliver total accuracy for these demanding applications.
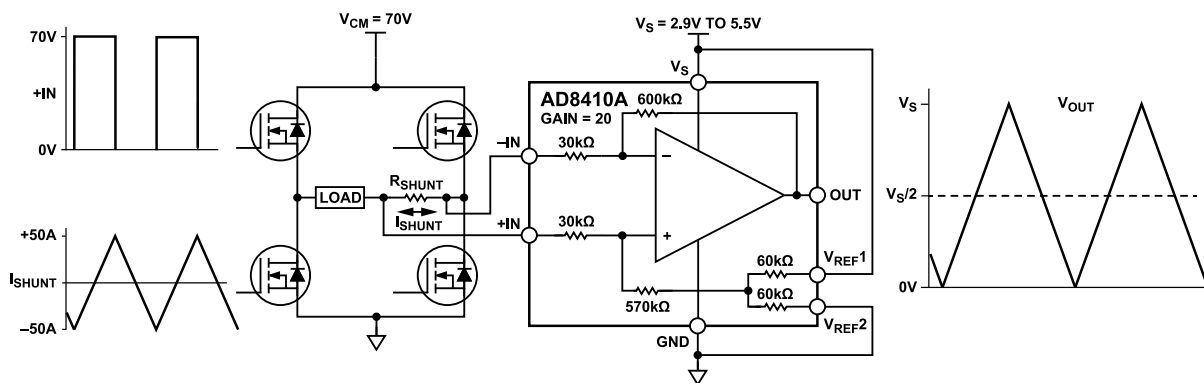

Figure 46. Typical Application

OUTPUT OFFSET ADJUSTMENT

The output of the AD8410A can be adjusted for unidirectional or bidirectional operation.

UNIDIRECTIONAL OPERATION

Unidirectional operation allows the AD8410A to measure currents through a resistive shunt in one direction. The basic modes for unidirectional operation are ground referenced output mode and V_S referenced output mode.

For unidirectional operation, the output can be set at the negative rail (near ground) or at the positive rail (near V_S) when the differential input is 0 V. The output moves to the opposite rail when a correct polarity differential input voltage is applied. The required polarity of the differential input depends on the output voltage setting. If the output is set at the positive rail, the input polarity must be negative to decrease the output. If the output is set at ground, the polarity must be positive to increase the output.

Ground Referenced Output Mode

When using the AD8410A in ground referenced output mode, both referenced inputs are tied to the GND pin, which causes the output to sit at the negative rail when there are zero differential volts at the input (see Figure 47).
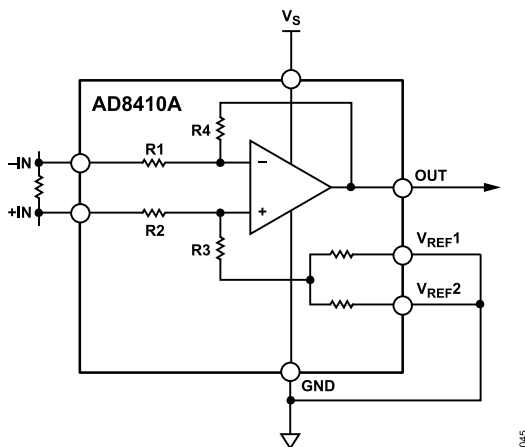
Figure 47. Ground Referenced Output

V_S Referenced Output Mode

V_S referenced output mode is set when both reference pins are tied to the positive supply. This mode is typically used when the diagnostic scheme requires detection of the amplifier and the wiring before power is applied to the load (see Figure 48).
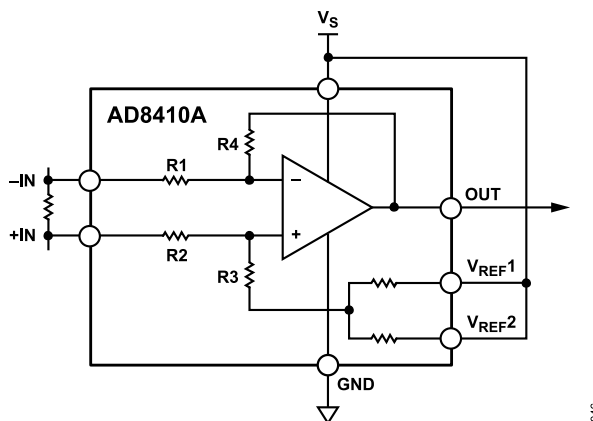
Figure 48. V_S Referenced Output

BIDIRECTIONAL OPERATION

Bidirectional operation allows the AD8410A to measure the currents through a resistive shunt in two directions.

In this case, the output is set anywhere within the output range. Typically, the output is set at half-scale for an equal range in both directions. In some cases, however, the output is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

Adjusting the output is accomplished by applying DC voltage to the reference inputs. $V_{REF}1$ and $V_{REF}2$ are tied to internal resistors that connect to an internal node. There is no operational difference between the reference pins.

EXTERNAL REFERENCED OUTPUT

Tie $V_{REF}1$ and $V_{REF}2$ together and to a reference to produce an output equal to the reference voltage when there is no differential input (see Figure 49). The output decreases with respect to the reference voltage when the input is negative, relative to the −IN pin, and increases when the input is positive, relative to the −IN pin.
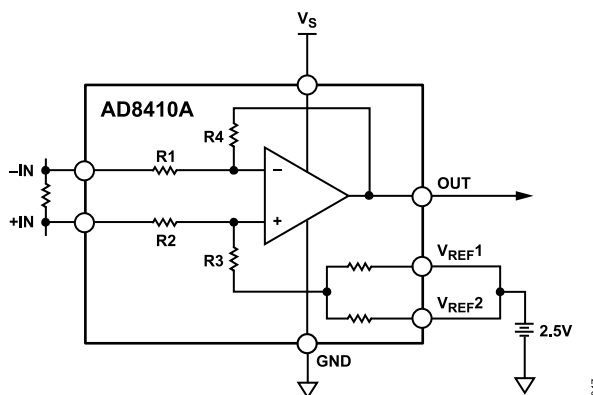
Figure 49. External Referenced Output

OUTPUT OFFSET ADJUSTMENT

SPLITTING THE SUPPLY

By tying one reference pin to the V_S pin and the other reference pin to the GND pin, the output is set at half of the supply when there is no differential input (see Figure 50). The benefit of this configuration is that an external reference is not required to offset the output for bidirectional current measurement. Tying one reference pin to the V_S pin and the other reference pin to the GND pin creates a midscale offset that is ratiometric to the supply, which means that if the supply increases or decreases, the output remains at half the supply. For example, if the supply is 5.0 V, the output is at half-scale or 2.5 V. If the supply increases by 10% (to 5.5 V), the output increases to 2.75 V.
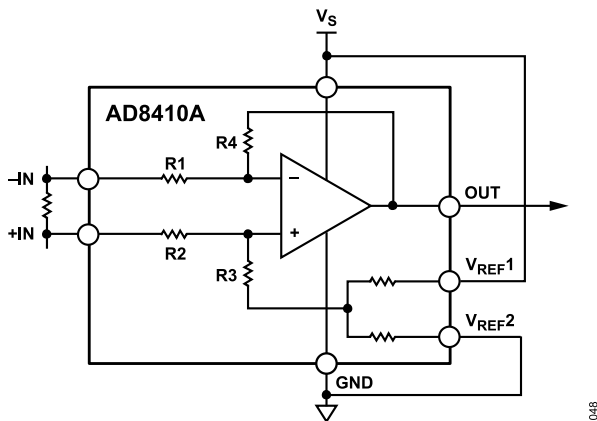
Figure 50. Split Supply

SPLITTING AN EXTERNAL REFERENCE

Use the internal reference resistors to divide an external reference by 2 with an accuracy of approximately 0.5%. Split an external reference by connecting one $V_{REF}X$ pin to the GND pin and the other $V_{REF}X$ pin to the reference voltage (see Figure 51).

Figure 51. Split External Reference

OFFSET VOLTAGE TERMINOLOGY

BOX METHOD

The AD8410A features an in-package trim core, which leads to a typical offset drift of ±0.21 µV/°C (using the Box Method) throughout the operating temperature range and the common-mode voltage range. This architecture does not compromise bandwidth, but the offset voltage drift signatures for the AD8410A vary part to part as shown in the Figure 52. After observing the mi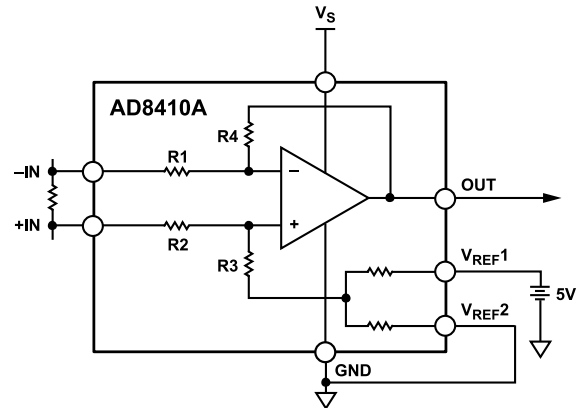nimum and maximum value for V_{OS} over the full temperature range from −40°C to 125°C, the V_{OS} in µV/°C is calculated for each part using the box method.
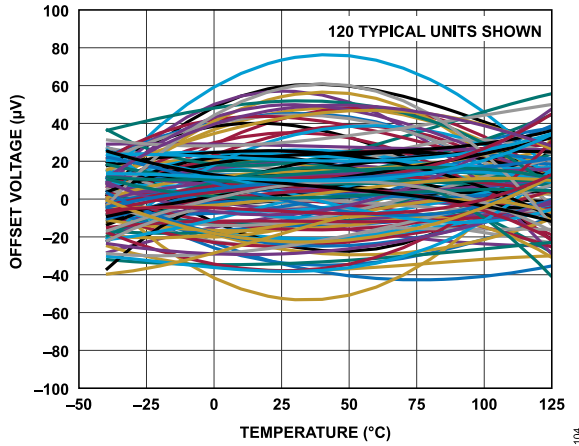
Figure 52. Offset Voltage vs. Temperature

A visual representation of this box method calculation and the mean value for the V_{OS} drift using the box method is shown in Figure 53. Based on the mean (Typ) value of ±0.21 µV/°C and the standard deviation of the box method drift of the 120 parts from Figure 52, a user can calculate a value (see equation (1)) for a guarantee V_{OS} drift by characterization, ±0.71 µV/°C.

$$\pm(MEAN + 5 \times (STANDARD\ DEVIATION)) \qquad (1)$$

This is valid from −40°C to 125°C temperature range.
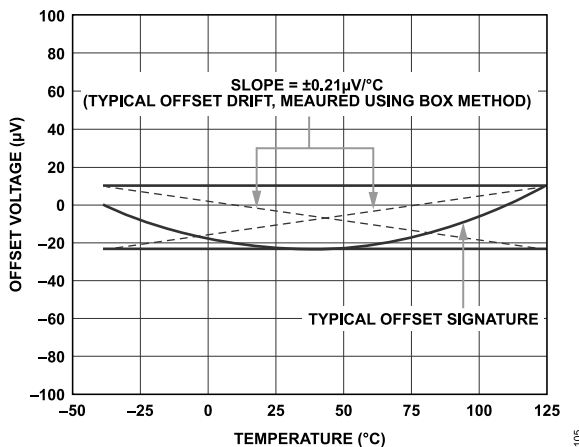
Figure 53. Box Method

BOWTIE METHOD

Typically, in the applications where the AD8410A is used, a calibration is done at 25°C. If a single point calibration at 25°C is done on the 120 parts as shown in Figure 52, this creates a plot shown in Figure 54. For each part, the slope of the line from 25°C to −40°C is calculated and the slope from 25°C to 125°C for each part is calculated. The mean and standard deviation for the slope of all the parts from 25°C to −40°C is then calculated. The V_{OS} max drift of ±1.85 µV/°C using the bowtie method is then calculated using equation (1). The mean and standard deviation for the slope of all the parts from 25°C to 125°C is then calculated. The V_{OS} max drift of 1.51 µV/°C using the bowtie method is then calculated using equation (1). The red lines in Figure 54 represent the worst-case V_{OS} drift slopes using the bowtie method that a user can guarantee through characterization. Calibrating at 25°C allows the max V_{OS} over the full temp range to be reduced to ~±151 µV, as opposed to the ±200 µV listed in the spec table as the max V_{OS} over temperature (with no calibration).

Figure 54. Bowtie Method

APPLICATIONS INFORMATION

MOTOR CONTROL

3-Phase Motor Control

The AD8410A is ideally suited for monitoring current in 3-phase motor applications such as brushless DC motors.

The 2.2 MHz typical bandwidth of the AD8410A provides instantaneous current monitoring. Additionally, the typical low offset drift of ±0.21 µV/°C means that the measurement error between the two motor phases is a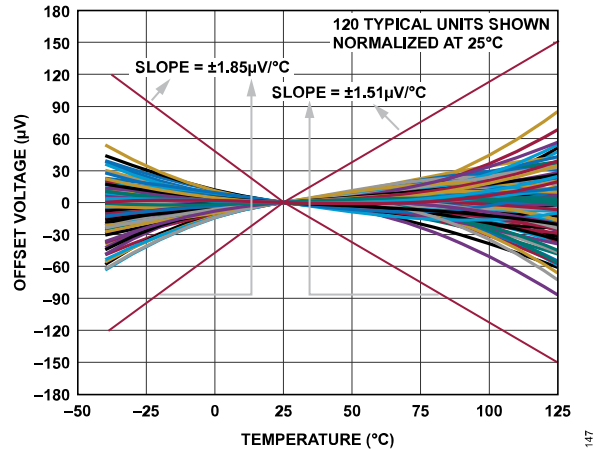t a minimum over temperature. The AD8410A rejects PWM input common-mode voltages in the −2 V to +70 V range. Monitoring the current on the motor phase allows sampling of the current at any point and provides diagnostic information, such as a short to ground and battery. The DigiTrim architecture used in the AD8410A provides precision specifications without the need for chopping and/or auto-zeroing. The DigiTrim architecture of the AD8410A avoids the potential for intermodulation distortion, which is observed when using amplifiers with chopping/auto-zero architectures. For the typical phase current measurement setup with the AD8410A, see Figure 55.
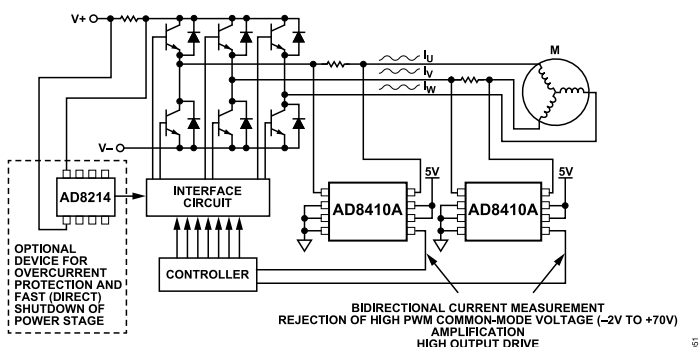
Figure 55. 3-Phase Motor Control

H-Bridge Motor Control

Another typical application for the AD8410A is to form part of the control loop in H-bridge motor control. In this case, place the shunt resistor in the middle of the H-bridge to accurately measure current in both directions by using the shunt available at the motor (see Figure 56). Using an amplifier and shunt in this location is a more accurate solution than a ground-referenced op amp because ground is not typically a stable reference voltage in this type of application. The instability of the ground reference causes inaccuracies in the measurements that can be made with a simple ground referenced op amp. The AD8410A measures current in both directions as the H-bridge switches and the motor changes direction. The output of the AD8410A is configured in an external referenced bidirectional mode (see the Bidirectional Operation section).

Figure 56. H-Bridge Motor Control

APPLICATIONS INFORMATION

SOLENOID CONTROL

High-Side Current Sense with a Low-Side Switch

In the case of a high-side current sense with a low-side switch, the PWM control switch is ground referenced. Connect an inductive load (solenoid) to a power supply and place a resistive shunt between the switch and the load (see Figure 57). An advantage of placing the 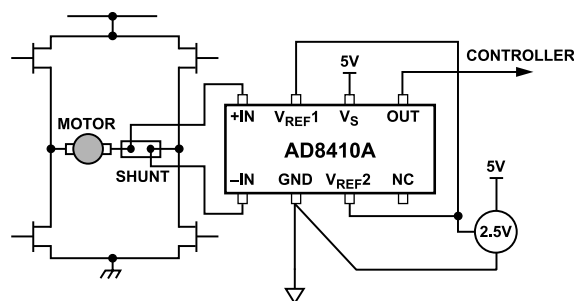shunt on the high side is that the entire current, including the recirculation current, is measurable because the shunt remains in the loop when the switch is off. In addition, diagnostics are enhanced because shorts to ground are detected with the shunt on the high side.

In this circuit configuration, when the switch is closed, the common-mode voltage decreases to near the negative rail. When the switch is open, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop above the battery by the clamp diode.
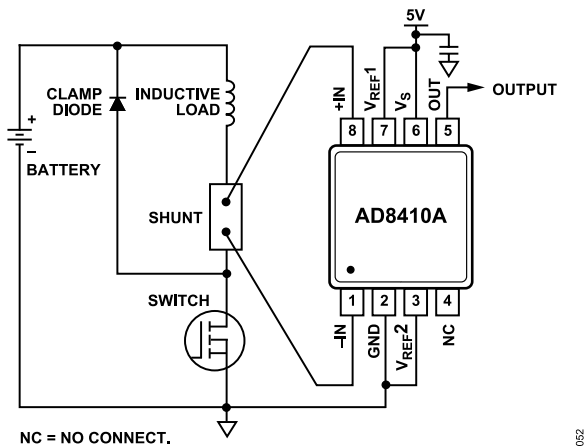

Figure 57. Low-Side Switch

High-Side Current Sense with a High-Side Switch

The high-side current sense with a high-side switch configuration minimizes the possibility of unexpected solenoid activation and excessive corrosion due to constant battery draw (see Figure 58). In this case, both the switch and the shunt are on the high side. When the switch is off, the battery is removed from the load, which prevents damage from potential shorts to ground while still allowing the recirculating current to be measured and to provide diagnostics. Removing the power supply from the load for the majority of the time that the switch is open minimizes the corrosive effects that can be caused by the differential voltage between the load and ground.

When using a high-side switch, the battery voltage is connected to the load when the switch is closed, causing the common-mode voltage to increase to the same value as the battery voltage. In this case, when the switch is open, the voltage reversal across the

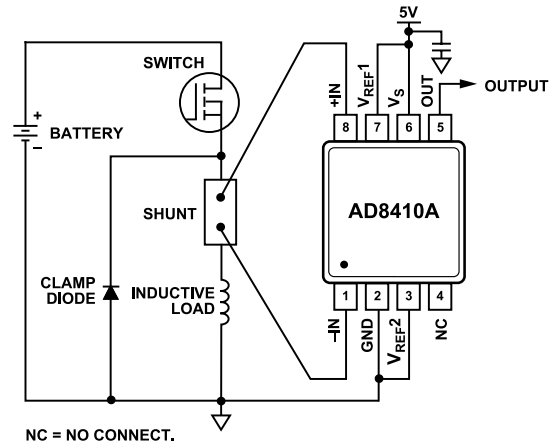inductive load causes the common-mode voltage to be held one diode drop below ground by the clamp diode.

Figure 58. High-Side Switch

High Rail Current Sensing

In the high rail current sensing configuration, the shunt resistor is referenced to the battery. High voltage is present at the inputs of the current-sense amplifier. When the shunt is battery referenced, the AD8410A produces a linear ground-referenced analog output. Additionally, the AD8214 provides an overcurrent detection signal in <100 ns (see Figure 59). This feature is useful in high current systems where fast shutdown in overcurrent conditions is essential.
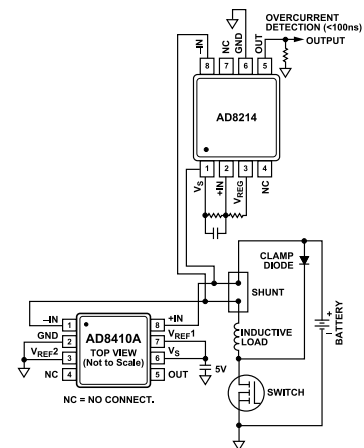
Figure 59. High Rail Current Sensing

INPUT FILTER

In typical applications, such as motor control and solenoid current sensing, filtering at the input of the AD8410A can be beneficial in reducing differential noise, as well as transients and current ripples flowing through the input shunt resistor. Also, it is recommended to filter at the input of the AD8410A to further reduce the electromagnetic interference (EMI). The EMI specifications vary depending on the application. Filter at the input if the output cannot be filtered because filtering at the output changes the low output impedance

APPLICATIONS INFORMATION

seen by the components attached to the output of the AD8410A. The +IN and −IN pins of the AD8410A have balanced input-bias currents. The input series resistors, R1 and R2 in Figure 60, must be the same measured value not to add large offset voltage on the output of the device as a result of R1 and R2. It is recommended to keep R1 and R2 at or below 100 Ω. In Figure 60, C1 and C3 must be the same value.

For example, at 48 V common-mode, when using a 10 Ω resistor for R1 and R2, the estimated maximum error that is seen on the input of the AD8410A ($V_{ErrorRTI}$) due to the R1 and R2resistors in the input filter is:

$$V_{ErrorRTI} = 10\ \Omega \times 2.7\ \mu A = 27\ \mu V \tag{2}$$

Where 2.7 μA is the maximum input offset current at 48 V input common mode, as listed in Table 1.

The EMI filter has two different bandwidths, common-mode and differential. The differential bandwidth defines the frequency response of the filter with a differential input signal applied between the two inputs of the amplifier, +IN and −IN.

The −3 dB differential bandwidth for the filter is:

$$BW_{DIFF} = \frac{1}{2\pi \times R1 \times ((2 \times C2) + C1)} \tag{3}$$

The common-mode bandwidth defines what a common-mode RF signal sees between GND and the +IN and −IN of the amplifier tied together.

The −3 dB common-mode bandwidth for the filter is:

$$BW_{CM} = \frac{1}{2\pi \times R1 \times C1} \tag{4}$$

Keep the resistor values to a 1% tolerance and the filter capacitors to a 5% tolerance to assist with reducing AC common-mode rejection (CMR) errors. Choose C2 to be at least 10× larger than C1 or C3 to reduce AC CMR errors, which are caused by component mismatching.

Figure 60. Input Filter

OVERCURRENT DETECTION

In several current sensing applications, it is required to quickly detect when the current exceeds a certain threshold in the presence of a fault condition for safety concerns. As mentioned in the High Rail Current Sensing section, the AD8214 can be used for overcurrent detection in high current systems where fast shutdown in overcurrent conditions is essential.

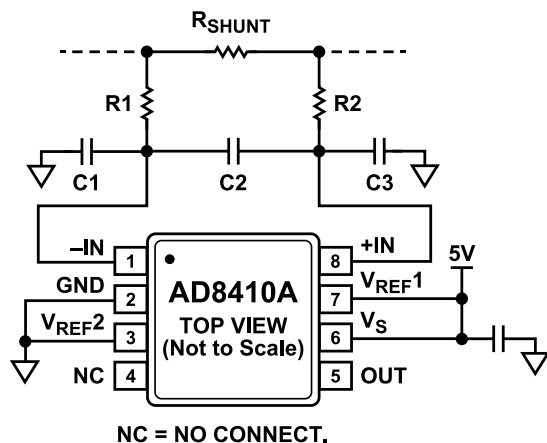Another common practice for overcurrent detection in current-sense applications is to use a comparator on the output of the current-sense amplifier. Figure 61 and Figure 62 show typical configurations for monitoring current and using a comparator for overcurrent detection in unidirectional current and bidirectional currents, respectively.

Choose the values of R1 and R2 in Figure 61 and Figure 62 to set the threshold voltage at which the overcurrent detection trips. For example, for the bidirectional overcurrent detection configuration shown in Figure 62, if the shunt resistance (R_{SHUNT}) is 25 mΩ, and it is required to trip the overcurrent detection at ±3 A, use the following equations (5), (6), and (7) to find the R1 value after choosing an arbitrary value for R2. Choose, R2 = 4800 Ω, and V_S = 5 V.

Threshold voltage (V_{THR}) is the voltage that the output of the AD8410A must reach to trip the overcurrent detection. If it is required that the overcurrent detection trips at 3 A, then:

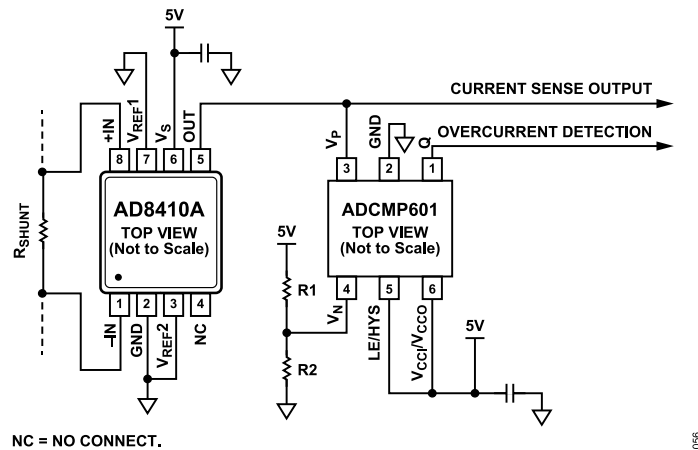$$V_{THR} = 3\ A \times R_{SHUNT} \times 20\ V/V + 2.5\ V \tag{5}$$

The 2.5 V is added because the references are set up in split supply mode, then:

$$V_{THR} = 3\ A \times 25\ m\Omega \times 20\ V/V + 2.5\ V = 4\ V \tag{6}$$

After V_{THR} is known, use the following equation (7) to find R1:

$$R1 = \frac{R2(V_S - V_{THR})}{V_{THR}} = \frac{4800\ \Omega \times (5\ V - 4\ V)}{4\ V}$$
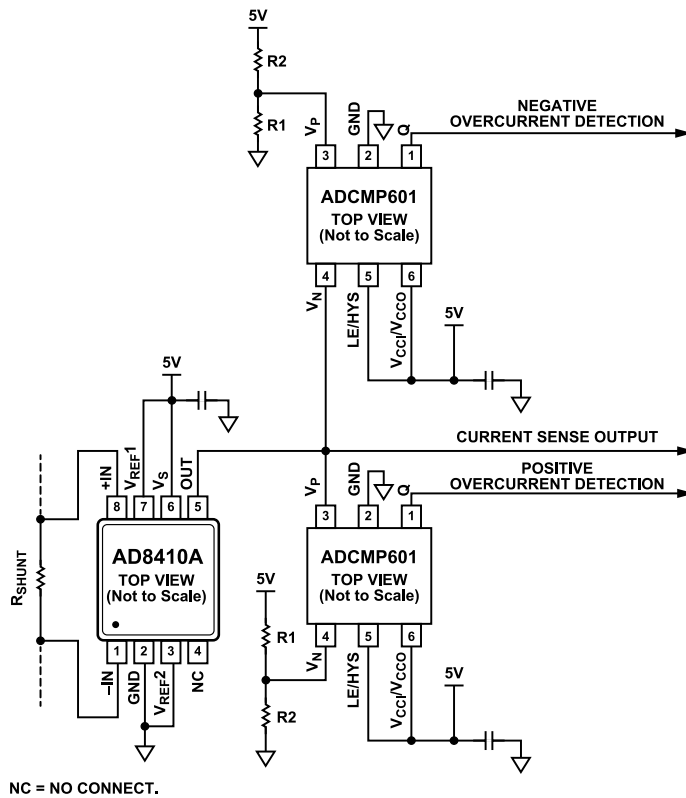$$= 1200\ \Omega \tag{7}$$

APPLICATIONS INFORMATION

*Figure 61. Unidirectional Overcurrent Detection*

Figure 62. Bidirectional Overcurrent Detection

For the second ADCMP601, keep the same values for R1 and R2. Attach the V_N pin to the output of the AD8410A, attach R2 to the 5 V supply, attach R1 to ground, and attach the V_P pin to the connection between R2 and R1 to allow negative overcurrent detection (as shown in Figure 62).

Therefore, when the output of the AD8410A reaches as shown in equation (8), then the output of the ADCMP601 used for negative overcurrent detection trips high.

$$1\ \text{V} (2.5\ \text{V} - 3\ \text{A} \times 25\ \text{m}\Omega \times 20\ \text{V/V}) = 1\ \text{V} \tag{8}$$

OUTLINE DIMENSIONS
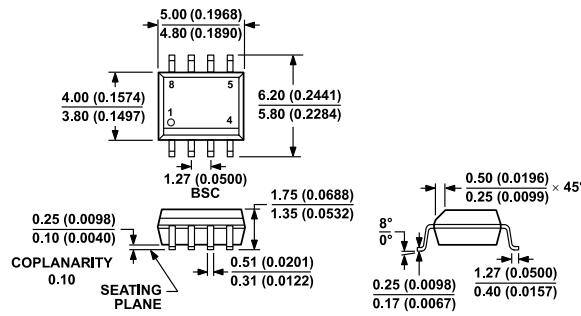
COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 63. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions Shown in millimeters and (inches)

Updated: January 21, 2023

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
AD8410AWBRZ	−40°C to +125°C	8-Lead SOIC_N	Tube, 98	R-8
AD8410AWBRZ-RL	−40°C to +125°C	8-Lead SOIC_N	Reel, 2500	R-8

[1] Z = RoHS-Compliant Part.

[2] W = Qualified for Automotive Applications.

EVALUATION BOARDS

Model[1]	Description
AD8410AR-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.