

# DEVKIT-MPC5748G

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### Caution:

These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

### Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2. 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in *ITALICS*

### Revision Information

Rev	Date	Designer	Comments
X1	23 Sep 2015	Catalin Neacsu	Initial release
X2	24 Sep 2015	Catalin Neacsu	Further changes. Decreased component size where possible.
X3	29 Sep 2015	Catalin Neacsu	Changed ethernet page. Changed caps around Q50 Rearranged GPIOs on page 15. Added more LEDs on page 14
X4	02 Oct 2015	Catalin Neacsu	Changed U50, USB connectors, ETH Connector, BOM optimization
X5	05 Oct 2015	Catalin Neacsu	Changed PN of U11 and C23
X6	07 Oct 2015	Catalin Neacsu	Small visual updates
X7	08 Oct 2015	Catalin Neacsu	Add separation resistors for USB interface, U50
X8	12 Oct 2015	Catalin Neacsu	Changed 3V3 converter, minor BOM optimization
X9	14 Oct 2015	Catalin Neacsu	Changed 3V3 converter, minor BOM optimization, better cost
X10	21 Oct 2015	Catalin Neacsu	Updated IO connections per Jesus Sanchez's request Added TP on page 3 per Ruiz Ricardo's request
X11	27 Oct 2015	Catalin Neacsu	Changed Power Supply page Added one user led
X12	28 Oct 2015	Catalin Neacsu	Changed PN for P2 and P7
X13	30 Oct 2015	Catalin Neacsu	Changed Power Supply page to allow supply selection
X14	02 Nov 2015	Catalin Neacsu	BOM Optimization
X15	03 Nov 2015	Catalin Neacsu	PN change for L1
X16	23 Dec 2015	Catalin Neacsu	Added Open SDA block Implemented other feedback
X17	06 Jan 2016	Catalin Neacsu	Implemented OpenSDA feedback
X18	08 Jan 2016	Catalin Neacsu	Changed some ICs to their NXP equivalent
X19	15 Jan 2016	Catalin Neacsu	P12, Y50 add GND connections. JTAG connector 14 pins
A	26 Jan 2016	Catalin Neacsu	Prototype Release
A1	13 Jun 2016	Jun Qiao	Update with Flexray, OpenSDA, Ethernet, LED, Buttons, GPIO.
A2	20 Jun 2016	Jun Qiao	Update with OpenSDA, GPIO connectors.
B	24 Jun 2016	Jun Qiao	Pilot Release

3 Different test points used in design:

TPVx - Through Hole Pad small


TPHx - Through Hole Pad Large (for standard 0.1" header).  
Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop

 TPV?

 TPH?

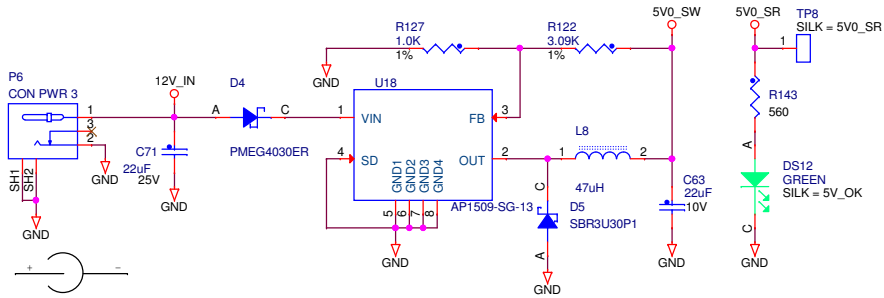
 TP?

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ICAP Classification:		CP:	IUC: PUBL: <b>X</b>
Designer: C Neacsu	Drawing Title: <b>DEVKIT-MPC5748G</b>		
Drawn by: C Neacsu	Page Title: <b>Index and Title Page</b>		
Approved: Peeses Philip	Size B	Document Number SCH-29030 PDF: SPF-29030	Rev B
Date: Thursday, July 21, 2016		Sheet 1 of 15	

# Power Input and Voltage Regulators

## 12V Power Supply Input 5V Switching Regulator

Input Voltage 12V, Output 5V at 1800mA

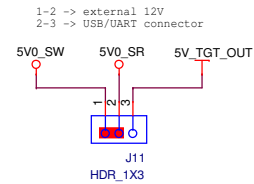


LAYOUT NOTE:  
ADD Graphical silk:

Layout note: follow IC datasheet recommendations for PCB layout and thermal dissipation

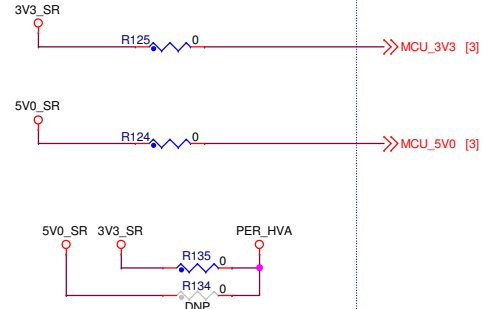
## Board supply selection

Select between USB and external 12V

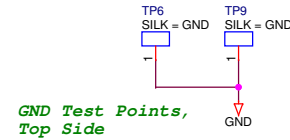


## Power Control

Jumpers can be fitted to facilitate power measurements

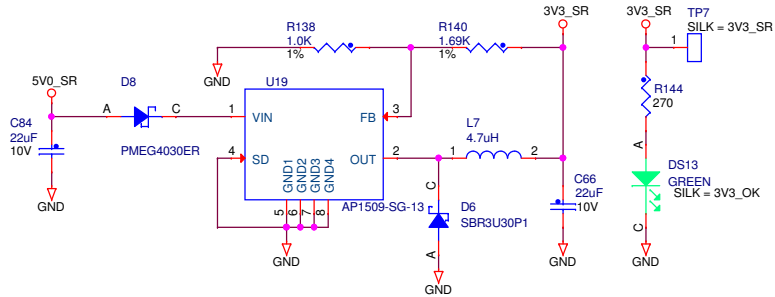


## Test and reference points



## 3.3V Switching Regulator

Input Voltage 5V, Output 3.3V at 1600mA



Layout note: follow IC datasheet recommendations for PCB layout and thermal dissipation

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ICAP Classification:		CP:	IUC: PUBI: <b>X</b>
Designer:	Drawing Title: <b>DEVKIT-MPC5748G</b>		
Drawn by:	Page Title: <b>Power Input, 5V, 3.3V Reg</b>		
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# Calypto MCU Power Connections

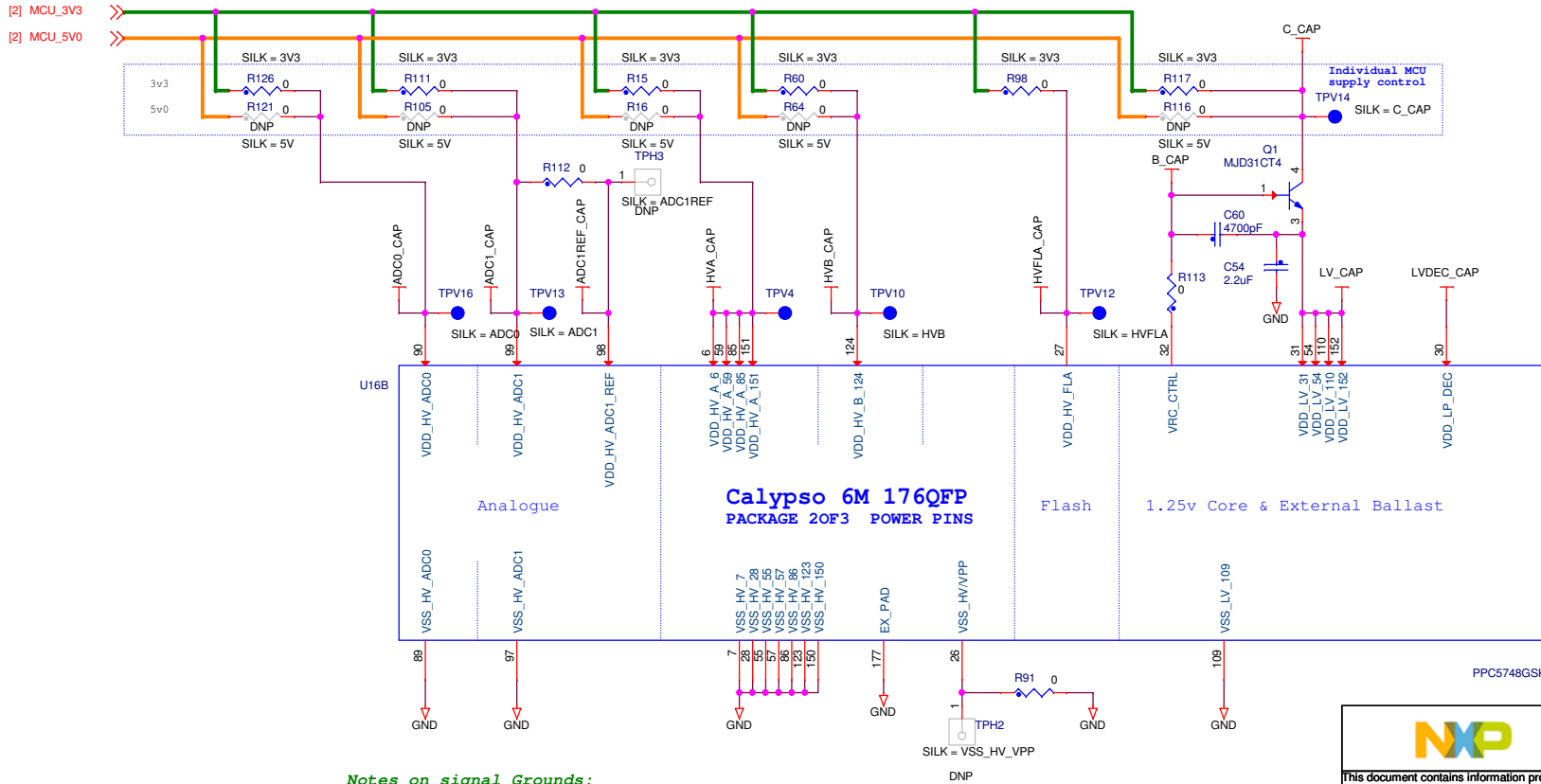
## Power Supply Constraints:

- If VDD\_HV\_A is driven from 3.3V, VDD\_HV\_FL A must also be supplied from 3.3V
- If VDD\_HV\_A is driven from 5V, the VDD\_HV\_FL A pin must be disconnected from 3.3V
- Don't attempt to over drive an analogue pad to 5V when the digital VDD\_HV\_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD\_HV\_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD\_HV\_A domain

## Default Configuration:

- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD\_HV\_A, VDD\_HV\_B, VDD\_HV\_C, VBallast)
- VDD\_HV\_FL A = External 3.3V supplied (jumper fitted)

The analogue pins can only be driven to the same voltage as the VDD\_HV\_x domain they are situated in (ie max 3.3V) so makes sense for the analogue supply and reference to be 3.3V

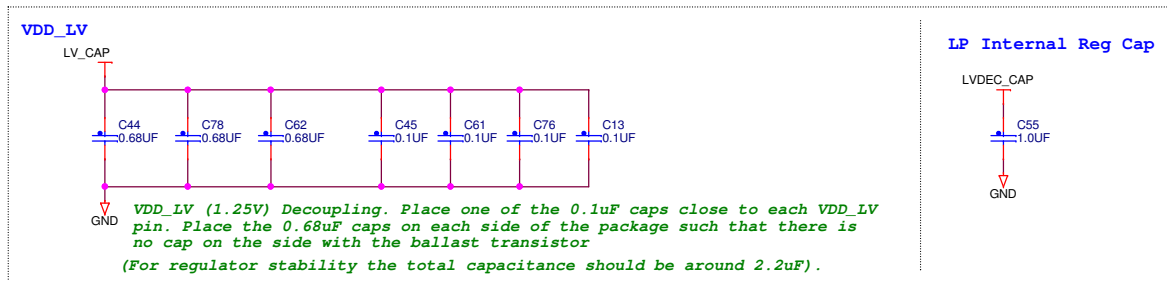
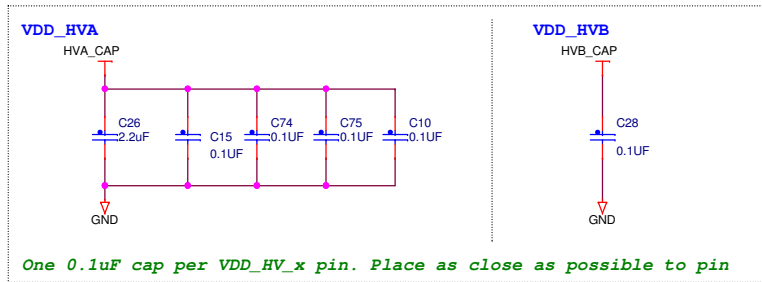
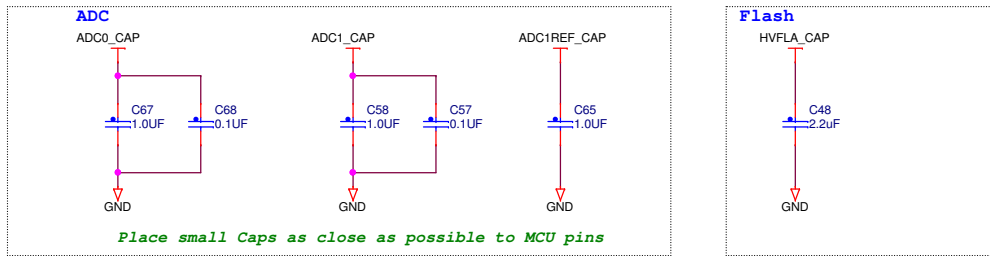


## Notes on signal Grounds:

- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue grond plane with single entry point (or ferrite) to digital ground plane.

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		1	

# Calypso MCU Decoupling and bulk storage

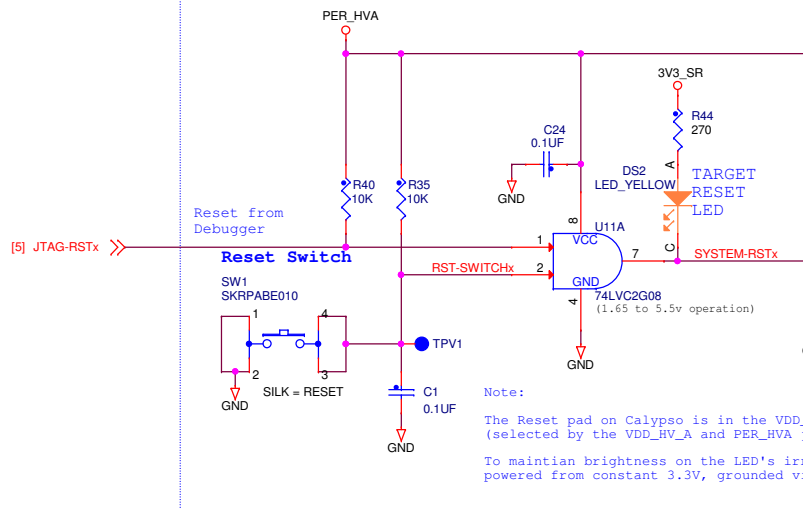


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# Reset and External Clock In

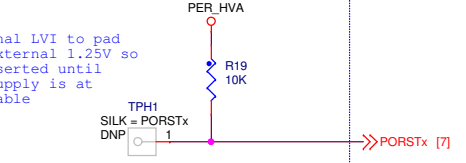
Reset is in the VDD\_HVA domain.

## Reset Input / Output



## PORST

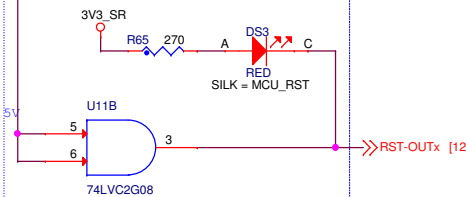
Connect an external LVI to pad when supplying external 1.25V so that PORST is asserted until external 1.25V supply is at threshold and stable



Bi Directional reset line to/from MCU

## Buffered RESET-out

Active reset drive (high / low) for any peripherals that need to be reset when MCU is in reset



## JTAG Standard 14-pin Connector

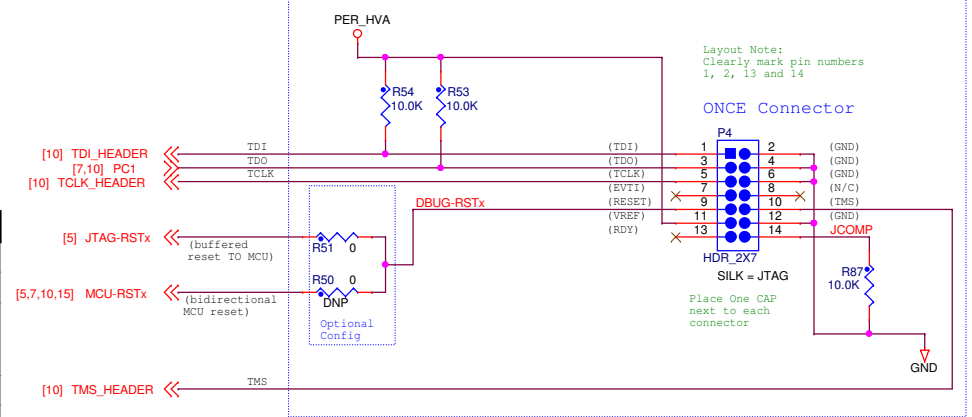


Table 13-3. Functional terminal state during power-up and reset

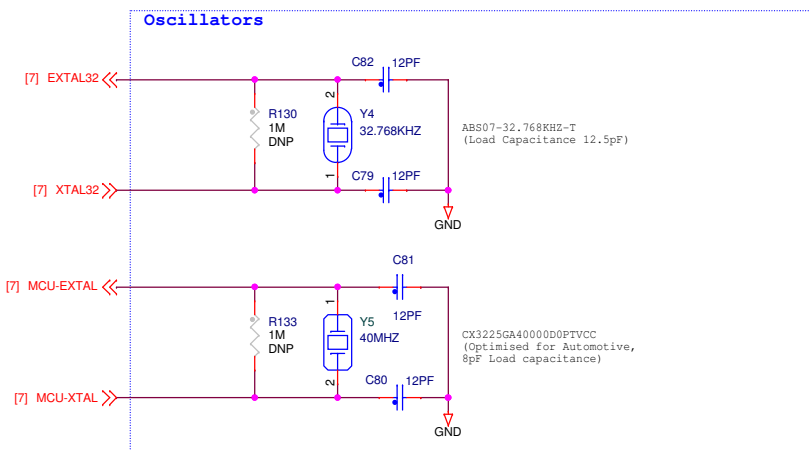
TERMINAL TYPE <sup>1</sup>	POWERUP pad state <sup>2</sup>	RESET pad state	DEFAULT pad state <sup>3</sup>	Comments
RESET	strong pull-down	strong pull-down	weak pull-up	functional reset pad.
PORST <sup>4</sup>	Weak pull down	Weak pull up	weak pull-up	power on reset pad.
GPIO	high impedance	high impedance	high impedance	by default, but configurable for STANDBY exit
ANALOG	high impedance	high impedance	high impedance	-
EOUT0, EOUT1	high impedance	high impedance	high impedance	-
TCK	high impedance	weak pull-up	weak pull-up	-
TMS	high impedance	weak pull-up	weak pull-up	-
TDI	high impedance	weak pull-up	weak pull-up	-
TDO	high impedance	high impedance	high impedance	-
TCK_ALT	high impedance	weak pull-up	weak pull-up	-
TMS_ALT	high impedance	weak pull-up	weak pull-up	-
TDI_ALT	high impedance	weak pull-up	weak pull-up	-
TDO_ALT	high impedance	high impedance	high impedance	-

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<b>DEVKIT-MPC5748G</b>					
By:	Page Title:				
<b>Reset Circuitry &amp; External Clock In, JTAG</b>					
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# Clocks



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Drawn by:	Page Title: <b>Clocks</b>		
Approved:	Size	Document Number	Rev
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U16A

[14] PA0	<< (LKD2)	24	PA0/GPIO0/EUOC_0_XCLKOUT0/EUOC_13_HWKPUI9/CAN1RX	LN11RXWKPUI6/CANRXVSL1/EUOC_16_XGPIO84/PE0	18	(GPIO)	PE0 [15]
[15] PA1	<< (GPIO)	19	PA1/GPIO1/EUOC_1_SWKPUI2/CANRXNM0	SDA1/CANTX/EUOC_17_YGPIO65/PE1	20	(GPIO)	PE1 [15]
[15] PA2	<< (GPIO)	17	PA2/GPIO2/EUOC_2_G/EUOC_0_XADCO_MAO2/WKPUI3	ULPI0_CLK/EIRO21/DSN1_1/SD_DAT3FR_A_TX_EN/EUOC_18_YGPIO66/PE2	156	(GPIO)	PE2 [13]
[14] PA3	<< (LSD1)	114	PA3/GPIO3/EUOC_3_G/LIN1TX/DCS4_1/MI_RX_CLK/EIRO0/ADCI_S0	ULPI0_NXT/WKPUI25/FR_A_RX/SD_CMD/DSOUT_1/EUOC_19_YGPIO67/PE3	157	(GPIO)	PE3 [13]
[14] PA4	<< (LSD1)	51	PA4/GPIO4/EUOC_4_G/DCS0_1/EUOC_24_YLN1RX/WKPUI9/CMP1_13	EIRO21/ULPI0_DS0/DAT1/FR_B_TX/DSCLK_1/EUOC_20_YGPIO68/PE4	160	(GPIO)	PE4 [19]
[15] PA5	<< (GPIO)	147	PA5/GPIO5/EUOC_5_G/LIN4TX/E2_ODS1/ULPI0_STP	WKPUI0/FR_B_RX/ULPI0_DS/SD_DAT2/ADCO_MAO/DCS0_1/EUOC_21_YGPIO69/PE5	161	(GPIO)	PE5 [19]
[15] PA6	<< (GPIO)	146	PA6/GPIO6/EUOC_6_G/DCS1_1/EZ_ODS0/LIN1RX/EIRO1/ULPI0_DIR	EIRO22/SD_CMD/ADCI_MAO/ADCO_MAO/DCS2_0/EUOC_22_XGPIO70/PE6	167	(GPIO)	PE6 [19]
[14] PA7	<< (LSD5)	128	PA7/GPIO7/EUOC_7_G/LIN1TX/MI_RX/D2/EIRO2/ADCI_S8	EIRO23/SD_CLK/ADCI_MAO/ADCO_MAO/DCS2_0/EUOC_23_XGPIO71/PE7	168	(GPIO)	PE7 [19]
[12] PA8	<< (HW1_EUOC4)	130	PA8/GPIO8/EUOC_8_X/EUOC_14_H/MI_RX/MI_RX/D1/EIRO3/RVSD/LIN1RX/ADCI_S9	SDA2/CANTX/EUOC_22_X/CANTX/GPIO72/PE8	22	(GPIO)	PE8 [19]
[12] PA9	<< (HW1_EUOC4)	130	PA9/GPIO9/EUOC_9_H/DCS2_1/MI_RX/MI_RX/RXD0/RVSD/ADCI_S10	CANRX/CANRX/WKPUI70/SD/EUOC_23_XGPIO73/PE9	25	(GPIO)	PE9 [15]
[14] PA10	<< (LSD3)	131	PA10/GPIO10/EUOC_10_H/SDA0/LIN2TX/MI_RX/COU/DSN1_1/ADCI_S11	EIRO10/SDA3/EIUC_30_YDCSS_1/LIN1TX/GPIO74/PE10	23	(GPIO)	PE10 [19]
[12] PA11	<< (GPIO)	53	PA11/GPIO11/EUOC_11_H/SCLO/ULPI0_FAULT/MI_RX/RX/EIRO16/LIN1RX/ADCI_S12	WKPUI4/LIN1RX/CS/LCKOUT1/DCS4_1/EUOC_24_XGPIO75/PE11	133	(SW2)	PE11 [15]
[15] PA12	<< (GPIO)	52	PA12/GPIO12/EUOC_12_G/DCS3_1/EUOC_26_Y/EIRO17/DSN1_0/CMP1_15	ADCI_S13/EIRO11/DSN1_2/MI_CRS/ULPI0_FAULT/EIUC_19_YGPIO76/PE12	127	(GPIO)	PE12 [14]
[15] PA13	<< (GPIO)	50	PA13/GPIO13/DSOUT_0/EUOC_29_Y/EUOC_25_Y/CANTX/CMP1_14	ADCI_X3/MI_RX/D3/EIUC_20_Y/DSOUT_2/GPIO77/PE13	137	(GPIO)	PE13 [15]
[15] PA14	<< (GPIO)	48	PA14/GPIO14/DSCLK_0/DCS0_0/EUOC_0_X/EUOC_23_X/EIRO4/CMP1_12	EIRO12/ULPI0_D2/EIUC_21_Y/DSCLK_2/GPIO78/PE14	136	(GPIO)	PE14 [11]
[15] PA15	<< (GPIO)	50	PA15/GPIO15/DCS0_0/DSCLK_0/EUOC_1_G/EUOC_21_Y/CANRX/WKPUI0/CMP1_10	ULPI0_DS/CLK_2/EIUC_22_X/DCS0_2/GPIO79/PE15	137	(SW1_SW2)	PE15 [11]
[9] PB0	<< (CAN0_TX)	39	PB0/GPIO16/CAN0TX/EUOC_30_Y/LIN0TX/EUOC_4_Y/CMP0_2	SAI0_MCLK/CMP2_16/ADCO_S8/CAN5TX/SOUT_4/DCS3_1/EUOC_10_H/GPIO80/PF0	63	(GPIO)	PF0 [15]
[9] PB1	<< (CAN0_RX)	40	PB1/GPIO17/EUOC_31_Y/EUOC_5_Y/LIN0RX/WKPUI4/CMP0_3/CAN0RX	SIN_4/CMP2_17/ADCO_S9/SAI0_BCLK/CS3_0/DCS4_1/EUOC_11_H/GPIO81/PF1	65	(GPIO)	PF1 [15]
[9] PB2	<< (CAN0_RX)	1	PB2/GPIO18/LIN1TX/SDA0/EUOC_30_Y/SD_DAT17	CMP2_18/ADCO_S10/SAI0_DS/CLK_4/DCS0_2/EUOC_12_H/GPIO82/PF2	66	(GPIO)	PF2 [15]
[9] PB3	<< (CAN0_RX)	1	PB3/GPIO19/EUOC_31_Y/SAI0/EUOC_8_X/WKPUI1/LIN0RX	CMP2_19/ADCO_S11/SAI0_DS/CS0_4/DCS1_2/EUOC_13_H/GPIO83/PF3	67	(GPIO)	PF3 [15]
[14,15] PB4	<< (GPIO)	91	PB4/GPIO20/ADCI_P0	CMP2_20/ADCO_S12/SAI0_D1/SOUT_5/DCS2_2/EUOC_14_H/GPIO84/PF4	68	(GPIO)	PF4 [15]
[15] PB5	<< (GPIO)	92	PB5/GPIO21/ADCI_P1	SIN_5/CMP2_21/ADCO_S13/SAI0_DS/CS2_0/DCS3_2/EUOC_22_X/GPIO85/PF5	69	(GPIO)	PF5 [15]
[15] PB6	<< (GPIO)	91	PB6/GPIO22/ADCI_P2	CMP2_22/ADCO_S14/ADCO_S14/EUOC_30_Y/SAI0_SYNC/CLK_5/DCS1_1/EUOC_23_X/GPIO86/PF6	69	(GPIO)	PF6 [15]
[15] PB7	<< (GPIO)	61	PB7/GPIO23/ADCI_P3	SAI1_MCLK/CMP2_23/ADCO_S15/CS0_5/DCS2_1/CLK_0/GPIO87/PF7	42	(GPIO)	PF7 [15]
[6] XTAL32	<< (GPIO)	60	PB8/GPIO24/ADCI_S0/WKPUI25/OSC32K_XTAL	CMP0_2/EUOC_15_Y/CANTX/DCS4_0/CANTX/GPIO88/PF8	41	(GPIO)	PF8 [15]
[6] EXTERNAL32	<< (GPIO)	60	PB9/GPIO25/ADCO_S1/WKPUI26/OSC32K_XTAL	CMP0_4/WKPUI22/CAN3RX/CAN2RX/EUOC_14_Y/DCSS_0/EIUC_1_H/GPIO89/PF9	46	(GPIO)	PF9 [15]
[15] PB10	<< (GPIO)	96	PB10/GPIO26/DSOUT_1/CAN3TX/CMP2_0/SAI0_SYNC/EUOC_29_Y/ADCO_S2/WKPUI8/CANRX	CMP1_8/EUOC_19_Y/EIUC_2_H/LIN1TX/DCS1_0/GPIO90/PF10	47	(GPIO)	PF10 [15]
[15] PB11	<< (GPIO)	101	PB11/GPIO27/EUOC_3_G/DCS0_0/ADCO_S3	CMP1_9/WKPUI5/LIN1RX/EUOC_20_Y/EIUC_3_H/DCS2_0/GPIO91/PF11	43	(GPIO)	PF11 [15]
[15] PB12	<< (GPIO)	103	PB12/GPIO28/EUOC_4_G/DCS1_0/DO1/ADCO_X0	CMP0_6/EUOC_16_X/LIN1TX/EIUC_25_Y/GPIO92/PF12	49	(GPIO)	PF12 [15]
[15] PB13	<< (GPIO)	105	PB13/GPIO29/EUOC_5_G/DCS2_0/MLBON/ADCO_X1	CMP1_11/WKPUI6/LIN1RX/EUOC_22_X/EIUC_26_Y/GPIO93/PF13	126	(SW1_SW2)	PF13 [15]
[15] PB14	<< (GPIO)	107	PB14/GPIO30/EUOC_6_G/DCS3_0/FR_DSG1/MLBSN/ADCO_X2	ADCI_X2/MI_RX/MDO/CAN1TX/EUOC_27_Y/CANTX/GPIO94/PF14	125	(GPIO)	PF14 [12]
[15] PB15	<< (GPIO)	107	PB15/GPIO31/EUOC_7_G/DCS4_0/MLBSG/MLBON/ADCO_X3	ADCI_X1/EIRO13/CANRX/CAN1RX/MI_RX/RX/DVE/EIUC_4_H/GPIO95/PF15	125	(SW1_SW2)	PF15 [12,15]
[10] PC0	<< (TD1)	154	PC0/GPIO32/RVSD/TDI	ADCI_X0/MI_RX/MDO/EIUC_23_X/CANTX/GPIO96/PF0	122	(SW1_SW2)	PF0 [12]
[10] PC1	<< (TD0)	149	PC1/GPIO33/TD0/RVSD	ADCI_S7/EIRO14/CANRX/MI_RX/CLK/EIUC_24_X/GPIO97/PF1	116	(GPIO)	PF1 [12]
[11] PC2	<< (HSB_CLK)	159	PC2/GPIO34/DSCLK_1/CAN4TX/EUOC_22_X/SSCM_DBG0/EIRO5/ULPI0_CLK	LIN1TX/CAN7X/DSCLK_3/EIUC_11_H/GPIO98/PF2	15	(GPIO)	PF2 [15]
[11] PC3	<< (LSD3)	144	PC3/GPIO35/DCS0_1/ADCO_MAO/EUOC_23_X/SSCM_DBG1/CAN1RX/CAN2RX/EIRO6/ULPI0_DIR	CAN1RX/WKPUI7/EUOC_1_Y/DCS0_3/EIUC_12_H/GPIO99/PF3	14	(GPIO)	PF3 [15]
[14] PC4	<< (HSB_TX)	158	PC4/GPIO36/EIUC_31_Y/FR_B_TX_EN/SD_DAT0/ULPI0_D1/SSCM_DBG2/DSN1_1/CANRX/EIRO7	LIN10TX/DSN1_1/LIN10TX/EIUC_13_H/GPIO100/PF4	13	(GPIO)	PF4 [15]
[15] PC5	<< (GPIO)	44	PC5/GPIO37/DSOUT_1/CAN1TX/EUOC_24_X/FR_A_TX/SD_CLK/ULPI0_DS/SSCM_DBG3/EIRO7	LIN10RX/DSN1_3/WKPUI8/EUOC_2_Y/EIUC_14_H/GPIO101/PF5	37	(GPIO)	PF5 [15]
[15] PC6	<< (GPIO)	45	PC6/GPIO38/LIN1TX/EIUC_28_Y/EUOC_17_Y/SSCM_DBG4/CMP0_7	CMP0_1/EUOC_3_Y/CLKOUT1/LIN1TX/EIUC_15_H/GPIO102/PF6	38	(GPIO)	PF6 [15]
[15] PC7	<< (GPIO)	175	PC7/GPIO39/EIUC_29_Y/CMP1_0/EUOC_18_Y/SSCM_DBG5/LIN1RX/WKPUI2	CMP0_0/WKPUI20/LIN1RX/EUOC_2_Y/CLKOUT1/EIUC_30_Y/EIUC_16_H/GPIO103/PF7	34	(GPIO)	PF7 [15]
[10] PC8	<< (HSB_TX)	175	PC8/GPIO40/LIN2TX/EUOC_3_G/SD_DAT6/SSCM_DBG6	EIRO15/CAN7TX/DCS0_2/LIN1TX/EIUC_17_Y/GPIO104/PF8	34	(GPIO)	PF8 [15]
[15] PC9	<< (GPIO)	36	PC9/GPIO41/EUOC_7_G/EUOC_7_Y/SSCM_DBG7/LIN2RX/WKPUI3	CAN7RX/WKPUI21/LIN1RX/EUOC_0_X/DSCLK_2/EIUC_18_Y/GPIO105/PF9	33	(SW1_SW2)	PF9 [15]
[15] PC10	<< (GPIO)	36	PC10/GPIO42/CAN1TX/CAN4TX/ADCO_MAI/CMP0_0	SIN_0/ULPI0_DAE/EIUC_31_Y/EUOC_24_X/GPIO106/PF10	139	(GPIO)	PF10 [11]
[15] PC11	<< (GPIO)	36	PC11/GPIO43/ADCO_MAO2/EUOC_1_Y/CAN1RX/CAN2RX/WKPUI5	ULPI0_D5/CS0_2/CS0_0/EUOC_25_Y/GPIO107/PF11	119	(GPIO)	PF11 [11]
[15] PC12	<< (HSB_TX)	173	PC12/GPIO44/EUOC_12_H/FR_DBG0/SD_DAT4/DSN1_2/EIRO9	ADCI_S2/MI_TX/D2/EUOC_12_Y/SOUT_0/EUOC_26_Y/GPIO108/PF12	115	(GPIO)	PF12 [15]
[13] PC13	<< (HSB_TX)	3	PC13/GPIO45/EUOC_13_H/DSOUT_2/FR_DBG1/SD_DAT5	ADCI_S1/MI_TX/D3/EUOC_13_Y/CLK_0/EUOC_27_Y/GPIO109/PF13	134	(GPIO)	PF13 [15]
[13] PC14	<< (HSB_TX)	3	PC14/GPIO46/EUOC_14_H/DSCLK_2/EUOC_6_Y/FR_DBG2/EIRO8	SIN_2/ULPI0_D0/LIN1TX/EIUC_0_X/GPIO110/PF14	135	(SW1_SW2)	PF14 [11]
[13] PC15	<< (HSB_TX)	4	PC15/GPIO47/EUOC_15_H/DCS0_2/EUOC_5_Y/FR_DBG3/EIRO20	LIN8RX/ULPI0_D1/SOUT_2/EIUC_1_H/GPIO111/PF15	135	(SW1_SW2)	PF15 [11]
[15] PD0	<< (GPIO)	77	PD0/GPI64/ADCI_P6/WKPUI27	ADCI_S3/DSN1_1/MI_RX/TXD1/EUOC_11_Y/EIUC_2_H/GPIO112/PF0	117	(SW1_TXD1)	PF0 [12]
[15] PD1	<< (GPIO)	78	PD1/GPI64/ADCI_P6/WKPUI28	ADCI_S4/MI_RX/TXD2/EUOC_10_Y/DSOUT_1/EIUC_3_H/GPIO113/PF1	118	(SW1_TXD2)	PF1 [12]
[15] PD2	<< (GPIO)	80	PD2/GPI64/ADCI_P6	ADCI_S5/MI_RX/MI_TX_EN/EUOC_9_Y/DSCLK_1/EIUC_4_H/GPIO114/PF2	120	(GPIO)	PF2 [12]
[15] PD3	<< (GPIO)	81	PD3/GPI64/ADCI_P7	ADCI_S6/MI_TX/ERDCS0_1/EIUC_5_H/GPIO115/PF3	162	(GPIO)	PF3 [15]
[15] PD4	<< (GPIO)	82	PD4/GPI64/ADCI_P8	ULPI0_DS/CS1/SOUT_3/EIUC_6_H/GPIO116/PF4	163	(GPIO)	PF4 [15]
[15] PD5	<< (GPIO)	83	PD5/GPI64/ADCI_P9	SIN_3/ULPI0_DS/SDA3/EIUC_7_H/GPIO117/PF5	164	(GPIO)	PF5 [14]
[15] PD6	<< (GPIO)	84	PD6/GPI64/ADCI_P10	ULPI0_D6/ADCI_MAO/ADCO_MAO/DCS3_2/EIUC_8_H/GPIO118/PF6	165	(GPIO)	PF6 [15]
[15] PD7	<< (GPIO)	84	PD7/GPI64/ADCI_P11	ULPI0_D7/ADCI_MAI/CS0_3/ADCO_MAI/DCS3_2/EIUC_9_H/GPIO119/PF7	165	(GPIO)	PF7 [15]
[15] PD8	<< (GPIO)	84	PD8/GPI64/ADCI_P12	SD_WP/SD_RST/ADCI_MAO/ADCO_MAO/DCS2_2/EIUC_10_H/GPIO120/PF8	155	(SW)	PF8 [15]
[15] PD9	<< (GPIO)	85	PD9/GPI64/ADCI_P13	TCK/RVSD/GPIO121/PF9	140	(GPIO)	PF9 [10]
[15] PD10	<< (GPIO)	85	PD10/GPI64/ADCI_P14	TMS/RVSD/GPIO122/PF10	140	(GPIO)	PF10 [10]
[15] PD12	<< (GPIO)	100	PD12/GPIO60/DCSS_0/EUOC_24_X/ADCO/ADCO_S4	ULPI0_D6/EIUC_5_H/CS0_0/DSOUT_3/GPIO123/PF11	141	(SW1_TXD1)	PF11 [11]
[15] PD13	<< (GPIO)	102	PD13/GPIO61/DCS0_1/EUOC_25_Y/ADCO_S5	ULPI0_D7/EIUC_26_Y/CS1_0/DSCLK_3/GPIO124/PF12	9	(GPIO)	PF12 [11]
[15] PD14	<< (GPIO)	104	PD14/GPIO62/DCS1_1/EUOC_26_Y/FR_DBG0/MLBDF/ADCO_S6	EOUT1/EIUC_26_Y/DCS0_3/SOUT_0/GPIO125/PF13	10	(GPIO)	PF13 [14]
[15] PD15	<< (GPIO)	106	PD15/GPIO63/DCS2_1/EUOC_27_Y/FR_DBG1/MLBSF/MLBDA1/ADCO_S7	EN_ERRE/EIUC_27_Y/DCS1_3/CLK_0/GPIO126/PF14	8	(GPIO)	PF14 [15]
[5,10,15] MCU-RSTx	<< (GPIO)	29	RESST	EOUT0/EIUC_17_Y/EUOC_9_Y/SOUT_1/GPIO127/PF15	8	(GPIO)	PF15 [15]
[5] PORSTx	<< (GPIO)	153	RESST				
[6] MCU-XTAL	<< (GPIO)	56	XTAL				
[6] MCU-EXTAL	<< (GPIO)	58	EXTAL				


Calypso 176QFF

PACKAGE 10F3 GPIO PINS

PCP5748GSKM4U6

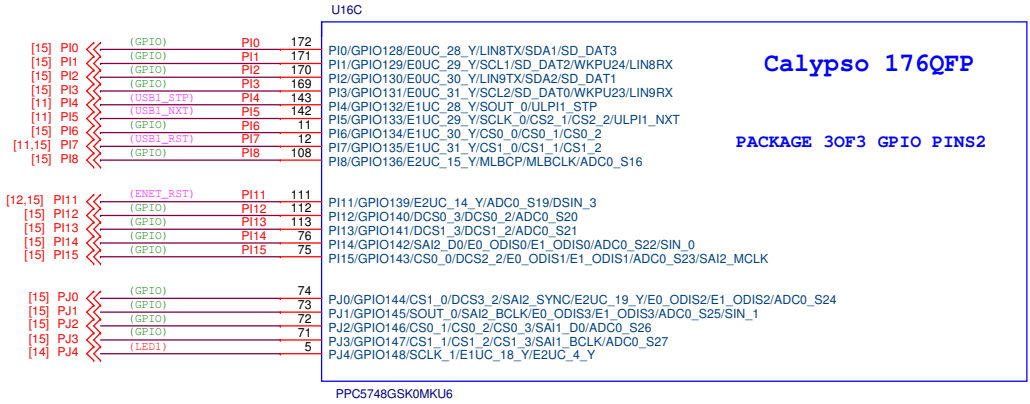
Key to text colours:

Purple	- Connect Physical Interfaces
Orange	- Other Peripherals and I/O
Blue	- Debug (JTAG & Hexus)
Black	- Clock, Reset and Control
Red	- I/O Matrix and other Functions (eg LED)
Green	- I/O Matrix (dedicated)

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Approved:	Size	Document Number	Rev B
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# Calypso GPIO 2 of 2

Key to text colours:  
 Purple - Comms Physical Interfaces  
 Orange - Other Peripherals and I/O  
 Blue - Debug (JTAG & Nexus)  
 Black - Clock, Reset and Control  
 RED - I/O Matrix and other functions (eg LED)  
 Green - I/O Matrix (dedicated)



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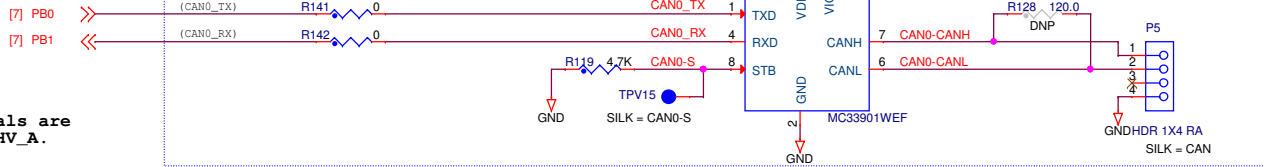
# CAN & LIN Physical

## CAN0 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)

VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V

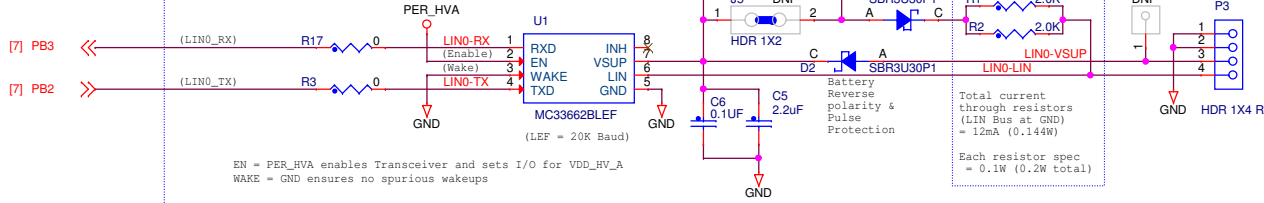
STB - High for Standby mode, pulled low for normal mode.



All CAN and LIN signals are in power domain VDD\_HV\_A.

All interfaces will work at 3.3V or 5.0V (PER\_HVA)

## LIN0 Physical Interface



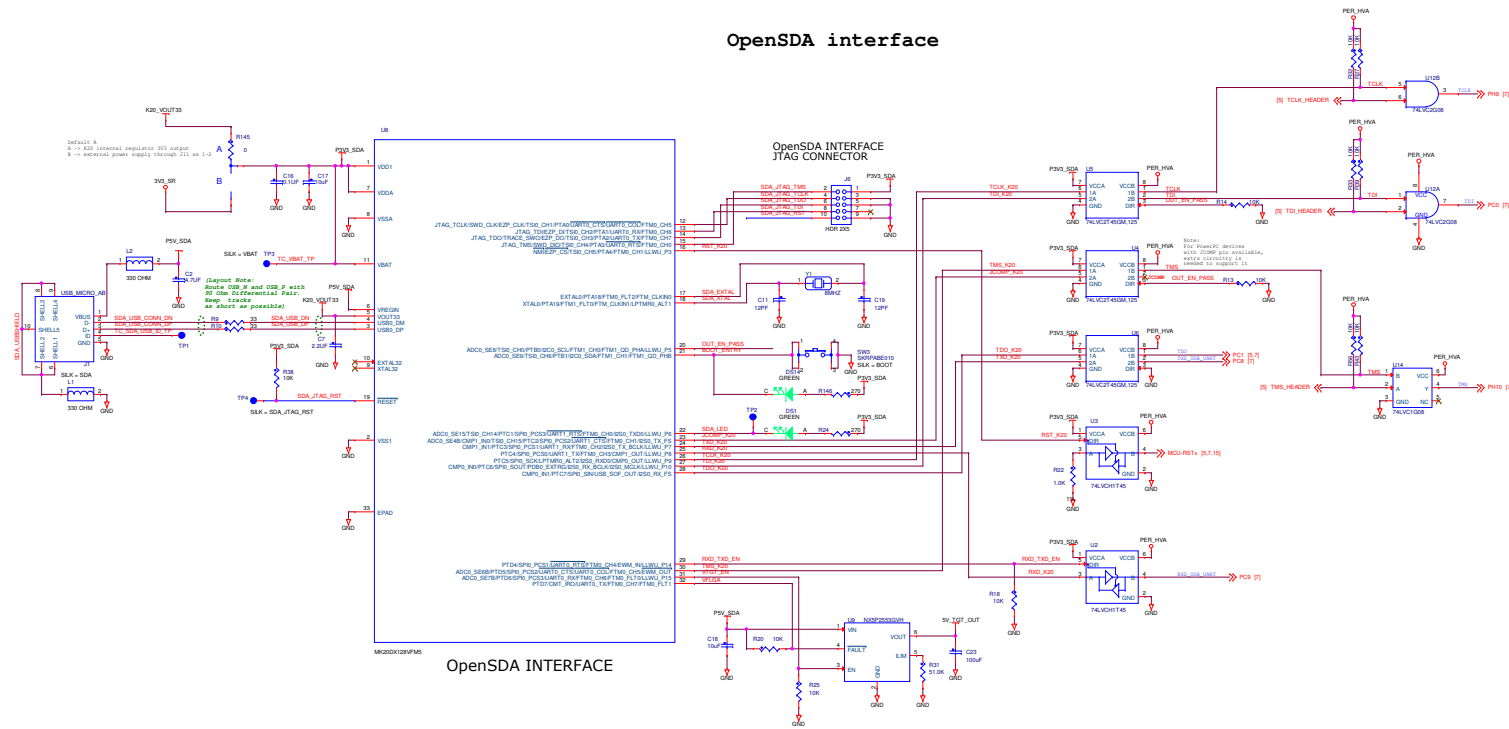
MC33662LEF LIN transceiver is newer version of 33661 offering:

- Full LIN compliance (33661 no longer compliant)
- Improved ESD protection on LIN pin up to 15KV
- Improved ESD on Wake and VSUP Pins
- Other EMC and performance improvements

See freescale.com for more details

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# OpenSDA interface



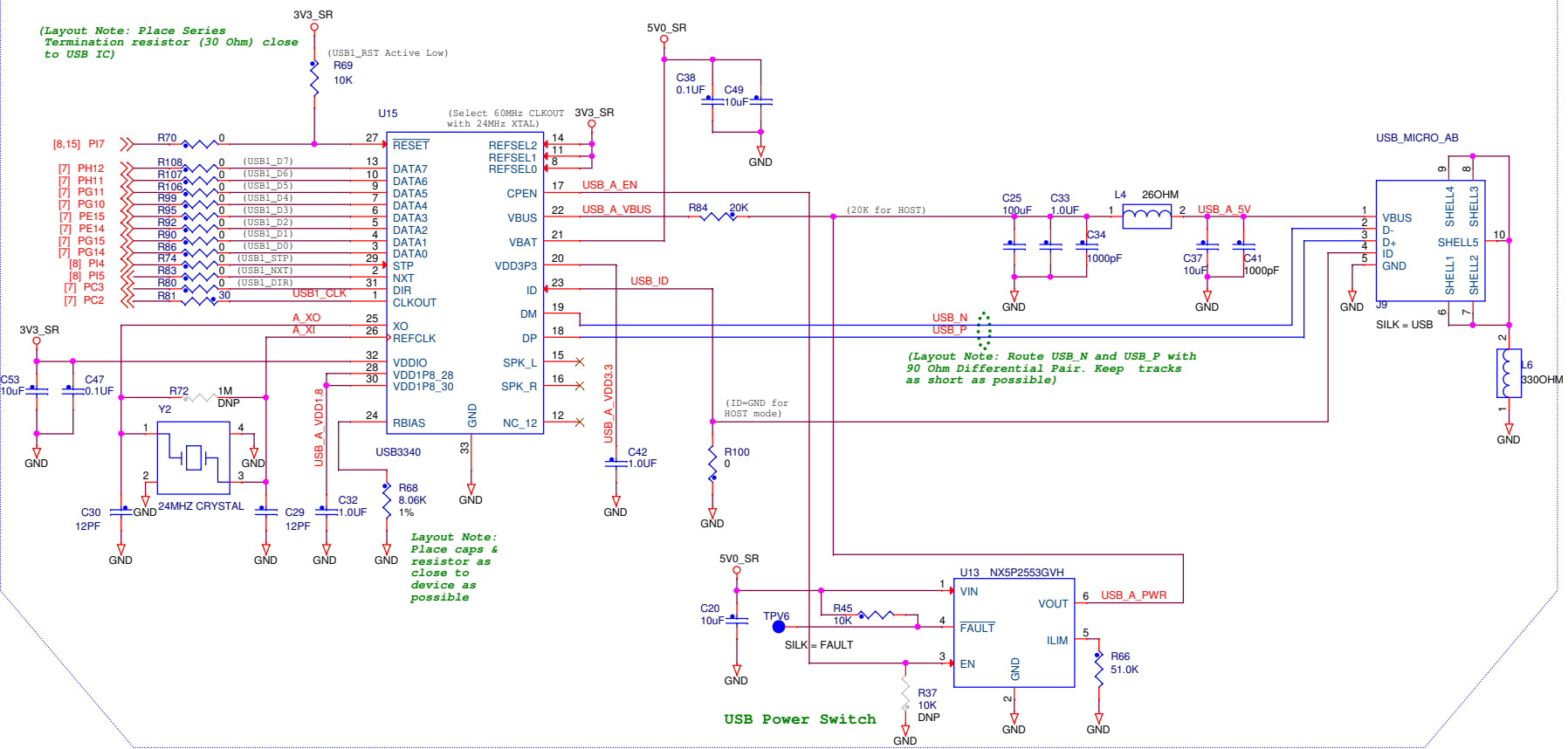
OpenSDA INTERFACE

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		<b>OpenSDA</b>	
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		SCM-09000	PDF-09000
Date:	Iteration:	Rev.:	Doc. No.:
		1.0	1.0

# USB (Type A Host and Type AB OTG)

USB Signals are in power domain VDD\_HV\_A

The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD\_HVA is set to 5V, USB MCU pads must be left as tri-state with no pullups or series resistors to be removed



(Layout Note: Place Series Termination resistor (30 Ohm) close to USB IC)

(USB1\_RST Active Low)

(Select 60MHz CLKOUT with 24MHz XTAL)

(Layout Note: Route USB\_N and USB\_P with 90 Ohm Differential Pair. Keep tracks as short as possible)

Layout Note: Place caps & resistor as close to device as possible

General Layout Note. Recommendation is to keep all tracks between MCU and USB PHI less than 3"

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Approved:	Size Document Number <b>USB Type A / Type AB</b>		
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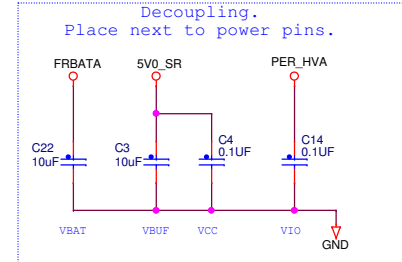
# FlexRAY Physical Interface

All Signals are in power domain VDD\_HV\_A.

FlexRAY interface will work at 3.3V or 5.0V (PER\_HVA)

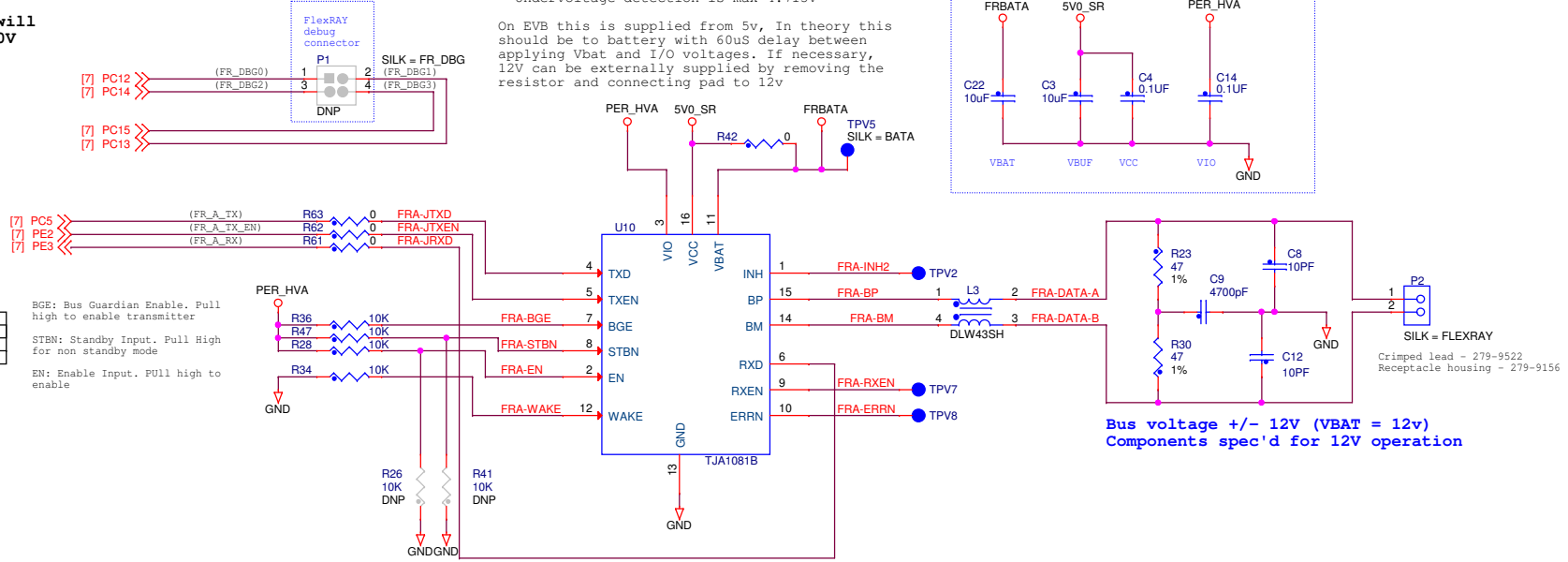
Note on VBAT:  
 - Operational range is 4.45V to 60V  
 - Undervoltage detection is max 4.715V

On EVB this is supplied from 5v, In theory this should be to battery with 60uS delay between applying Vbat and I/O voltages. If necessary, 12V can be externally supplied by removing the resistor and connecting pad to 12v



MODE	EN	STBN
Normal	1	1
Rec Only	0	1
Go to Sleep	1	0
Sleep	0	0

BGE: Bus Guardian Enable. Pull high to enable transmitter  
 STBN: Standby Input. Pull High for non standby mode  
 EN: Enable Input. Pull high to enable



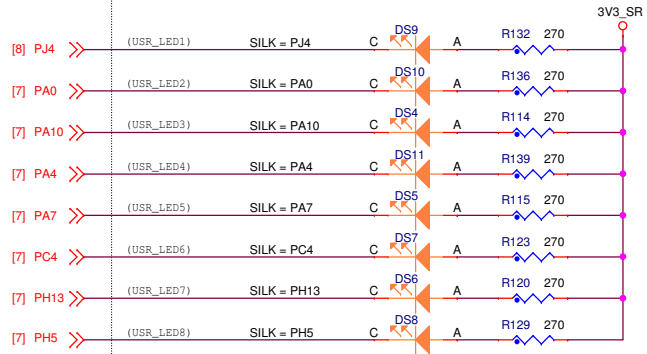
Bus voltage +/- 12V (VBAT = 12v)  
 Components spec'd for 12V operation

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Date: Thursday, July 21, 2016		Rev B	
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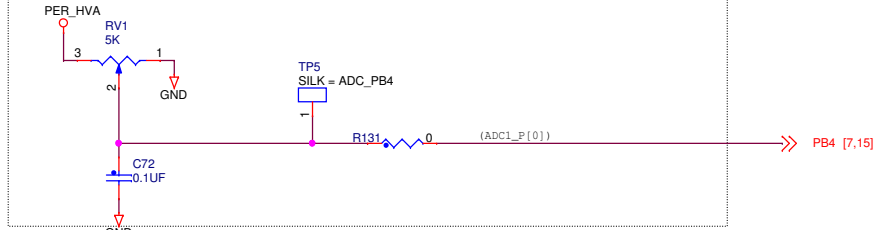
# User Peripherals (Led's, Switches and ADC Pot)

Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage)  
 Similarly, the LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains  
 The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage

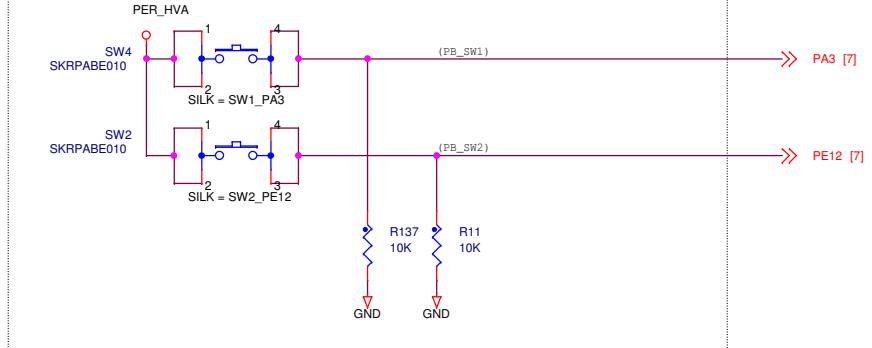
## User LED's (Active Low)



## ADC Input Pot and Test Point



## User Pushbutton Switches (Active High)



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