# SY54023AR

## Low Voltage 1.2V/1.8V CML 2x2 Crosspoint Switch 3.2Gbps, 3.2GHz

## General Description

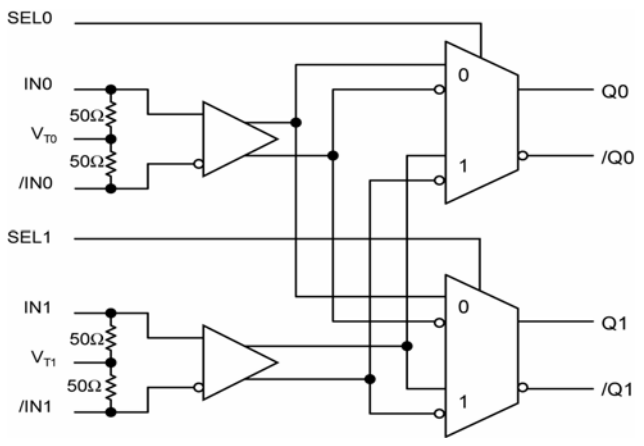
The SY54023AR is a fully differential, low voltage 1.2V/1.8V CML 2x2 Crosspoint. The SY54023AR can process clock signals as fast as 3.2GHz or data patterns up to 3.2Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled from a 2.5V driver) as small as 100mV (200mV$_{pp}$) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an internal voltage reference is provided to bias the $V_T$ pin. The outputs are 400mV CML, with extremely fast rise/fall times guaranteed to be less than 95ps.

The SY54023AR operates from a 2.5V ±5% core supply and a 1.8V or 1.2V ±5% output supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). The SY54023AR is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

## Functional Block Diagram




**Precision Edge®**

## Features

- 1.2V/1.8V CML 2x2 Crosspoint Switch
- Guaranteed AC performance over temperature and voltage:
  - DC-to- > 3.2Gbps throughput
  - <310ps propagation delay (IN-to-Q)
  - <15ps Output skew
  - <95ps rise/fall times
- Ultra-low jitter design
  - <1ps$_{RMS}$ cycle-to-cycle jitter
  - <10ps$_{PP}$ total jitter
  - <1ps$_{RMS}$ random jitter
  - <10ps$_{PP}$ deterministic jitter
- High-speed CML outputs
- 2.5V ±5% , 1.8/1.2V ±5% power supply operation
- Industrial temperature range: –40°C to +85°C
- Available in 16-pin (3mm x 3mm) MLF® package

## Applications

- Data Distribution: OC-48, OC-48+FEC
- SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

## Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Access
- Metro area network equipment

Precision Edge is a registered trademark of Micrel, Inc.
MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology.

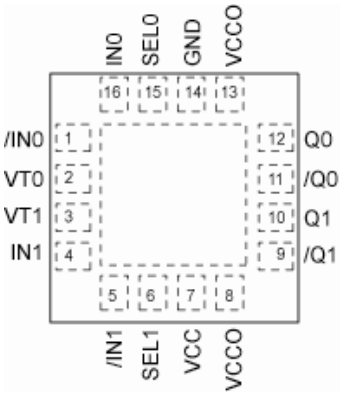
## Ordering Information[1]

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---|---|---|---|---|
| SY54023ARMG | MLF-16 | Industrial | 023A with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY54023ARMGTR[2] | MLF-16 | Industrial | 023A with Pb-Free bar-line indicator | NiPdAu Pb-Free |

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at $T_A$ = 25°C, DC Electricals only.
2. Tape and Reel.

## Pin Configuration




**16-Pin MLF® (MLF-16)**

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 16,1<br>4,5 | IN0, /IN0<br>IN1,/IN1 | Differential Inputs: These input pairs are the differential signal inputs to the device. They accept differential signals as small as 100mV (200mV$_{PP}$). Each input pin internally terminates with 50Ω to the VT pin. |
| 2<br>3 | VT0<br>VT1 | Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. An internal high impedance resistor divider biases VT to allow input AC-coupling. For AC-coupling, bypass VT with a 0.1µF low ESR capacitor to VCC. See “Interface Applications” subsection and Figure 2a. |
| 15<br>6 | SEL0<br>SEL1 | These single-ended TTL/CMOS-compatible inputs select the inputs to the crosspoint switch. Note that this input is internally connected to a 25k ohm pull-up resistor and will default to a logic HIGH state if left open. |
| 7 | VCC | Positive Power Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the $V_{CC}$ pin as possible. Supplies input and core circuitry. |
| 8,13 | VCCO | Output Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the $V_{CCO}$ pins as possible. Supplies the output buffer. |
| 14 | GND,<br>Exposed pad | Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pin. |
| 12,11<br>10,9 | Q0, /Q0<br>Q1, /Q1 | CML Differential Output Pairs: Differential buffered copy of the input signal. The output swing is typically 390mV. See “Interface Applications” subsection for termination information. |

## Truth Table

| SEL0 | SEL1 | Q0 | Q1 |
|---|---|---|---|
| L | L | IN0 | IN0 |
| L | H | IN0 | IN1 |
| H | L | IN1 | IN0 |
| H | H | IN1 | IN1 |

## Absolute Maximum Ratings[1]

Supply Voltage ($V_{CC}$) ..... –0.5V to +3.0V
Supply Voltage ($V_{CCO}$) ..... –0.5V to +2.7V
$V_{CC}$ - $V_{CCO}$ ..... <1.8V
$V_{CCO}$ - $V_{CC}$ ..... <0.5V
Input Voltage ($V_{IN}$) ..... –0.5V to $V_{CC}$ + 0.5V
CML Output Voltage ($V_{OUT}$) ..... 0.6V to $V_{CCO}$+0.5V
Current ($V_T$)
Source or sink current on VT pin ..... ±100mA
Input Current
Source or sink current on (IN, /IN) ..... ±50mA
Maximum operating Junction Temperature ..... 125°C
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature ($T_s$) ..... –65°C to +150°C

## Operating Ratings[2]

Supply Voltage ($V_{CC}$) ..... 2.375V to 2.625V
($V_{CCO}$) ..... 1.14V to 1.9V
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Package Thermal Resistance[3]
MLF®
Still-air ($\theta_{JA}$) ..... 75°C/W
Junction-to-board ($\psi_{JB}$) ..... 33°C/W

## DC Electrical Characteristics[4]

$T_A$ = –40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage Range | $V_{CC}$<br>$V_{CCO}$<br>$V_{CCO}$ | 2.375<br>1.14<br>1.7 | 2.5<br>1.2<br>1.8 | 2.625<br>1.26<br>1.9 | V<br>V<br>V |
| $I_{CC}$ | Power Supply Current | Max. $V_{CC}$ | | 37 | 50 | mA |
| $I_{CCO}$ | Power Supply Current | No Load. $V_{CCO}$ | | 32 | 42 | mA |
| $R_{IN}$ | Input Resistance<br>(IN-to-$V_T$, /IN-to-$V_T$ ) | | 45 | 50 | 55 | Ω |
| $R_{DIFF_IN}$ | Differential Input Resistance<br>(IN-to-/IN) | | 90 | 100 | 110 | Ω |
| $V_{IH}$ | Input HIGH Voltage<br>(IN, /IN) | IN, /IN | 1.2 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage<br>(IN, /IN) | $V_{IL}$ with $V_{IH}$ = 1.2V | 0.2 | | $V_{IH}$–0.1 | V |
| $V_{IH}$ | Input HIGH Voltage<br>(IN, /IN) | IN, /IN | 1.14 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage<br>(IN, /IN) | $V_{IL}$ with $V_{IH}$ = 1.14V, (1.2V-5%) | 0.66 | | $V_{IH}$–0.1 | V |
| $V_{IN}$ | Input Voltage Swing<br>(IN, /IN) | see Figure 3a | 0.1 | | 1.0 | V |
| $V_{DIFF_IN}$ | Differential Input Voltage Swing<br>(\|IN - /IN\|) | see Figure 3b | 0.2 | | 2.0 | V |
| $V_{T_IN}$ | Voltage from Input to $V_T$ | | | | 1.28 | V |

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. $\psi_{JB}$ and $\theta_{JA}$ values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## CML Outputs DC Electrical Characteristics[5]

$V_{CCO}$ = 1.14V to 1.26V $R_L$ = 50Ω to $V_{CCO,}$
$V_{CCO}$ = 1.7V to 1.9V, $R_L$ = 50Ω to $V_{CCO}$ or 100Ω across the outputs,
$V_{CC}$ = 2.375V to 2.625V. $T_A$ = –40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $R_L$ = 50Ω to $V_{CCO}$ | $V_{CCO}$-0.020 | $V_{CCO}$-0.010 | $V_{CCO}$ | V |
| $V_{OUT}$ | Output Voltage Swing | See Figure 3a | 300 | 390 | 475 | mV |
| $V_{DIFF_OUT}$ | Differential Output Voltage Swing | See Figure 3b | 600 | 780 | 950 | mV |
| $R_{OUT}$ | Output Source Impedance | | 45 | 50 | 55 | Ω |

## LVTTL/CMOS DC Electrical Characteristics[5]

$V_{CC}$ = 2.5V ±5%; $V_{CCO}$ = 1.14V to 1.26V or 1.7V to 1.9V; $T_A$ = –40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | | -125 | | 30 | µA |
| $I_{IL}$ | Input LOW Current | | -300 | | | µA |

**Note:**

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC Electrical Characteristics

$V_{CCO}$ = 1.14V to 1.26V $R_L$ = 50Ω to $V_{CCO,}$
$V_{CCO}$ = 1.7V to 1.9V, $R_L$ = 50Ω to $V_{CCO}$ or 100Ω across the outputs,
$V_{CC}$ = 2.375V to 2.625V. $T_A$ = –40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Frequency | NRZ Data | 3.2 | | | Gbps |
| | | $V_{OUT}$ > 200mV Clock | 3.2 | | | GHz |
| $t_{PD}$ | Propagation Delay IN-to-Q | Figure 1a | 150 | 210 | 310 | ps |
| | SEL-to-Q | Figure 1a | 90 | 200 | 350 | ps |
| $t_{Skew}$ | Input-to-Input Skew | Note 6 | | 5 | 20 | ps |
| | Output-to-Output skew | Note 7 | | 3 | 15 | ps |
| | Part-to-Part Skew | Note 8 | | | 75 | ps |
| $t_{Jitter}$ | Data Random Jitter | Note 9 | | | 1 | $ps_{RMS}$ |
| | Deterministic Jitter | Note 10 | | | 10 | $ps_{PP}$ |
| | Clock Cycle-to-Cycle Jitter | Note 11 | | | 1 | $ps_{RMS}$ |
| | Total Jitter | Note 12 | | | 10 | $ps_{PP}$ |
| | Crosstalk Induced Jitter (Adjacent Channel) | Note 13 | | | 0.7 | $ps_{PP}$ |
| $t_R$ $t_F$ | Output Rise/Fall Times (20% to 80%) | At full output swing. | 30 | 60 | 95 | ps |
| | Duty Cycle | Differential I/O | 47 | | 53 | % |

**Notes:**

6. Input-to-Input skew is the difference in time between both inputs, measured at the same output for the same temperature, voltage and transition.
7. Output-to-Output skew is the difference in time between both outputs, receiving data from the same input, for the same temperature, voltage and transition.
8. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
9. Random jitter is measured with a K28.7 pattern, measured at ≤ $f_{MAX}$.
10. Deterministic jitter is measured at 2.5Gbps with both K28.5 and $2^{23}$–1 PRBS pattern.
11. Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
12. Total jitter definition: with an ideal clock input frequency of ≤ $f_{MAX}$ (device), no more than one output edge in $10^{12}$ output edges will deviate by more than the specified peak-to-peak jitter value.
13. Crosstalk induced jitter is defined as the added jitter that results from signals applied to the adjacent channel. It is measured at the output while applying a similar, differential clock frequency to both inputs that is asynchronous with respect to each other.

## Interface Applications

For Input Interface Applications, see Figures 4a through 4f and for CML Output Termination, see Figure 5a through Figure 5d.

### CML Output Termination with VCCO 1.2V

For VCCO of 1.2V, Figure 5a, terminate the output with 50Ω-to-1.2V, DC coupled, not 100Ω differentially across the outputs.

If AC-coupling is used, Figure 5d, terminate into 50Ω-to-1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage.

Do not AC couple with internally terminated receiver. For example, 50Ω ANY-IN input. AC-coupling will offset the output voltage by 200mV and this offset voltage will be too low for proper driver operation. Any unused output pair needs to be terminated when VCCO is 1.2V, do not leave floating.

### CML Output Termination with VCCO 1.8V

For VCCO of 1.8V, Figure 5a and Figure 5b, terminate with either 50Ω-to-1.8V or 100Ω differentially across the outputs. AC- or DC-coupling is fine.

### Input AC Coupling

The SY54023AR input can accept AC-coupling from any driver. Bypass VT with a 0.1µF low ESR capacitor to VCC as shown in Figures 4c and 4d. VT has an internal high impedance resistor divider as shown in Figure 2a, to provide a bias voltage for AC-coupling.

## Timing Diagrams

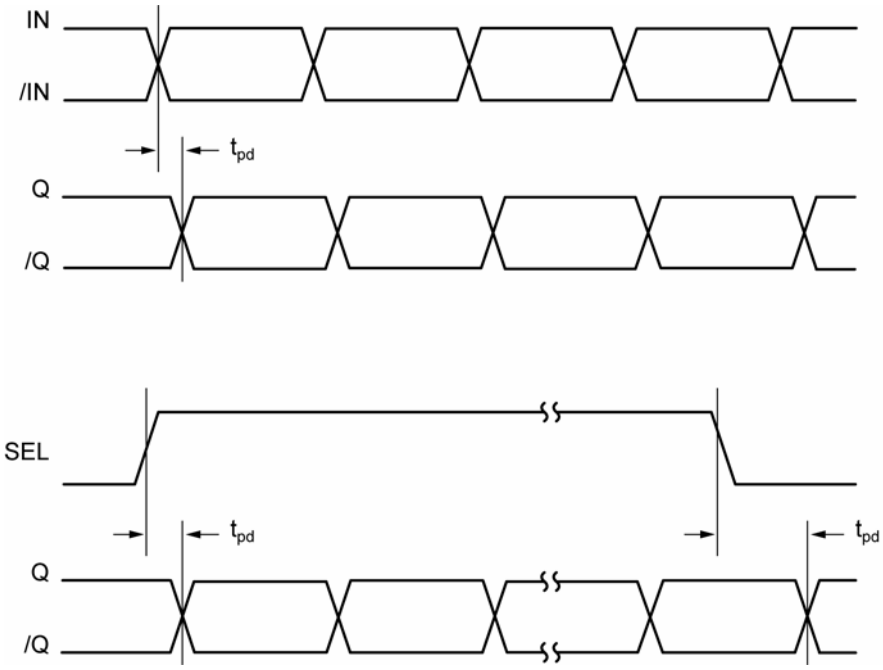
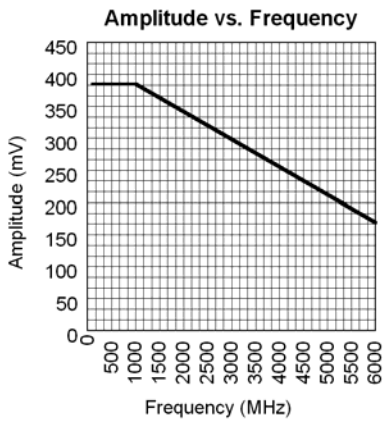
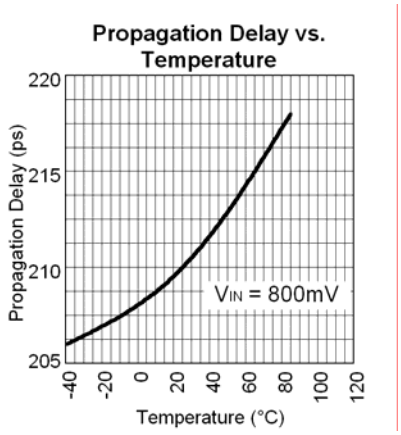



**Figure 1a. Propagation Delay**

## Typical Characteristics

$V_{CC}$ = 2.5V, $V_{CCO}$ = 1.2V GND = 0V, $V_{IN}$ = 100mV, $R_L$ = 50Ω to 1.2V, $T_A$ = 25°C, unless otherwise stated.

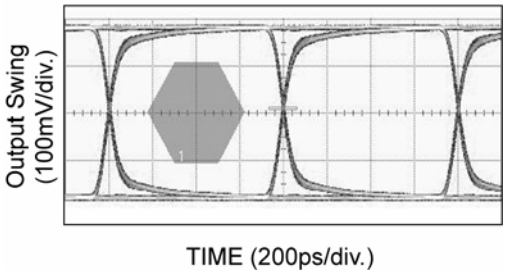


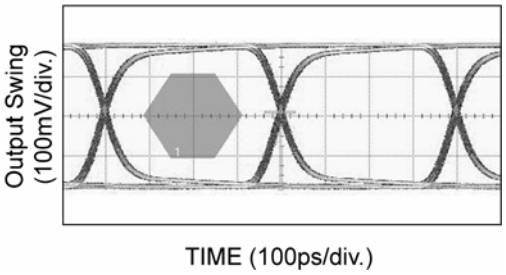
## Functional Characteristics

$V_{CC}$ = 2.5V, $V_{CCO}$ =1.2V GND = 0V, $V_{IN}$ = 400mV, $R_L$ = 50Ω to 1.2V, Data Pattern: $2^{23}$-1, $T_A$ = 25°C, unless otherwise stated.

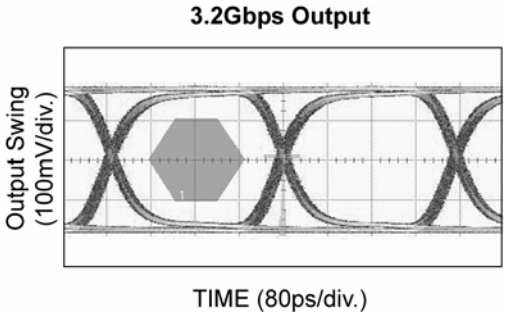
**1.25Gbps Output**




**2.5Gbps Output**



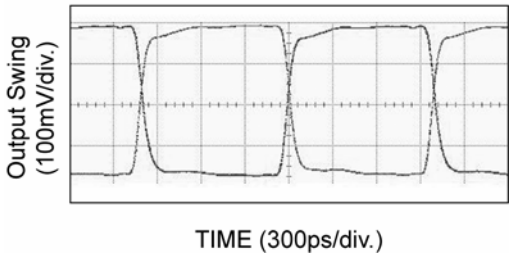

**3.2Gbps Output**



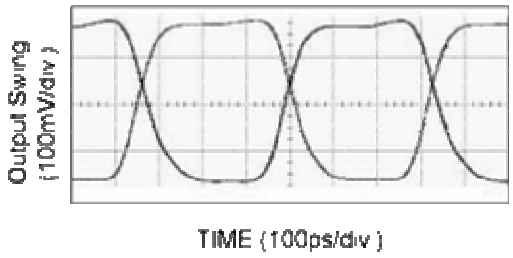
## Functional Characteristics

$V_{CC}$ = 2.5V, $V_{CCO}$ =1.2V GND = 0V, $V_{IN}$ = 400mV, $R_L$ = 50Ω to 1.2V, $T_A$ = 25°C, unless otherwise stated.

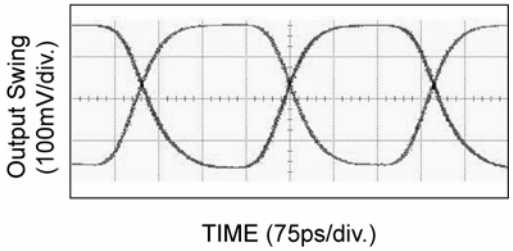
**500MHz Output**



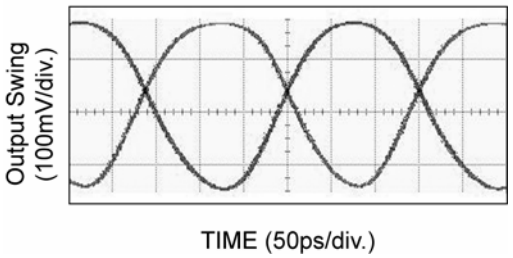

**1.5GHz Output**




**2GHz Output**




**3.2GHz Output**



## Input and Output Stage

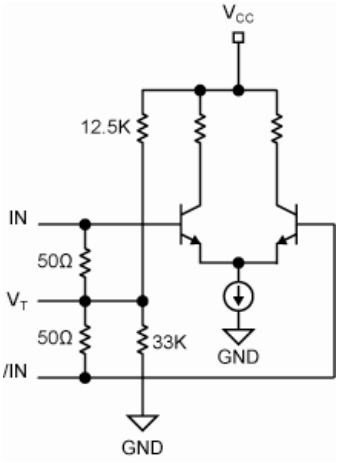



**Figure 2a. Simplified Differential Input Buffer**

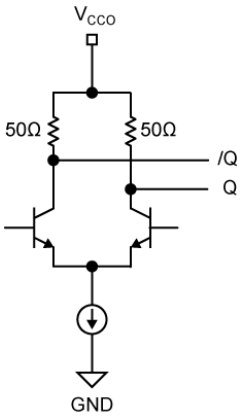



**Figure 2b. Simplified CML Output Buffer**

## Single-Ended and Differential Swings

**Figure 3a. Single-Ended Swing**

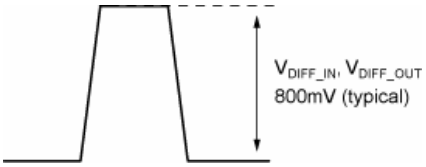



**Figure 3b. Differential Swing**

## Input Interface Applications

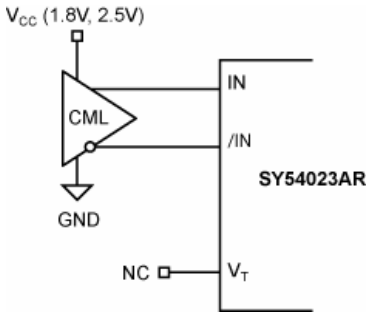



**Figure 4a. CML Interface (DC-Coupled, 1.8V, 2.5V)**

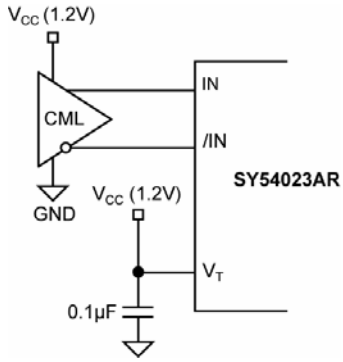



**Figure 4b. CML Interface (DC-Coupled, 1.2V)**

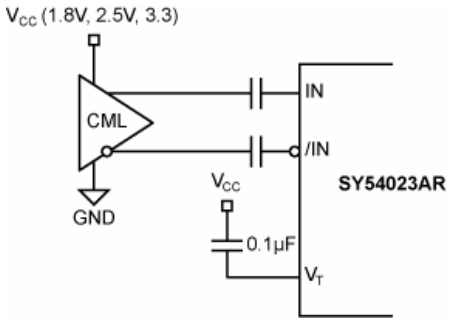



**Figure 4c. CML Interface (AC-Coupled)**

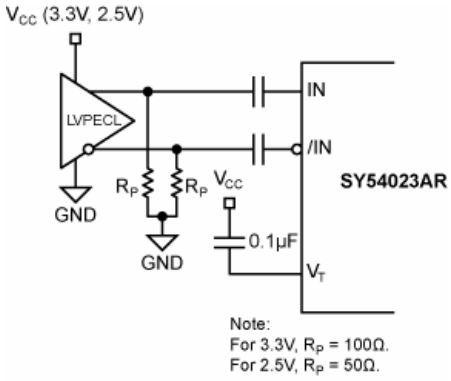



**Figure 4d. LVPECL Interface (AC-Coupled)**

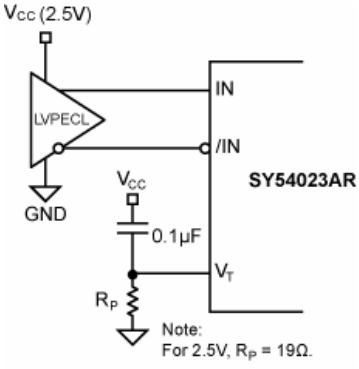



**Figure 4e. LVPECL Interface (DC-Coupled)**

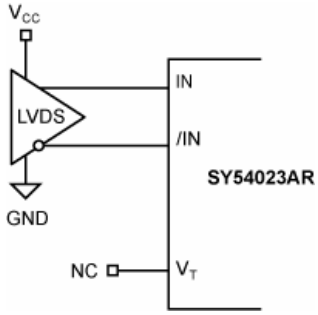



**Figure 4f. LVDS Interface**

## CML Output Termination

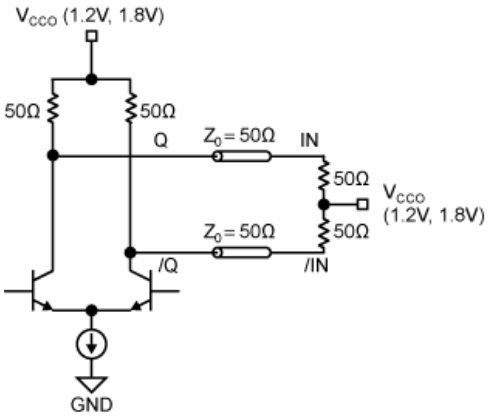



**Figure 5a. 1.2V or 1.8V CML DC-Coupled Termination**

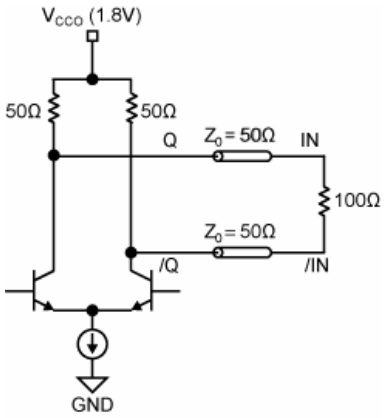



**Figure 5b. 1.8V CML DC-Coupled Termination**

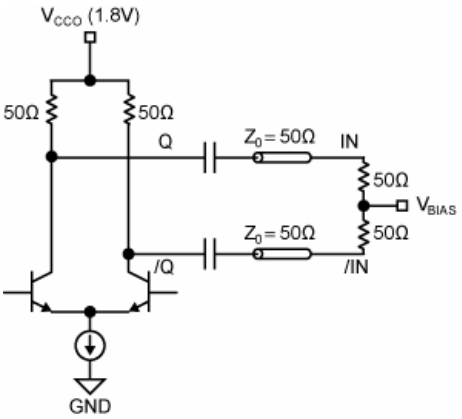



**Figure 5c. CML AC-Coupled Termination ($V_{CCO}$ 1.8V only)**

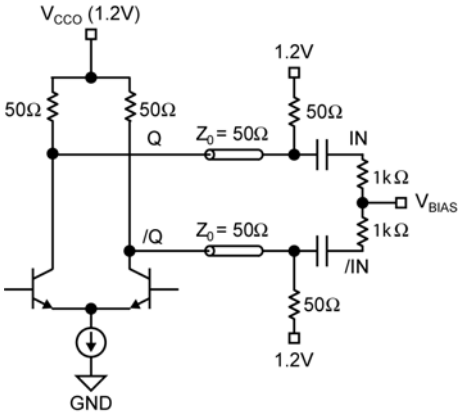
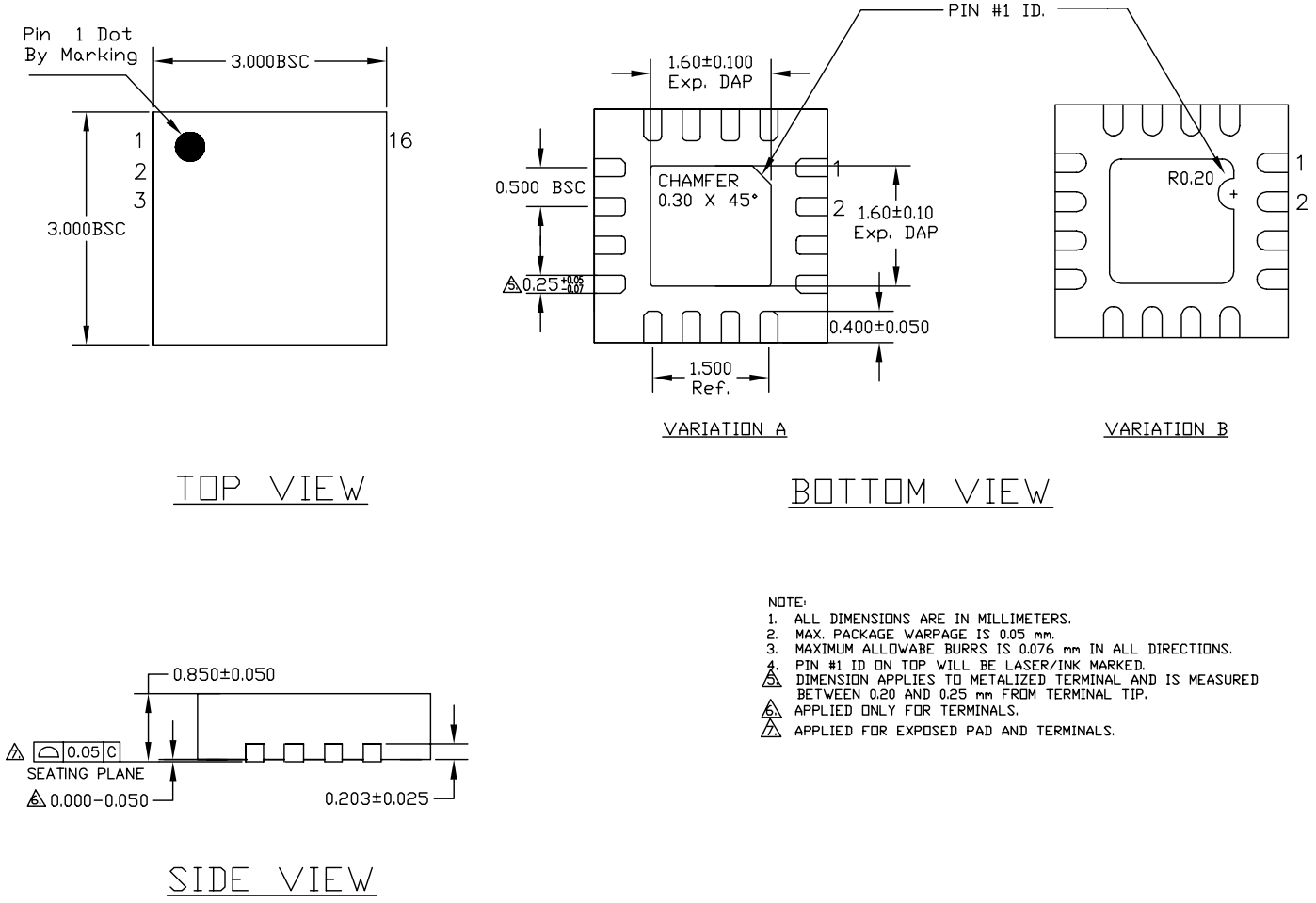



**Figure 5d. CML AC-Coupled Termination ($V_{CCO}$ 1.2V only)**

## Related Product and Support Documents

| Part Number | Function | Datasheet Link |
|---|---|---|
| SY54023R | 3.2Gbps/2.5GHz Precision, 2x2 Low Voltage CML Crosspoint Switch with Internal Termination and Fail Safe Inputs | http://www.micrel.com/page.do?page=/product-info/products/sy54023r.shtml |
| HBW Solutions | New Products and Termination Application Notes | http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml |

## Package Information




**16-Pin MLF® (3mm x3mm) (MLF-16)**

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