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2100AI/AT FW Maintenance Release

PCN: 34670

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Revision History:

Revision 1, 2022-08-19: This document supersedes the original PCN #34670, dated 2022-07-29. The Product Ship Date is being modified from 2022-09-04 to 2022-09-20. This is now reflected in the Product Ship Date field below. No other changes have been made to this notification and all other details remain the same.

Type:	Firmware Revision
Description:	Release to production of MU05 FW for 2100AI/AT SSDs See attached change list for bugs fixed and improvements made Micron plans on shipping 2100 SSDs with FW MU05 immediately. Please contact your Micron Account Team if you have any questions or concerns.
Reason:	Improved Product Quality and Reliability
Product Affected:	All 2100AI and 2100AT SSDs

Affected Micron Part Number	Recommended Replacement	Customer Part Number
COMPONENT		
MTFDHBL064TDP-1AT12AIYY		
MTFDHBL064TDQ-1AT12ATYY		**MTFDHBL064TDQ-1AT12ATYY-ND**
MTFDHBL128TDP-1AT12AIYY		**MTFDHBL128TDP-1AT12AIYY-ND**

MTFDHBL128TDQ-1AT12ATYY		**MTFDHBL128TDQ-1AT12ATYY-ND**
MTFDHBL256TDP-1AT12AIYY		**MTFDHBL256TDP-1AT12AIYY-ND**
MTFDHBL256TDQ-1AT12ATYY		**MTFDHBL256TDQ-1AT12ATYY-ND**
MTFDHBL512TDP-1AT12AIYY		**MTFDHBL512TDP-1AT12AIYY-ND**
MTFDHBL512TDQ-1AT12ATYY		**MTFDHBL512TDQ-1AT12ATYY-ND**
MTFDHBM1T0TDP-1AT12AIYY		**MTFDHBM1T0TDP-1AT12AIYY-ND**
MTFDHBM1T0TDQ-1AT12ATYY		**MTFDHBM1T0TDQ-1AT12ATYY-ND**
MODULE		
MTFDHBK064TDP-1AT12AIYY		
MTFDHBK128TDP-1AT12AIYY		
MTFDHBK1T0TDP-1AT12AIYY		**MTFDHBK1T0TDP-1AT12AIYY-ND**
MTFDHBK1T0TDQ-1AT12ATYY		
MTFDHBK256TDP-1AT12AIYY		**MTFDHBK256TDP-1AT12AIYY-ND**
MTFDHBK512TDP-1AT12AIYY		**MTFDHBK512TDP-1AT12AIYY-ND**

*Materials that have been ordered are in **bold**.

Method of Identification:	FW ID: MU05; BGA: Send IDENTIFY command to the drive, Reference Bytes (71:64) from the IDENTIFY response; M.2: On label
Micron Sites Affected:	Fab10N - SG Fab10W - SG MSB - Singapore
Product Ship Date:	2022-09-20

NOTE: Per JEDEC Standard J-STD-046 Section 3.2.3; lack of acknowledgment of this PCN within 30 days constitutes acceptance of change.

Thank you

Introduction

The following is a list of changes and fixes for Micron's 2100AI/AT PCIe NVMe NAND Flash family of solid-state drives (SSDs) running firmware revision MU05. This firmware is compatible with all form factors and capacities of the 2100 SSD family. This document should be used in conjunction with the 2100AI/AT PCIe NVMe NAND Flash SSD data sheet which is available on www.micron.com.

All issues listed in Table 1 are resolved in MU05 and newer firmware.

Firmware Revision Identification

Determine the firmware revision by using nvme CLI (command line interface) or Micron Storage Executive tool (found on www.micron.com):

```
user@system:~$ sudo nvme id-ctrl /dev/nvme0
NVME Identify Controller:
...
fr : MU05
...
```

Summary of Issues Fixed

Table 1: Issue Descriptions and Details

Issue #:	Description:	Details:
1	UNH IOL NVMe v16a compliance improvements	Various bug fixes found during UNH IOL NVME compliance testing.[R1]
2	ULINK TCG v8 compliance improvements	Various bug fixes found during ULINK TCG compliance testing.[R2]
3	ULINK NVMe Protocol v4.0 improvements	Various bug fixes found during ULINK NVMe Protocol v4.0 compliance testing.[R3]
4	Improved voltage loss protection during SSD power up	Increased the robustness of voltage loss protection in the firmware boot process. This was done to address a single customer device which encountered an unrealistic stress test violating the datasheet specification.
5	Improved SLC block resource management for dynamic cache usage	Improved handling of the SLC blocks used in the dynamic cache. In this rare case, back-to-back power cycles could cause the SSD to enter write protect mode.[R4]
6	Temporary unresponsiveness of SSD due to Host Memory Buffer (HMB) data corruption	Drive firmware can better handle corrupted non-user data in host memory when HMB is in use. User data is not exposed to this issue. [1]
7	Feature enhancement to support light throttling with Host Controller Thermal Management (HCTM)	The throttling feature has been improved by adding the capability of light throttling. There is no impact to customers not setting HCTM feature. [1]
8	Garbage collection may lead to unresponsive drive	Fixed an issue where garbage collection could cause SRAM memory contention which may corrupt the encryption key. Corruption of the key will cause an unresponsive drive because data can no longer be decoded whether OPAL is enabled or disabled.

9	LED behavior has been stabilized to 2Hz when active.	Improved the stability of the LED blink rate when SSD is active (2Hz).
10	#PERST affecting PCIe physical layer stability	Improved PERST# timing to improve link negotiation at the physical layer on specific customer systems.
11	SMART Critical Error indicator, Data Units Written, and Available spares may contain over estimated data	Improved SMART reliability in rare corner cases where values displayed are inaccurate or over estimated
12	NVMe error log and interrupt coalescing across lower power state	Improved interrupt coalescing setting and NVMe error log data by making them persistent across PS4.
13	NAND read disturb may occur if host workload is near read only	Garbage collection normally only takes place when a host issues a write to the SSD. However, for workloads which are almost all reads, over time read disturb may occur. For these workloads background garbage collection can be enabled using a set/get feature command. Background garbage collection is disabled by default in MU05 (same as previous firmware).[3]
14	SMART *Superblock Average Erase Count (TLC)* gap between minimum and maximum shows an anomalous gap in the event of an unsafe shutdown	Firmware operation has also been improved to reduce erroneous erase count gap due to power cycling. The host should be designed to prevent unsafe shutdowns.
15	Incorrect LBA range type reported after FFU with older firmware	Fixed an issue where updating from firmware <=MU02 to MU03x or MU04x may cause the LBA Range Type capabilities field to be incorrect.
16	Host may fail to detect SSD	Fixed a corner case issue related to an incorrect NAND timing setting which may cause the SSD to fail to boot properly. This affects only the 512GB and 1TB capacities.
17	SSD may enter write protect mode during PCM configuration	Fixed a corner case issue where the SSD may enter write protect if there is an existing grown bad block when configuring the physical capacity management feature.
18	Customer unique workload combined with a specific physical capacity management configuration may cause the SSD to enter write protect mode	Fixed a specific issue where a workload may exhaust SLC resources and lead to write protect mode. The affected host workload is 90% SLC data and 10% TLC data written concurrently where the 90/10 ratio is maintained over time.
19	Increased the maximum number of supported IO queues for 2100 for most capacities	The maximum number of IO queues supported has been increased in MU05 compared to MU04.3 to the following values: 64GB to 2, 128GB to 4, and 256GB to 8. The 512GB and 1TB capacities remain the same as MU04.3 at 16.

20	Function Level Reset during a Dataset Management – Deallocate command may cause an unresponsive SSD	Fixed a corner case issue where a Function Level Reset (FLR) during a *Dataset Management -- Deallocate* attribute may cause the SSD to become unresponsive.[2]
21	Improved flexibility for SSD Production Programming (SLC Reflow Management)	The Production Programming (SLC Reflow Management) feature can now be used until the average block erase count is <10 *Superblock Average Erase Count (TLC)* erase cycles and the lock command has not been issued to the SSD. Refer to TN-FD-53 for more details.
22	Improved host voltage supply stability detection in SMART attributes	Added a new field to extended SMART log 0xD0. This field will track host power supply droops on PWR_1 (3.3V). See TN-FD-59 for details.
23	TCG Locking Security Provider (SP) session may not start properly	Improved the robustness of internal routines relating to initialization of TCG states.
24	If SSD encounters UECC in metadata, it may hang during power up	Fixed a corner case where the SSD may not power on properly due to the presence of an UECC in metadata. This does not affect user data.
25	Spurious LBA out of range error	Fixed and improved functions for managing HMB data by the firmware after controller resets which could cause an erroneous error to be returned.
26	Lifetime data integrity in the NVM over temperature	Fixed an error in the NAND data integrity management which could lead to UECCs if the SSD *Superblock Average Erase Count (TLC)* is more than 700 cycles.
27	Physical Capacity Management (PCM) does not automatically lock based on the amount of data written to the SSD	Firmware will now automatically lock the SSD's PCM configuration once 10X of the native capacity of data is written to it.
28	Format NVM reports no error on TCG active SSD	Fixed an issue where a NVM Format command is allowed even though the SSD is in a TCG Active state. The format command should be aborted
29	Rapid and numerous Function Level Resets during HMB use can cause SSD to become unresponsive	Improved handling of a corner case where rapid, consecutive function level resets can cause the HMB engine to become unresponsive thus leading to the SSD not responding to the host. This issue was found using a compliance tester and not associated with a customer sighting.
30	Set feature for power management fails during a *Sanitize* operation	Fixed an issue where an invalid field response is sent to the host when issuing a set feature command for power management during a *Sanitize* operation.[1]
31	SSD does not enter Power State 0 when a Device Self-Test is in progress	Fixed an issue where the SSD does not enter PS0 if there is a device self-test (DST) in progress. [1]

32	SSD Firmware returns incorrect error status after IV (interrupt vector) configuration set	Fixed an issue where the SSD firmware may return an invalid error status when the host attempts a set features Interrupt Vector Configuration command.
33	Autonomous Power State Transition (APST) timing may be incorrect after SSD reset	Fixed an issue where the APST entry timing is incorrect after the host resets the SSD. [1]
34	Physical Region Page (PRP) handling improvements	Improved firmware handling of PRP checks on read, write, compare, firmware download, set and get feature commands. [1]
35	Short Drive Self-Test (DST) continues running after controller reset	Fixed an issue where the short device self-test will continue its progress even after a controller reset issued. [1]
36	SSD transitions using APST while Active State Power Management (ASPM) is disabled	Fixed an issue where the SSD may transition power states in APST even though ASPM is disabled by the host.
37	SSD may enter write protect after many unsafe shutdowns	Fixed a corner case issue where the SSD may enter write protect and/or use up spare blocks erroneously when experiencing many unsafe back-to-back power cycles.
38	SSD may timeout in response to host PCIe MRd (Memory Read) commands	Addressed an issue to avoid a false error detected during processing of rapid back-to-back Memory Read commands.

Notes:

(1) Refer to NVM Express™ Revision 1.3c

(2) Linux does not use FLR (Functional Level Reset) although an API is exposed by the NVMe driver. OS boot loader should avoid using FLR.

(3) Please refer to the latest version of the 2100 PCIe NVME NAND Flash SSD Data sheet for instructions on enabling background garbage collection.

References

(R1) https://www.iol.unh.edu/solutions/test-tools/interact

(R2) https://ulinktech.com/products/tcg-storage-certification-test-suite/

(R3) https://ulinktech.com/products/ulink-nvme-test-suites/

(R4) https://www.micron.com/-/media/client/global/documents/products/technical-marketing-brief/brief_ssd_dynamic_write_accel.pdf

Revision History

Rev. A – 6/22/2022

- Initial release