P-Channel Power MOSFET

-20V, -11A, 16mΩ

FEATURES

- Fast Switching
- Suitable for 1.8V drive applications
- RoHS compliant
- Halogen-free according to IEC 61249-2-21

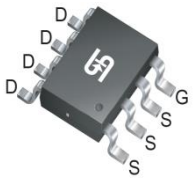
APPLICATIONS

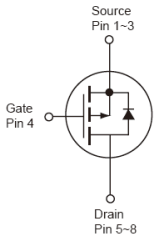
- Load Switch
- Networking

PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		-20	V
$R_{DS(on)}$ (max)	V_{GS} = -4.5V	16	mΩ
	V_{GS} = -2.5V	22	
	V_{GS} = -1.8V	28	
Q_g	V_{GS} = 4.5V	24	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOP-8





Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±10	V
Continuous Drain Current, Silicon limited	T_C = 25°C	I_D	-14	A
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	-11	A
	T_C = 100°C		-7	
Pulsed Drain Current (Note 2)		I_{DM}	-44	A
Total Power Dissipation	T_C = 25°C	P_D	5	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL RESISTANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	25	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	50	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	BV_{DSS}	-20	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	$V_{GS(TH)}$	-0.3	-0.5	-1.0	V
Gate-Source Leakage Current	V_{GS} = ±10V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = -20V	I_{DSS}	--	--	-1	μA
Drain-Source On-State Resistance (Note 3)	V_{GS} = -4.5V, I_D = -6A	$R_{DS(on)}$	--	13	16	mΩ
	V_{GS} = -2.5V, I_D = -4A		--	16	22	
	V_{GS} = -1.8V, I_D = -3A		--	22	28	
Dynamic (Note 4)						
Total Gate Charge	V_{DS} = -10V,I_D = -6A, V_{GS} = -4.5V	Q_g	--	24	--	nC
Gate-Source Charge		Q_{gs}	--	3.4	--	
Gate-Drain Charge		Q_{gd}	--	4	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz	C_{iss}	--	2565	--	pF
Output Capacitance		C_{oss}	--	232	--	
Reverse Transfer Capacitance		C_{rss}	--	120	--	
Switching (Note 5)						
Turn-On Delay Time	V_{GS} = -4.5V, V_{DD} = -10V, I_D = -1A, R_{GEN} = 25Ω	$t_{d(on)}$	--	12	--	ns
Rise Time		t_r	--	18	--	
Turn-Off Delay Time		$t_{d(off)}$	--	153	--	
Fall Time		t_f	--	60	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	V_{GS} = 0V, I_S = -1A	V_{SD}	--	--	-1	V

Notes:

1. Package current limit.
2. Pulsed width limited by maximum junction temperature.
3. Pulse test: Pulse ≤ 300μs, duty cycle ≤ 2%.
4. For DESIGN AID ONLY, not subject to production testing.
5. Switching time is essentially independent of operating temperature.

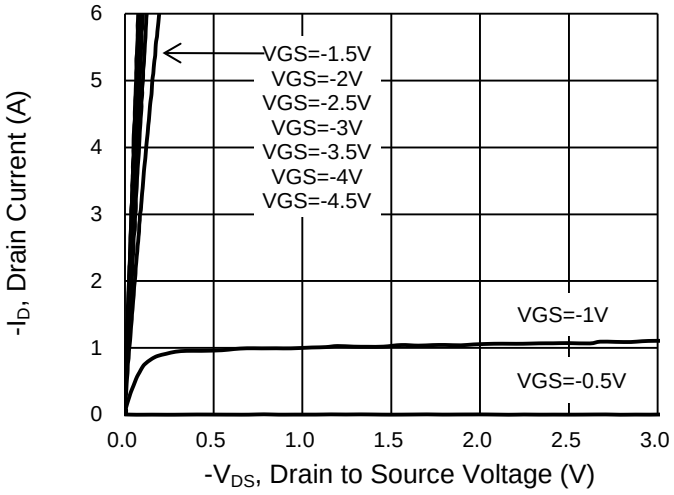
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM160P02CS RLG	SOP-8	2.5Kpcs / 13”Reel

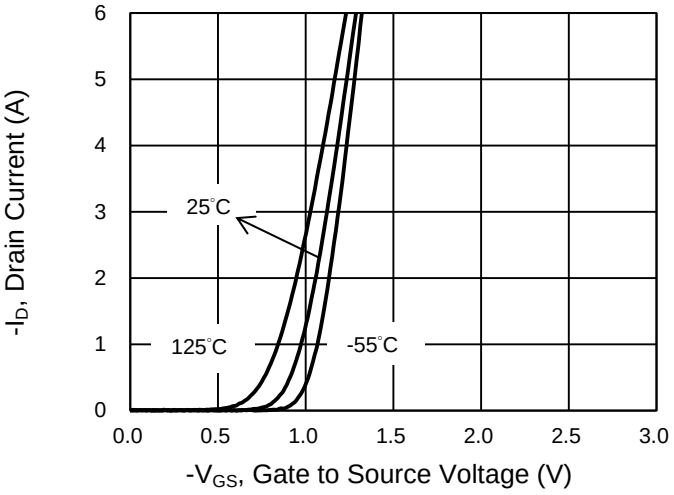
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

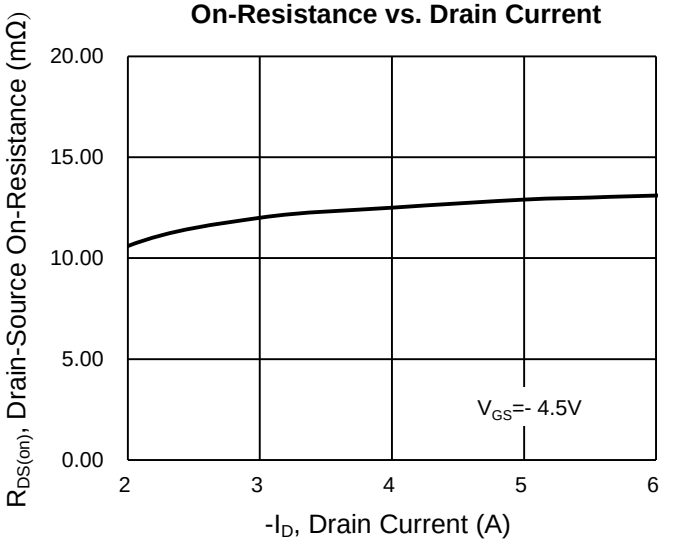
Output Characteristics



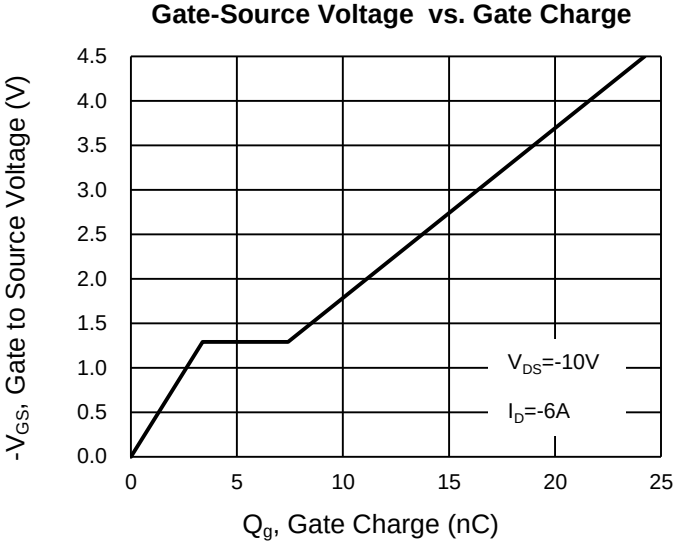
Transfer Characteristics



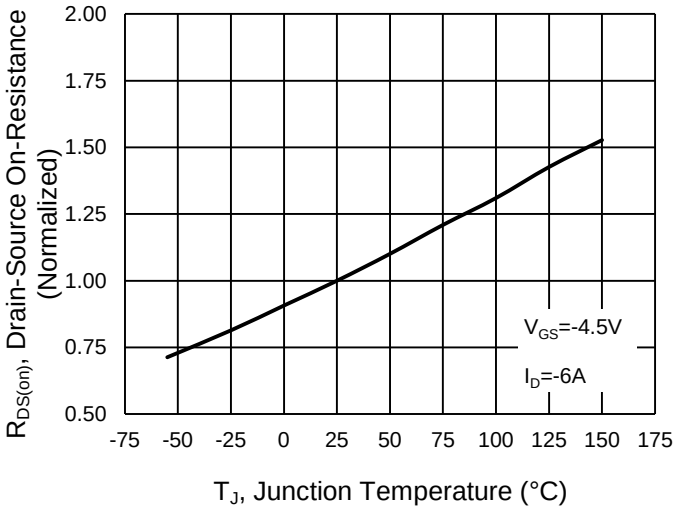
On-Resistance vs. Drain Current



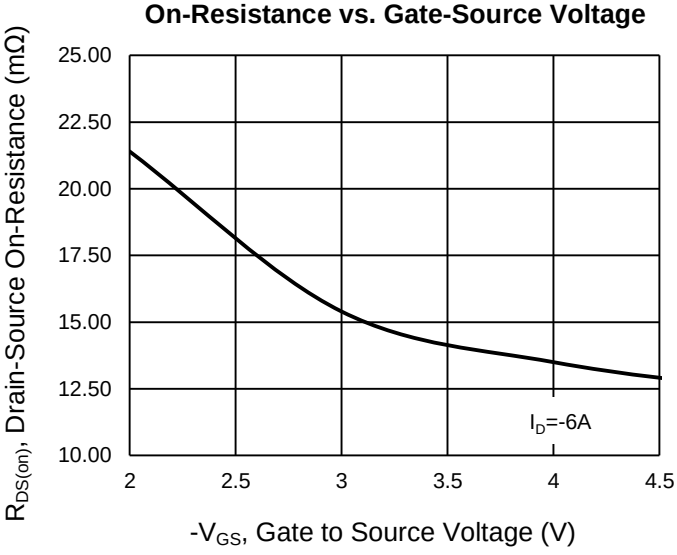
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



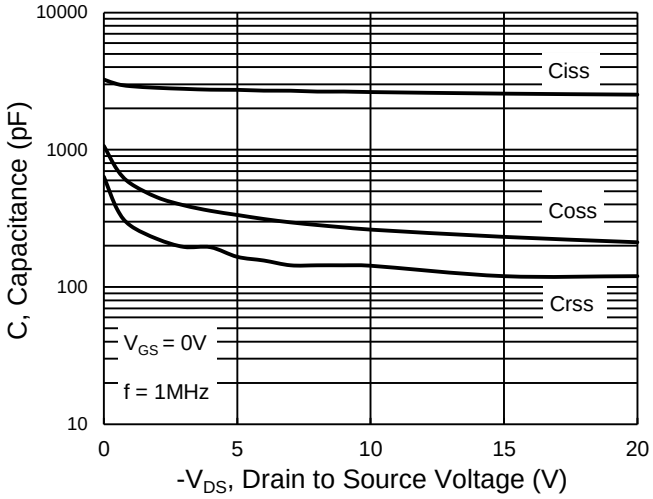
On-Resistance vs. Gate-Source Voltage



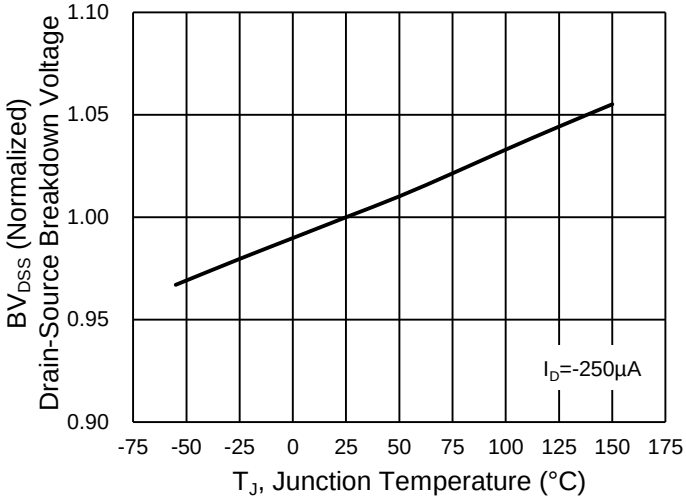
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

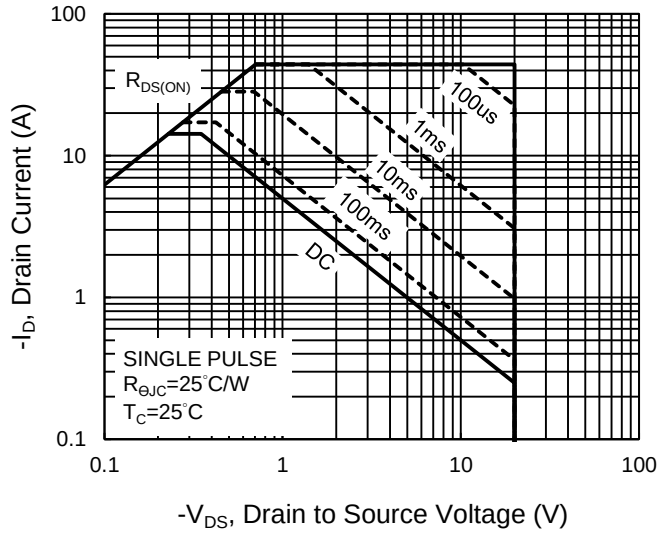
Capacitance vs. Drain-Source Voltage



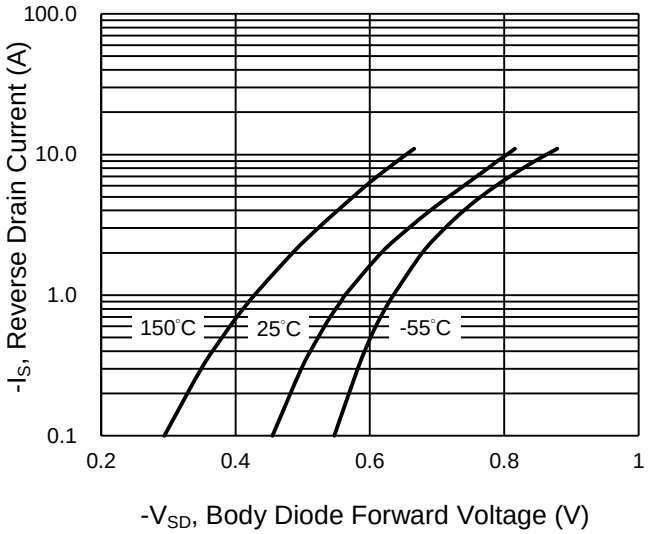
BV_{DSS} vs. Junction Temperature



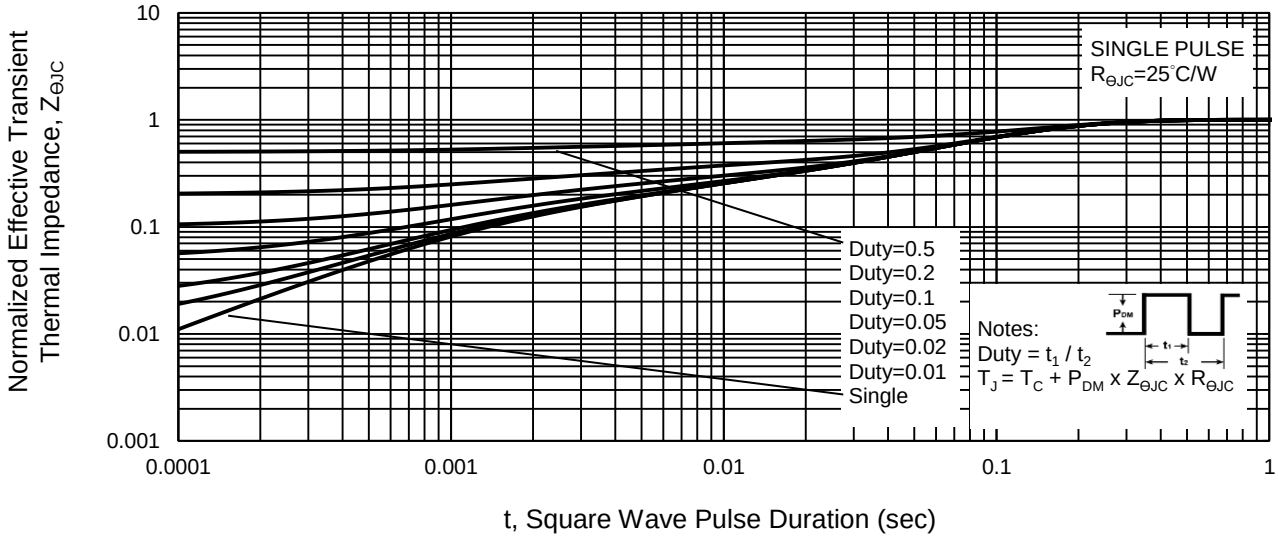
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



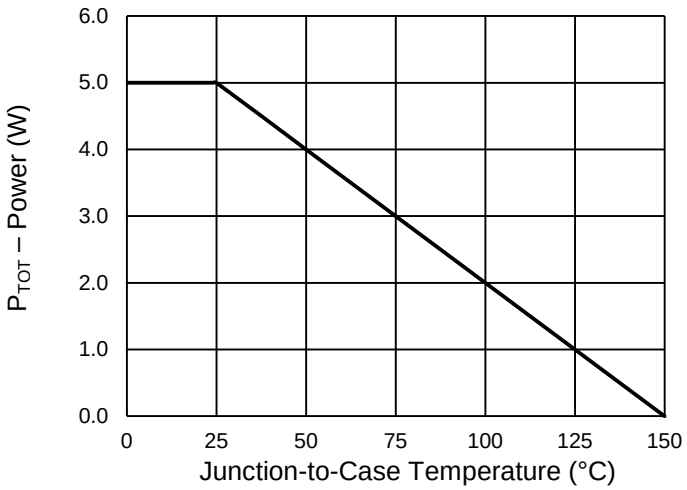
Normalized Thermal Transient Impedance, Junction-to-Case



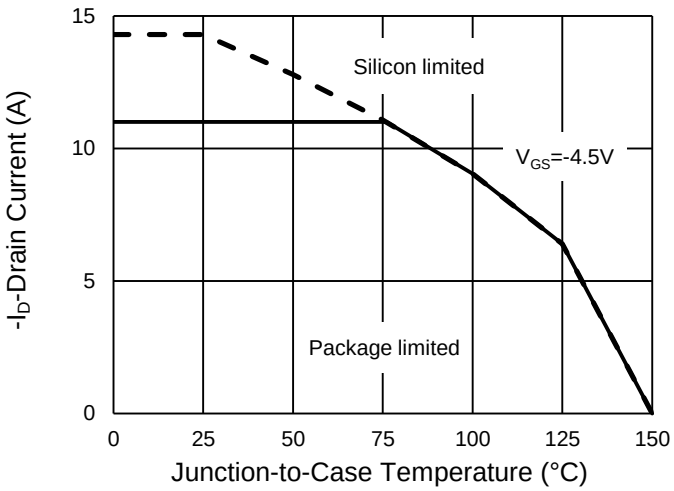
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

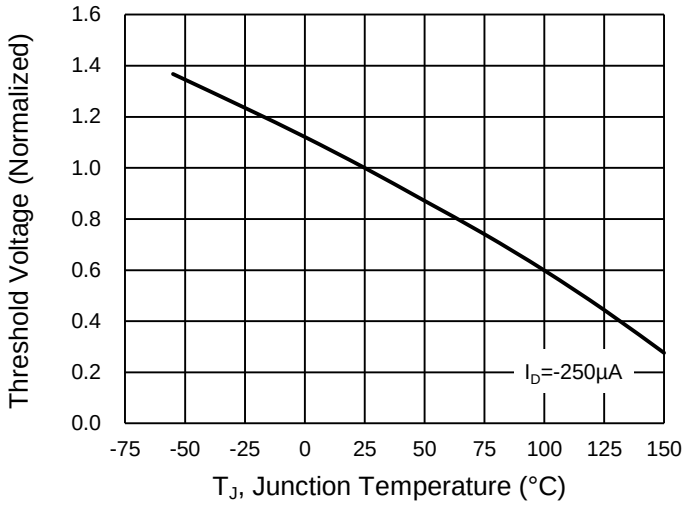
Power Dissipation



Drain Current

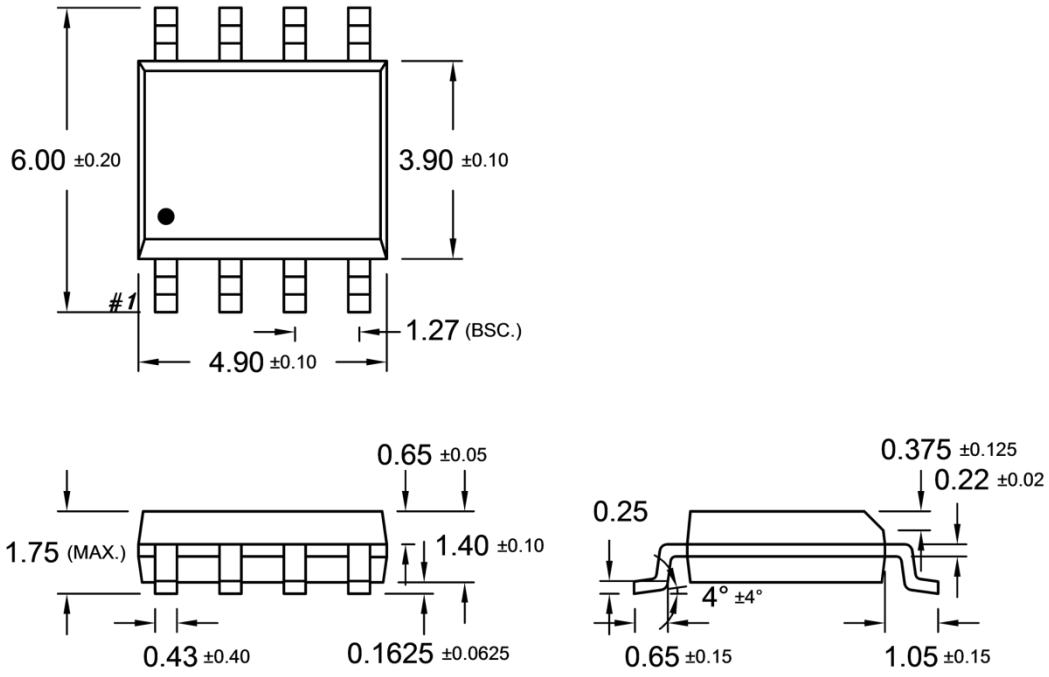


Normalized gate threshold voltage vs Temperature

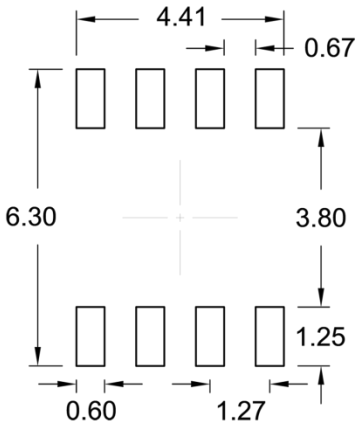


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

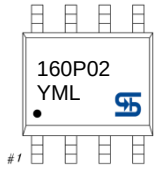
SOP-8



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code
M = Month Code

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code (1~9, A~Z)

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