LM5155EVM-SEPIC User's Guide

The LM5155EVM-SEPIC Evaluation Module (EVM) is designed to showcase the LM5155 wide input voltage Boost/SEPIC/Boost controller, implementing a SEPIC converter with a coupled inductor. The EVM operates at 2.2 MHz, and it produces a regulated output of 12 V 24 W from an input of 5 V to 42 V. When the input voltage is between 3 V to 5 V, the output power is derated down to 10 W. The factory-installed controller is the LM5155-Q1. However, by replacing the IC, the EVM can also be used to demonstrate the performance of the LM51551-Q1, LM5155 and LM51551. The difference between the LM5155-Q1 and LM51551-Q1, or between the LM5155 and LM51551, is that the latter features the hiccup mode for overload protection.

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1 Features and Electrical Performance

The LM5155EVM-SEPIC supports the following features and performance capabilities:

- Wide input voltage range from 3 V to 42 V, to cover typical automotive battery voltage ranges including cold cranking and load dump transients
- Optimized for input voltage range from 6 V to 18 V
- Tightly regulated output voltage of 12 V with a 1% accurate reference voltage
- Supports 2 A full load when V$_{IN}$ is greater than 5 V
- Supports 0.8 A load current when V$_{IN}$ drops to 3 V
- 2.2 MHz switching frequency
- Peak efficiency > 88%
- Can evaluate LM51551-Q1, LM5155, and LM51551 ICs, by replacing the factory installed IC with the corresponding IC
- Hiccup mode for output over current protection (applicable only with LM51551 and LM51551-Q1)

The electrical performance of the EVM is show in Table 1. The EVM terminals and signal test points are listed in Table 2. The typical application circuit is shown in Figure 2. The EVM complete schematic is shown in Figure 19.

1.1 Electrical Parameters

Table 1. Electrical Performance

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage Range V_{IN}	Normal operation, 2 A full load	6	12	18	V
	Maximum transient voltage, 2 A full load	5		42	V
	Power derating from 2 A down to 0.8 A	3		5	V
Input voltage turn on $V_{IN(ON)}$	Adjusted by the UVLO/SYNC resistors		2.9		V
Input voltage turn off $V_{IN(OFF)}$			2.8		V
OUTPUT CHARACTERISTICS					
Output Voltage V_{OUT}			12		V
Maximum Output Current I_{OUT}	$V_{IN} > 5$ V	2			A
	3 V $< V_{IN} < 5$ V	0.8		2	A
Output Voltage V_{OUT_OV}			13.2		V
SYSTEM CHARACTERISTICS					
Switching Frequency			2.2		MHz
External Clock Synchronization	Recommended. IC can synchronize to wider frequency range	1.8		2.5	MHz
Full Load Efficiency			88		%
LM5155-Q1 Junction Temperature, T_J		-40		150	C

1.2 EVM Power Derating Curve

The LM5155EVM-SEPIC is designed to support a full load of 2 A when the input voltage is higher than 5 V. When the input voltage is below 5 V, the output power needs to be derated, owing to the peak current limitation of the selected inductor on the EVM. Figure 1 shows the power derating curve.
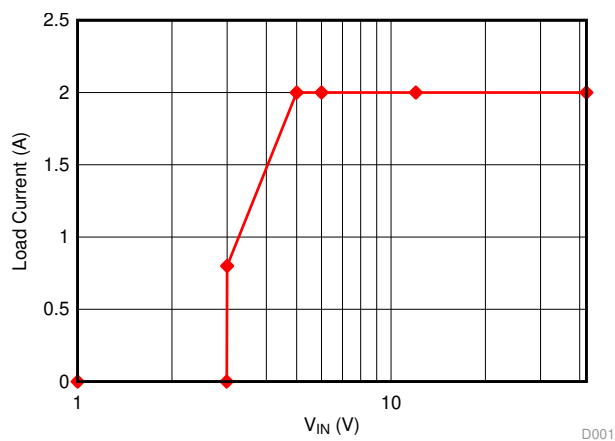

Figure 1. Power Derating vs Input Voltage

1.3 Terminals and Signal Test Points

Table 2 summarizes the EVM terminals and signal test points.

Table 2. EVM Terminals and Signal Test Points

Terminal	SIGNAL	PINS	FUNCTION DESCRIPTION
J1	VIN+		Input Connector
J2	VOUT+		Output Connector
J3	GND		Input Return Connector
J4	GND		Output Return Connector
J5	VCC	Pin 1	IC VCC Pin Signal
	COMP	Pin 2	IC COMP Pin Signal
	SS	Pin 3	IC SS Pin Signal
	PGOOD	Pin 4	IC PGOOD Pin Signal.
	UVLO	Pin 5	IC UVLO Pin Signal and External Enable Control
	BIAS-IC	Pin 6	IC BIAS Pin Signal
J6	PGND		PGND Signal
J7	PGND		PGND Signal
TP1	VIN+		Input Voltage Sense Point
TP2	VOUT		Output Voltage Sense Point
TP3	GND		Input Return Sense Point
TP4	GND		Output Return Sense Point

2 Application Schematic

Figure 2 shows a typical LM5155 SEPIC schematic employing a coupled inductor. Note that the same schematic is applicable to the LM51551, LM5155-Q1, and LM51551-Q1. Refer to Figure 19 for the complete EVM schematic.
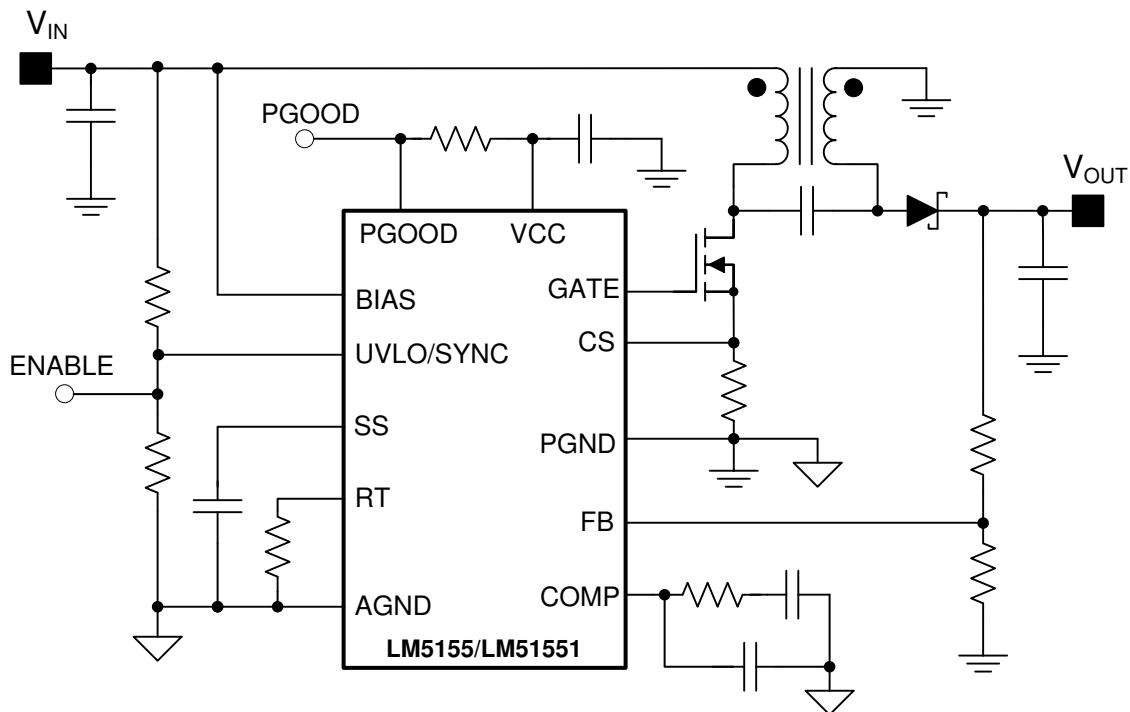

Figure 2. Typical SEPIC Schematic Employing the LM5155/LM51551 and Coupled Inductor

3 EVM Picture

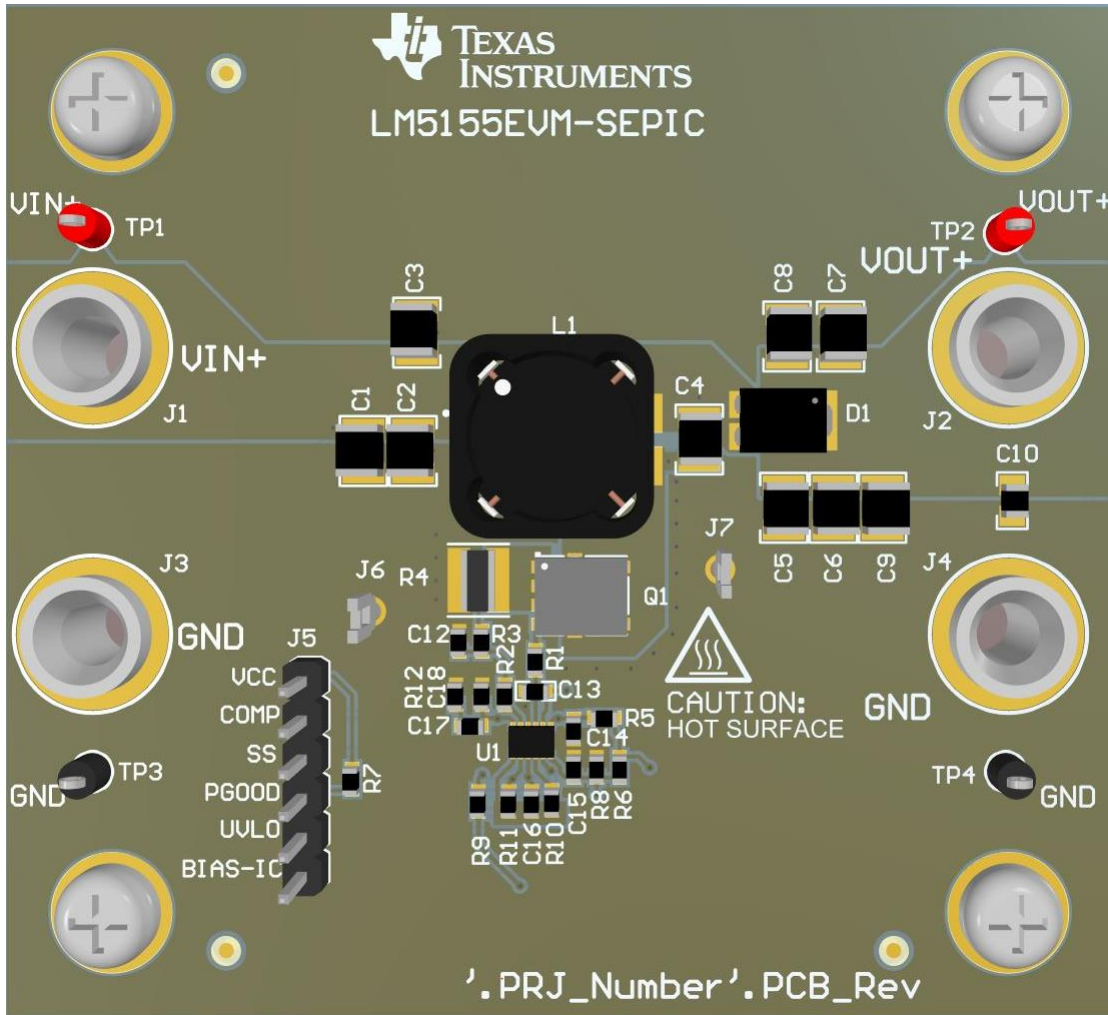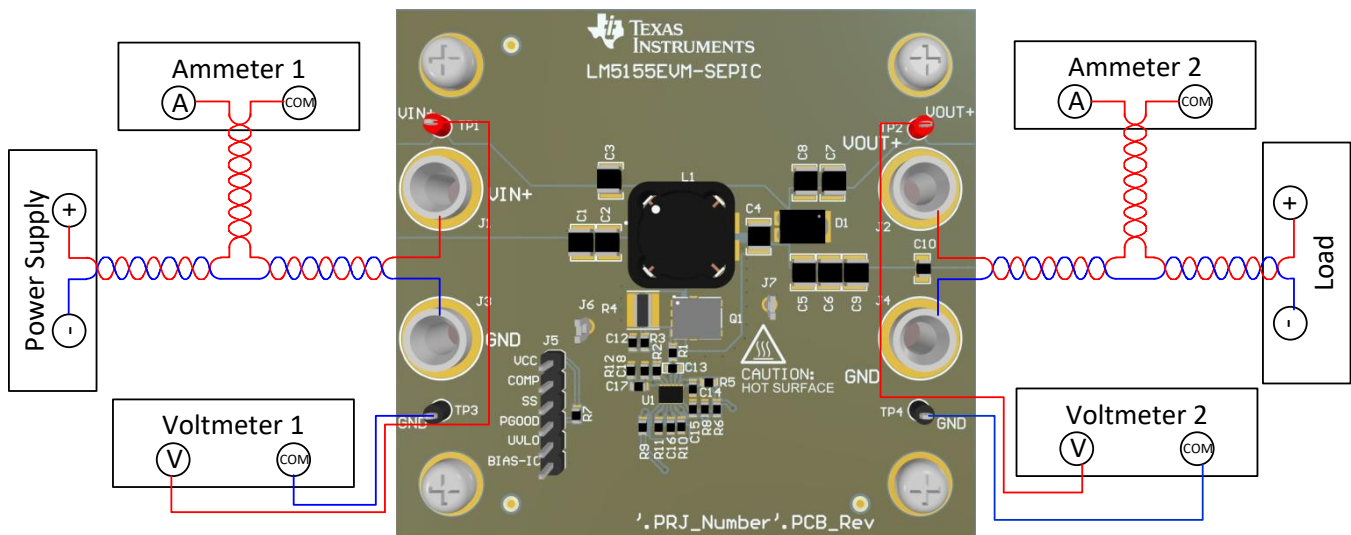Figure 3 shows a 3D-rendered picture of the LM5155EVM-SEPIC. The actual board color may differ.

Figure 3. LM5155EVM-SEPIC 3D-Rendered Picture

4 Test Setup and Procedure

4.1 Bench Setup

Figure 4 shows the bench setup. The Load can be an electronic load or a resistor load.

Figure 4. Test Setup

4.2 Test Equipment

Power Supply: The input voltage source (VIN) should be an adjustable power supply capable of 0 V to 42 V and source at least 10 A.

Electronic Loads: The E-Load should be capable of at least 20 V and 5 A.

Multi-meters:
- Voltmeter 1: Input voltage, connect from VIN to GND
- Voltmeter 2: Output voltage, connect from VOUT to GND
- Ammeter 1: Input current, must be able to handle 10 A. A shunt resistor can be used as needed.
- Ammeter 2: Output current, must be able to handle 3 A. A shunt resistor can be used as needed.

Oscilloscope: An oscilloscope and 10× probes with at least 20-MHz bandwidth is required. Measure the output voltage ripple directly across an output capacitor with a short ground lead. Do not use a long-lead ground connection due to the possibility of noise being coupled into the signal. To measure other waveforms, adjust the oscilloscope as needed.

Input and Output Cables: Cables capable of conducting 10 A current are recommended. Avoid the use of overly-long cables. Cable impedance, especially the inductances, may affect the circuit operation. To minimize the cable impedance effects, *twist the pair of cables* at both input and output ports.

4.3 Precautions

> **CAUTION:**
> **Prolonged operation with low input at full power will cause heating of the MOSFET (Q1).**
> **Board surface is hot. Do not touch. Contact may cause burns.**

5 Test Data

Figure 5 through Figure 18 show the typical performance of the LM5155EVM-SEPIC according to the Bill of Materials and the configuration described in Section 6. Based on measurement techniques and environmental variables, measurements might differ slightly from the data presented.
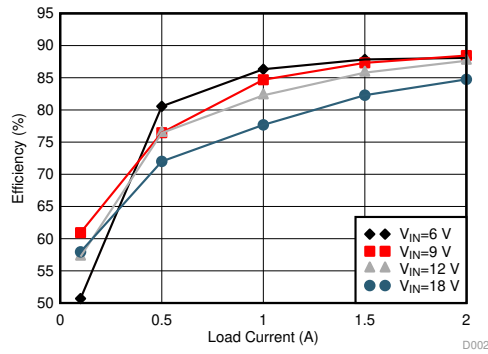
5.1 Efficiency

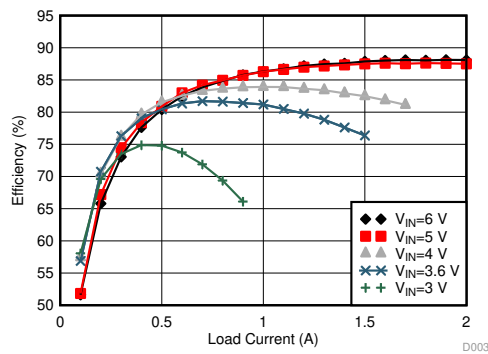**Figure 5. Efficiency vs Load under Normal V$_{IN}$, F$_{SW}$ = 2.2 MHz**

Figure 6. Efficiency vs Load under Low V$_{IN}$, F$_{SW}$ = 2.2 MHz
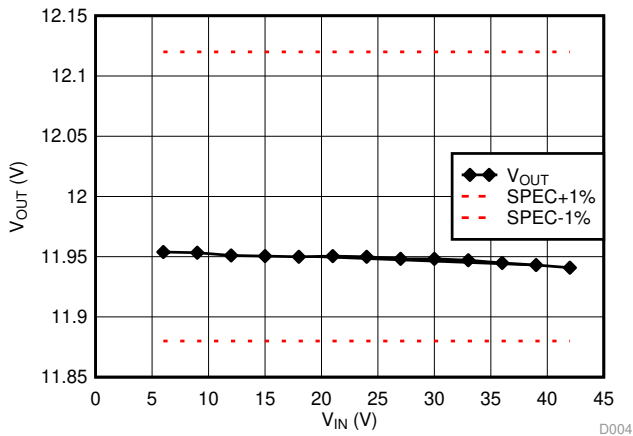
5.2 Output Regulation

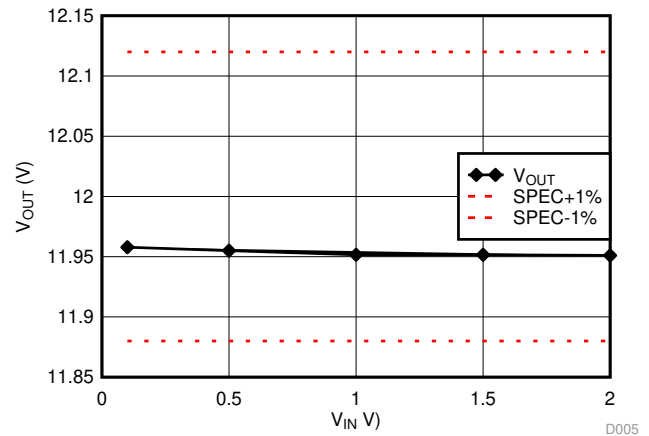

Figure 7. Output Regulation vs Input Voltage, I$_{OUT}$ = 2 A

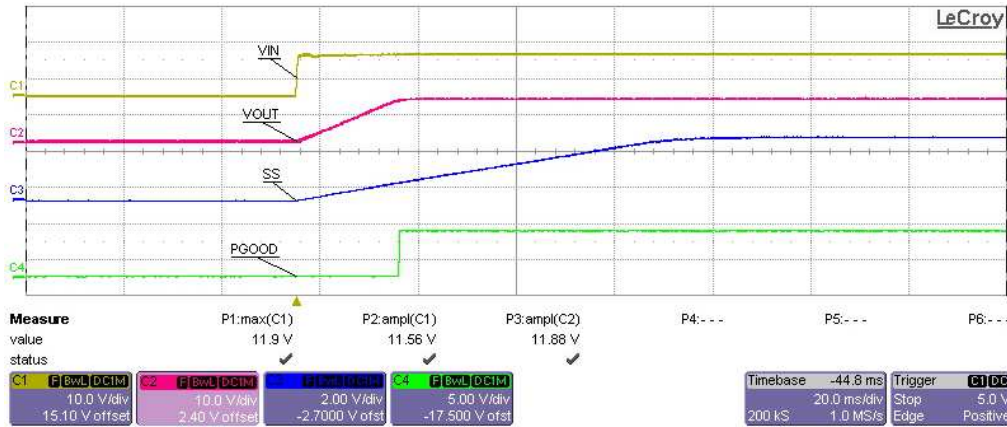**Figure 8. Output Regulation vs Load, v$_{IN}$ = 12 V**

5.3 *Typical Power Up*

Figure 9. EVM Power Up under I$_{OUT}$ = 2 A
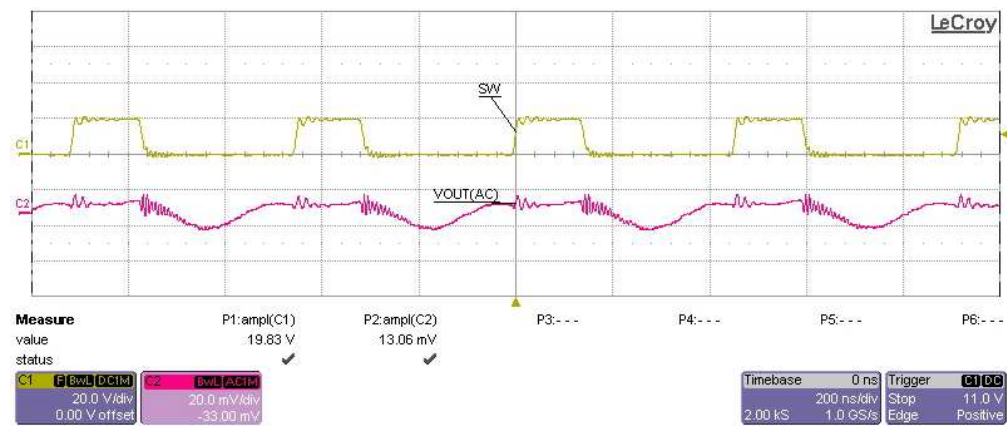
5.4 *Output Ripple Voltage*

Figure 10. Output Ripple Voltage under V$_{IN}$ = 6 V and I$_{OUT}$ = 2 A
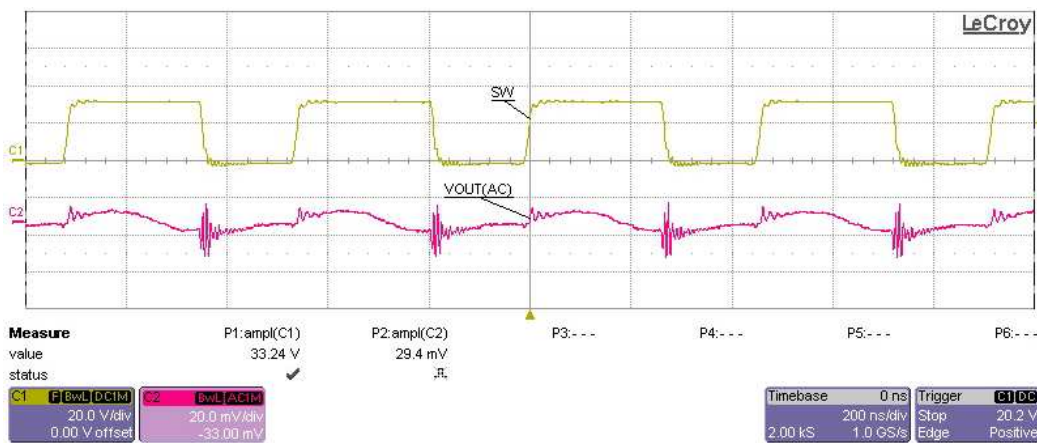
Figure 11. Output Ripple Voltage under V$_{IN}$ = 18 V and I$_{OUT}$ = 2 A
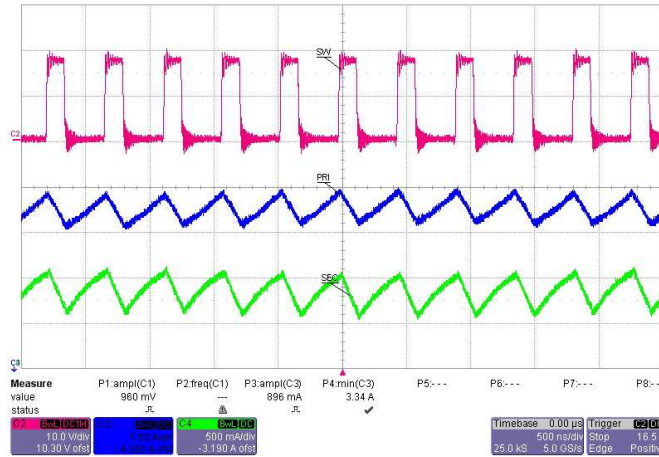
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5.5 *Coupled Inductor Currents*

Figure 12. Coupled Inductor Currents - V_IN = 6 V, I_OUT = 2 A

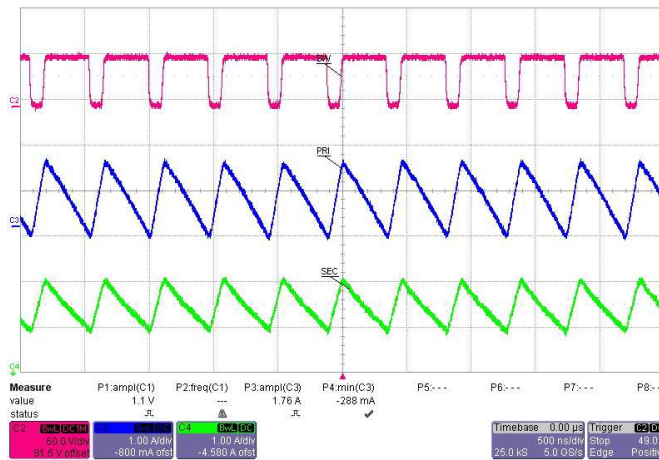**Figure 13. Coupled Inductor Currents - V_IN = 42 V, I_OUT = 2 A**

5.6   *Dynamic DIR Change*

5.7   *Step Load Response*
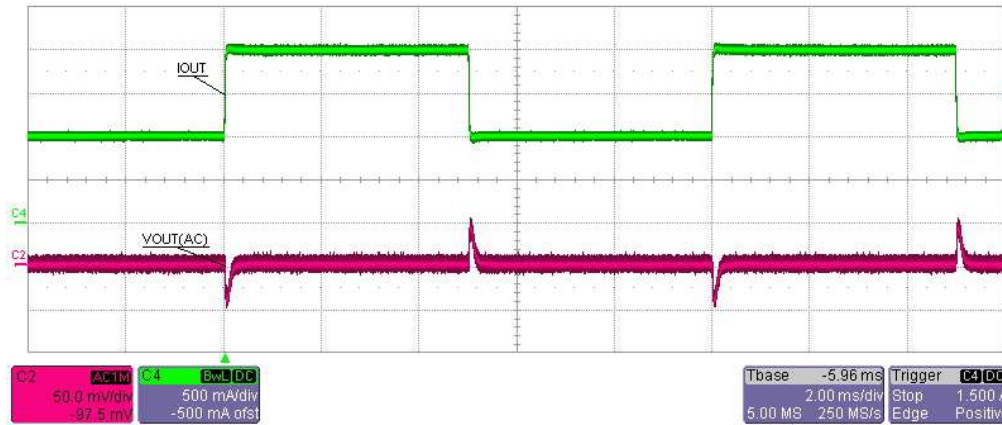
Figure 14. Step Load Response under V$_{IN}$ = 6 V, I$_{OUT}$ = 1 to 2-A Step
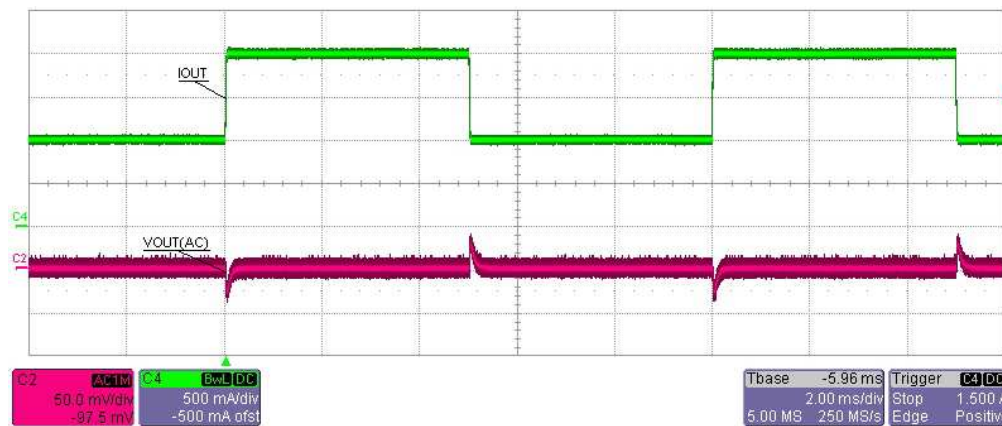
Figure 15. Step Load Response under V$_{IN}$ = 12 V, I$_{OUT}$ = 1 to 2-A Step
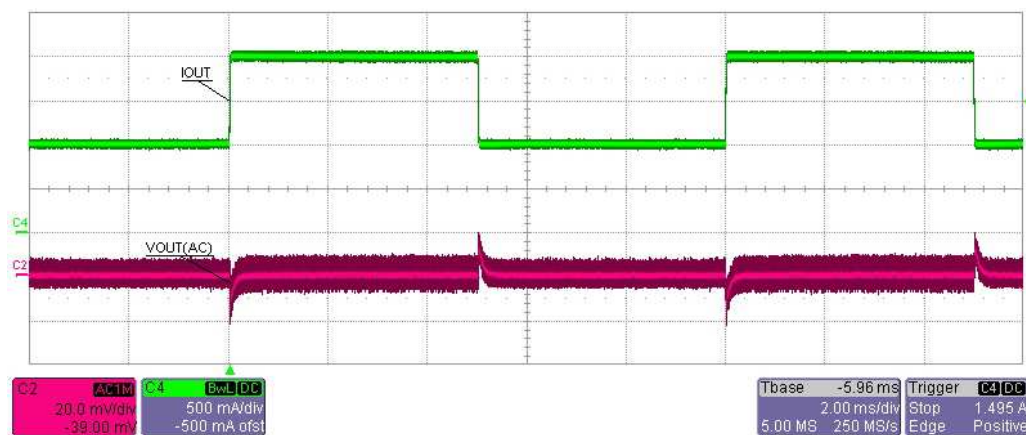
Figure 16. Step Load Response under V$_{IN}$ = 42 V, I$_{OUT}$ = 1 to 2-A Step

5.8 Bode Plots
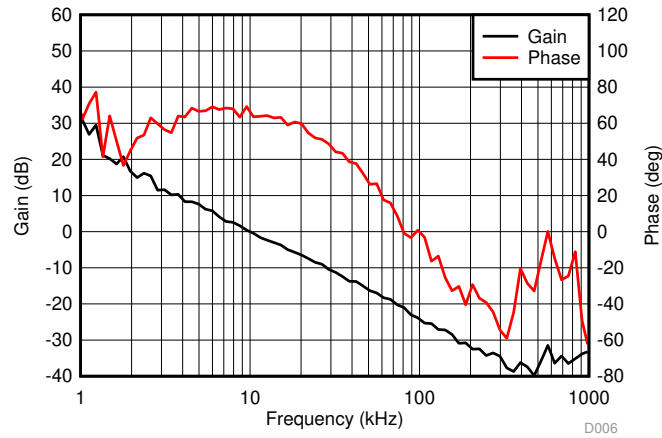
Figure 17. EVM Bode Plots

5.9 Overloading Hiccup Mode

Overloading Hiccup Mode is applicable only to the LM51551 and LM51551-Q1 ICs. Under overloading or output short circuit, the circuit triggers the retry mode.
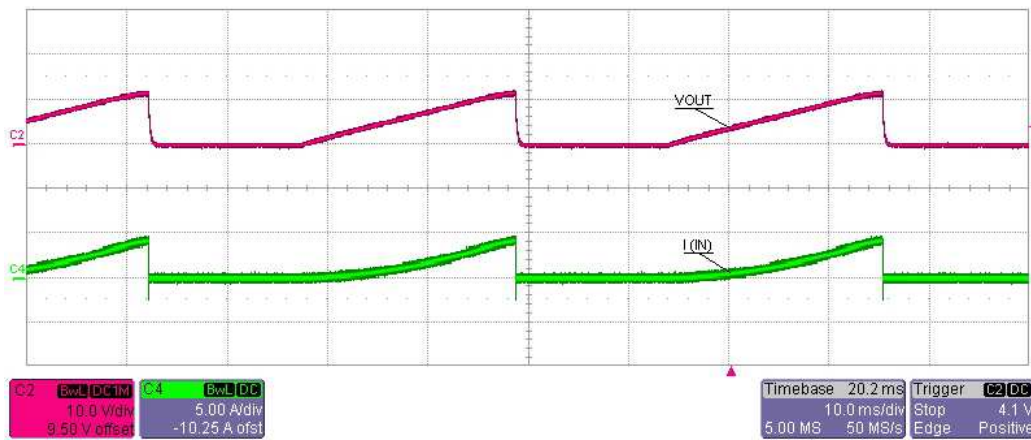
Figure 18. Output Overloading Hiccup Mode

6 Design Files

6.1 Schematics
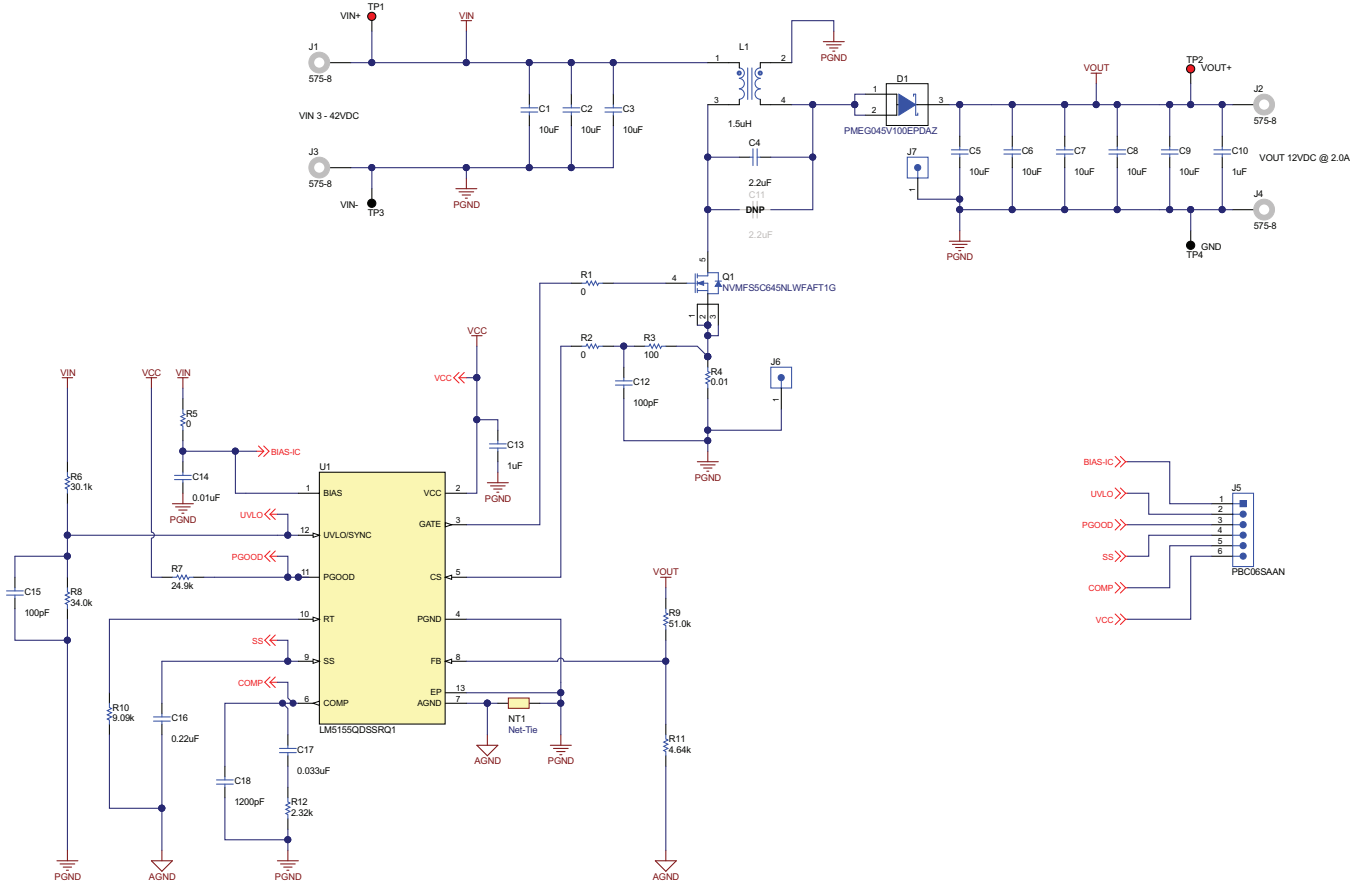
Figure 19. EVM Schematic

6.2 Bill of Materials

Table 3. LM5155EVM-SEPIC Bill of Materials

| Designator	Quantity	Description	Part Number	Manufacturer
!PCB1	1	Printed Circuit Board	BMC030	Any
C1, C2, C3, C5, C6, C7, C8, C9	8	CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, 1210	GRM32ER71H106KA12L	MuRata
C4	1	CAP, CERM, 2.2 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1	CGA6N3X7R2A225K230AB	TDK
C10	1	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	CGA4J3X7R1H105K125AB	TDK
C12	1	CAP, CERM, 100 pF, 50 V,+/- 1%, C0G/NP0, 0603	C0603C101F5GACTU	Kemet
C13	1	CAP, CERM, 1 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 0603	GCM188R71C105MA64D	MuRata
C14	1	CAP, CERM, 0.01 uF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	CGA3E2C0G1H103J080AA	TDK

Table 3. LM5155EVM-SEPIC Bill of Materials (continued)

Designator	Quantity	Description	Part Number	Manufacturer
C15	1	CAP, CERM, 100 pF, 100 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	GCM1885C2A101JA16D	MuRata
C16	1	CAP, CERM, 0.22 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R71E224KA55D	MuRata
C17	1	CAP, CERM, 0.033 uF, 50 V, +/- 5%, X7R, 0603	06035C333JAT2A	AVX
C18	1	CAP, CERM, 1200 pF, 100 V, +/- 5%, C0G/NP0, 0603	GRM1885C2A122JA01D	MuRata
D1	1	Diode, Schottky, 60 V, 10 A, AEC-Q101, CFP15	PMEG060V100EPDZ	Nexperia
L1	1	Coupled inductor, 1.5 uH, 17.5 A, 0.012 ohm, SMD	7448700015	Wurth Elektronik
Q1	1	MOSFET, N-CH, 60 V, 100 A, AEC-Q101, SO-8FL	NVMFS5C645NLWFAFT1G	ON Semiconductor
R1, R2	2	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3GEY0R00V	Panasonic
R3	1	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3EKF1000V	Panasonic
R4	1	RES, 0.01, 1%, 1 W, 1508	RL3720WT-R010-F	Susumu Co Ltd
R5	1	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R6	1	RES, 30.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060330K1FKEA	Vishay-Dale
R7	1	RES, 24.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060324K9FKEA	Vishay-Dale
R8	1	RES, 34.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060334K0FKEA	Vishay-Dale
R9	1	RES, 51.0 k, 1%, 0.1 W, 0603	RC0603FR-0751KL	Yageo
R10	1	RES, 9.09 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06039K09FKEA	Vishay-Dale
R11	1	RES, 4.64 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06034K64FKEA	Vishay-Dale
R12	1	RES, 2.32 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06032K32FKEA	Vishay-Dale
TP1, TP2	2	Test Point, Miniature, Red, TH	5000	Keystone
TP3, TP4	2	Test Point, Miniature, Black, TH	5001	Keystone
U1	1	Automotive Grade 2.2-MHz Wide Input Non-synchronous Boost Controller, DSS0012C (WSON-12)	LM5155QDSSRQ1	Texas Instruments
C11	0	CAP, CERM, 2.2 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1	CGA6N3X7R2A225K230AB	TDK

6.3 Board Layout

The EVM PC Board consists of two copper layers, and the board includes various headers for flexible configurations suitable for different applications. Figure 20 through Figure 23 show the EVM PCB artwork.
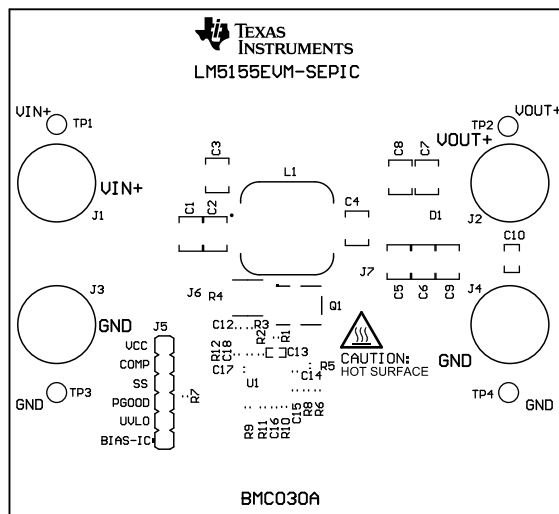

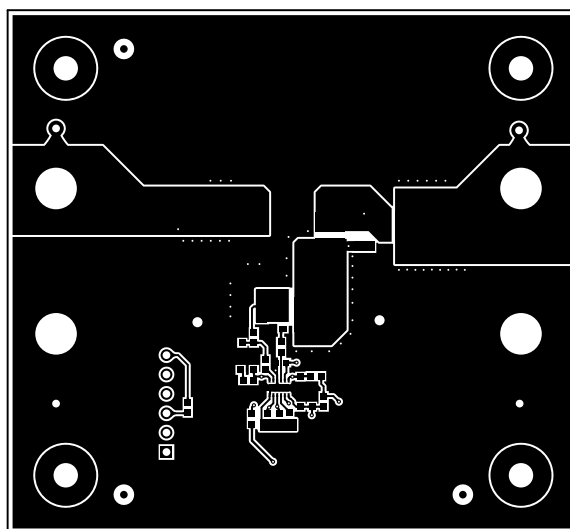**Figure 20. EVM Top Layer Silkscreen**
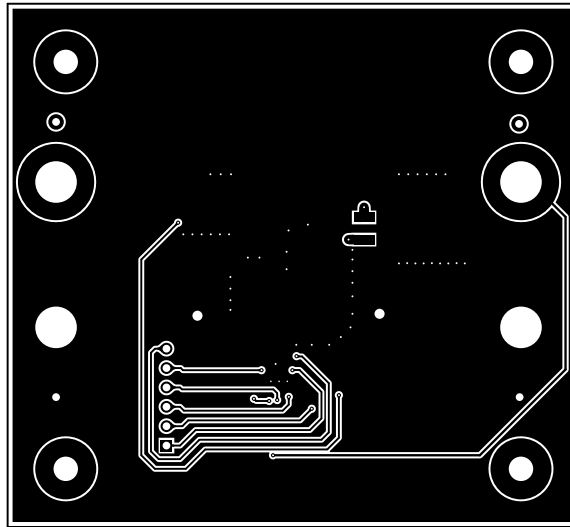

Figure 21. EVM Top Layer Copper

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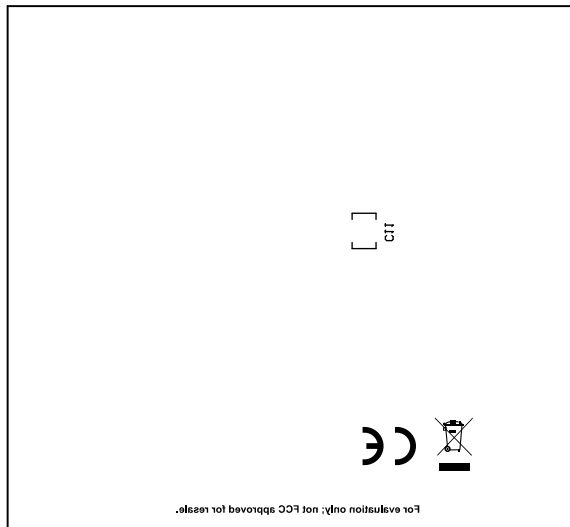
Figure 22. EVM Bottom Layer Copper

Figure 23. EVM Bottom Layer Silkscreen

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