IS65WV25616ALL
IS65WV25616BLL

256K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC SRAM

JUNE 2017

FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation
  36 mW (typical) operating
  9 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  1.65V--2.2V V_{DD} (65WV25616ALL)
  2.5V--3.6V V_{DD} (65WV25616BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- TEMPERATURE OFFERINGS:
  Option A1: -40°C to +85°C
  Option A2: -40°C to +105°C
  Option A3: -40°C to +125°C
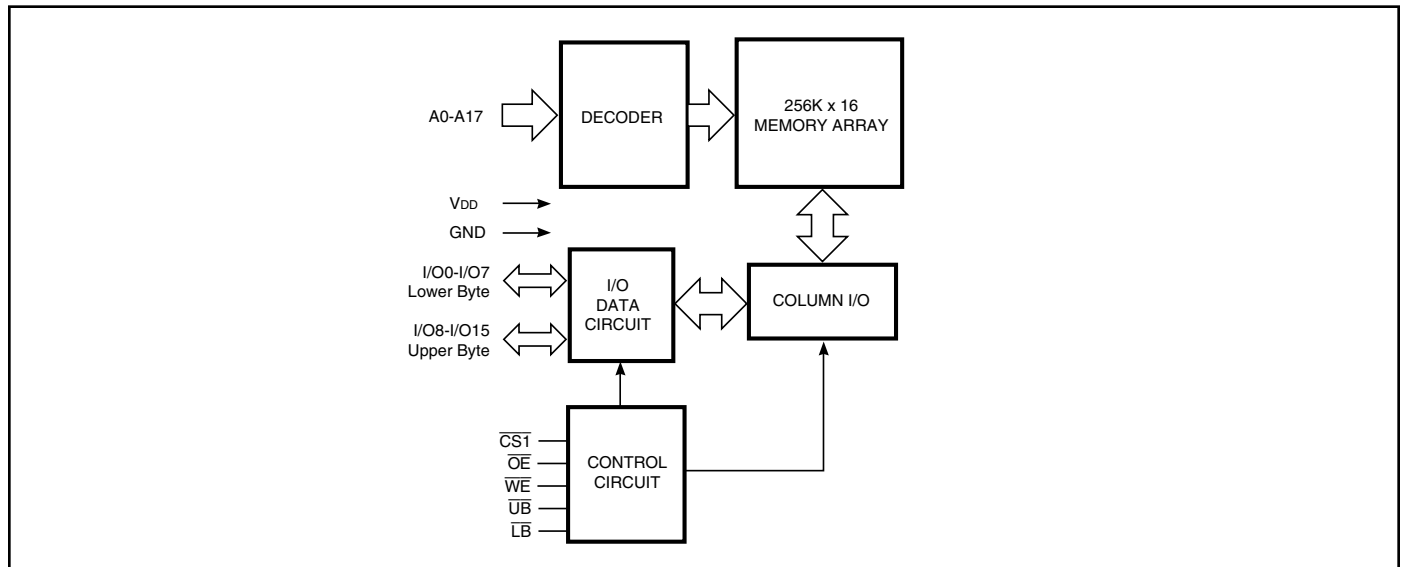- Lead-free available

DESCRIPTION

The *ISSI* IS65WV25616ALL/IS65WV25616BLL are high-speed, low power, 4M bit SRAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when $\overline{CS1}$ is LOW, and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS65WV25616BALL/65WV25616BLL are packaged in the JEDEC standard 44-Pin TSOP (TYPE II) and 48-pin mini BGA (6mmx8mm).
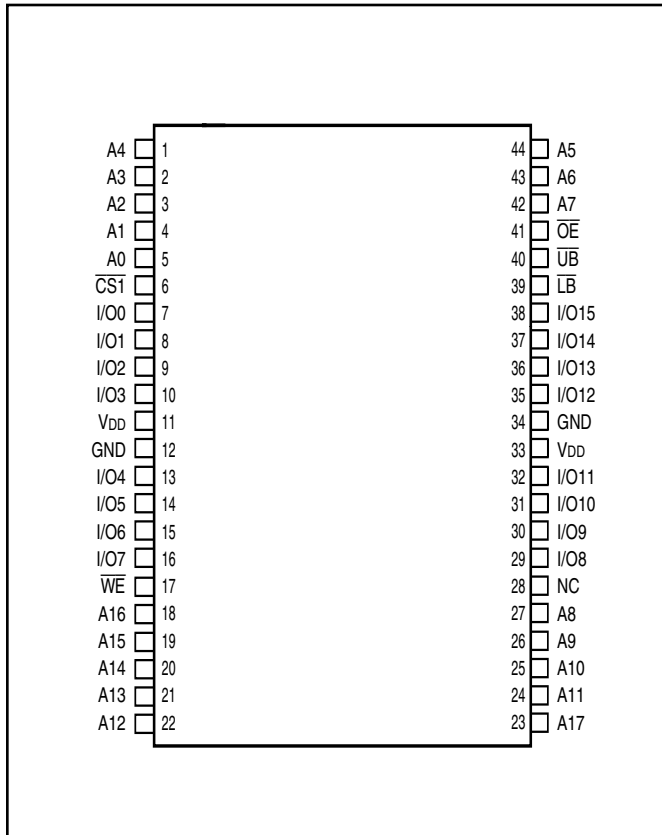
FUNCTIONAL BLOCK DIAGRAM

Integrated Silicon Solution, Inc. — www.issi.com
Rev. E
06/12/2017

IS65WV25616ALL, IS65WV25616BLL

44-Pin mini TSOP (Type II)
(Package Code T)

A4 □ 1	44 □ A5
A3 □ 2	43 □ A6
A2 □ 3	42 □ A7
A1 □ 4	41 □ $\overline{OE}$
A0 □ 5	40 □ $\overline{UB}$
$\overline{CS1}$ □ 6	39 □ $\overline{LB}$
I/O0 □ 7	38 □ I/O15
I/O1 □ 8	37 □ I/O14
I/O2 □ 9	36 □ I/O13
I/O3 □ 10	35 □ I/O12
V$_{DD}$ □ 11	34 □ GND
GND □ 12	33 □ V$_{DD}$
I/O4 □ 13	32 □ I/O11
I/O5 □ 14	31 □ I/O10
I/O6 □ 15	30 □ I/O9
I/O7 □ 16	29 □ I/O8
$\overline{WE}$ □ 17	28 □ NC
A16 □ 18	27 □ A8
A15 □ 19	26 □ A9
A14 □ 20	25 □ A10
A13 □ 21	24 □ A11
A12 □ 22	23 □ A17

PIN CONFIGURATIONS
48- ball mini BGA (6mm x 8mm)
(Package Code B)
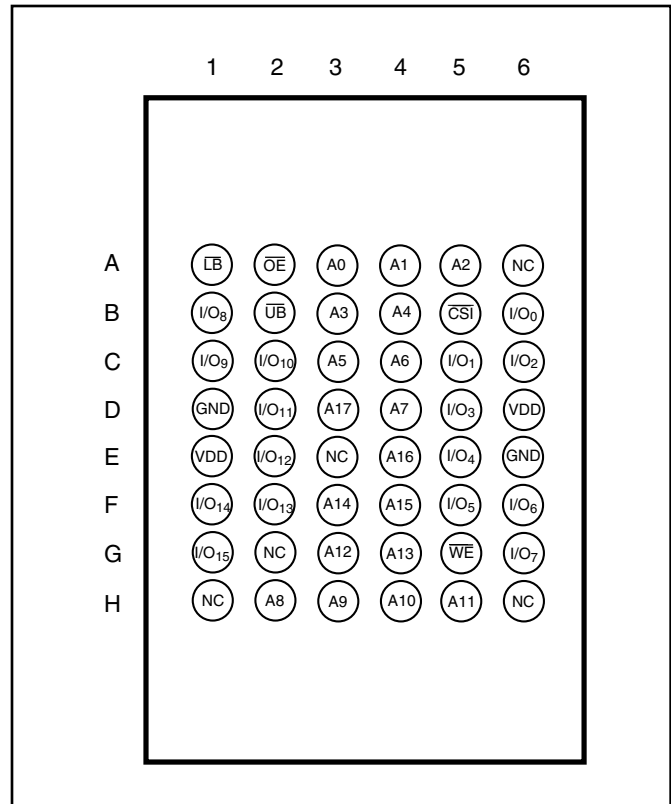
PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V$_{DD}$	Power
GND	Ground

44-Pin mini TSOP (Type II)
2 Chip Enable Option
(Package Code T2)

A4 □ 1	44 □ A5
A3 □ 2	43 □ A6
A2 □ 3	42 □ A7
A1 □ 4	41 □ $\overline{OE}$
A0 □ 5	40 □ $\overline{UB}$
$\overline{CS1}$ □ 6	39 □ $\overline{LB}$
I/O0 □ 7	38 □ I/O15
I/O1 □ 8	37 □ I/O14
I/O2 □ 9	36 □ I/O13
I/O3 □ 10	35 □ I/O12
V$_{DD}$ □ 11	34 □ GND
GND □ 12	33 □ V$_{DD}$
I/O4 □ 13	32 □ I/O11
I/O5 □ 14	31 □ I/O10
I/O6 □ 15	30 □ I/O9
I/O7 □ 16	29 □ I/O8
$\overline{WE}$ □ 17	28 □ CS2
A16 □ 18	27 □ A8
A15 □ 19	26 □ A9
A14 □ 20	25 □ A10
A13 □ 21	24 □ A11
A12 □ 22	23 □ A17
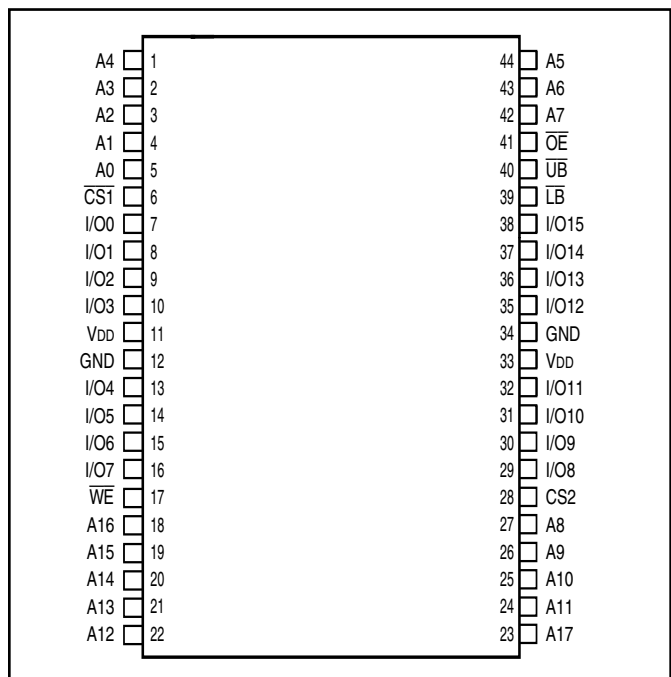
TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0-I/O7	I/O8-I/O15	V$_{DD}$ Current
						I/O PIN		
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	L	X	High-Z	High-Z	I_{CC}
	H	L	H	X	L	High-Z	High-Z	I_{CC}
Read	H	L	L	L	H	D$_{OUT}$	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D$_{OUT}$	
	H	L	L	L	L	D$_{OUT}$	D$_{OUT}$	
Write	L	L	X	L	H	D$_{IN}$	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D$_{IN}$	
	L	L	X	L	L	D$_{IN}$	D$_{IN}$	

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.2 to V_{DD}+0.3	V
V_{DD}	V_{DD} Related to GND	−0.2 to V_{DD}+0.3	V
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	IS65WV25616ALL	IS65WV25616BLL
A1	-40°C to +85°C	1.65V - 2.2V	2.5V-3.6V
A2	−40°C to +105°C	1.65V - 2.2V	2.5V-3.6V
A3	−40°C to +125°C	1.65V - 2.2V	2.5V-3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
		I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
		I_{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
			2.5-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}[1]	Input LOW Voltage		1.65-2.2V	−0.2	0.4	V
			2.5-3.6V	−0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		−2	2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		−2	2	µA

Notes:
1. V_{IL} (min.) = −1.0V for pulse width less than 10 ns.

IS65WV25616ALL, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 70	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	A1	25	mA
			A2, A3	30	
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V $\overline{WE}$ = V_{DD}-0.2V f=1MHZ	A1	10	mA
			A2, A3	15	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH} , f = 1 MHz	A1	0.5	mA
			A2, A3	0.6	
		OR			
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}			
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	A1	15	µA
			A2	30	
			A3	50	
		OR			
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, $V_{IN} \leq 0.2V$, f = 0; $\overline{UB}$ / $\overline{LB}$ = $V_{DD} - 0.2V$			

IS65WV25616BLL, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55	Max. 70	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	A1	40	—	mA
			A2, A3	—	40	
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V $\overline{WE}$ = V_{DD}-0.2V, f=1MHZ	A1	15	—	mA
			A2, A3	—	20	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH} , f = 1 MHz	A1	0.45	—	mA
			A2, A3	—	0.45	
		OR				
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}				
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	A1	20	—	µA
			A2	—	55	
			A3	—	90	
		OR				
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, $V_{IN} \leq 0.2V$, f = 0; $\overline{UB}$ / $\overline{LB}$ = $V_{DD} - 0.2V$				

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	8	pF
C_{OUT}	Input/Output Capacitance	$V_{OUT} = 0V$	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	IS65WV25616ALL (Unit)	IS65WV25616BLL (Unit)
Input Pulse Level	0.4V to V_{DD}-0.2V	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	IS65WV25616ALL 1.65V-2.2V	IS65WV25616BLL 2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V_{REF}	0.9V	1.5V
V_{TM}	1.8V	2.8V

AC TEST LOADS
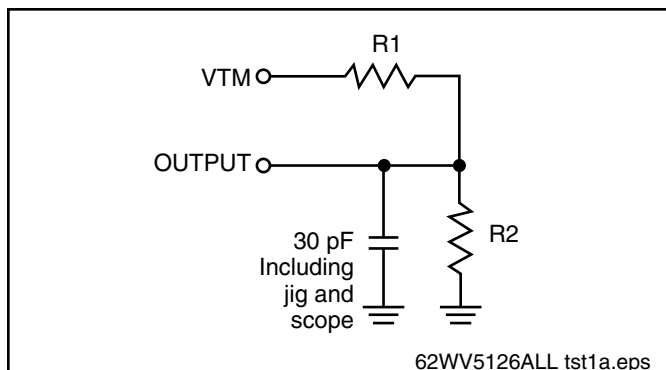
Figure 1
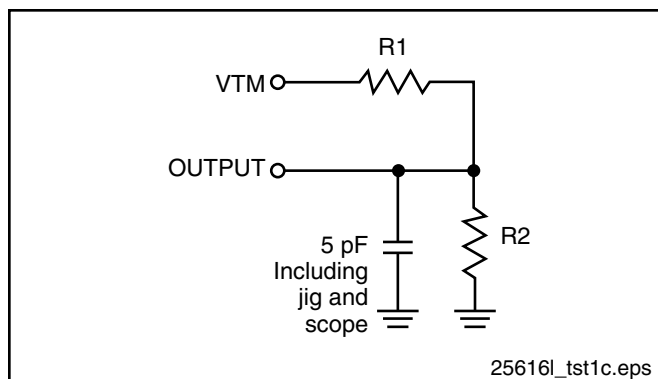
Figure 2

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS1}	$\overline{CS1}$ Access Time	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCS1}	$\overline{CS1}$ to High-Z Output	0	20	0	25	ns
t_{LZCS1}	$\overline{CS1}$ to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	55	—	70	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	20	0	25	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$)

25616R1.eps
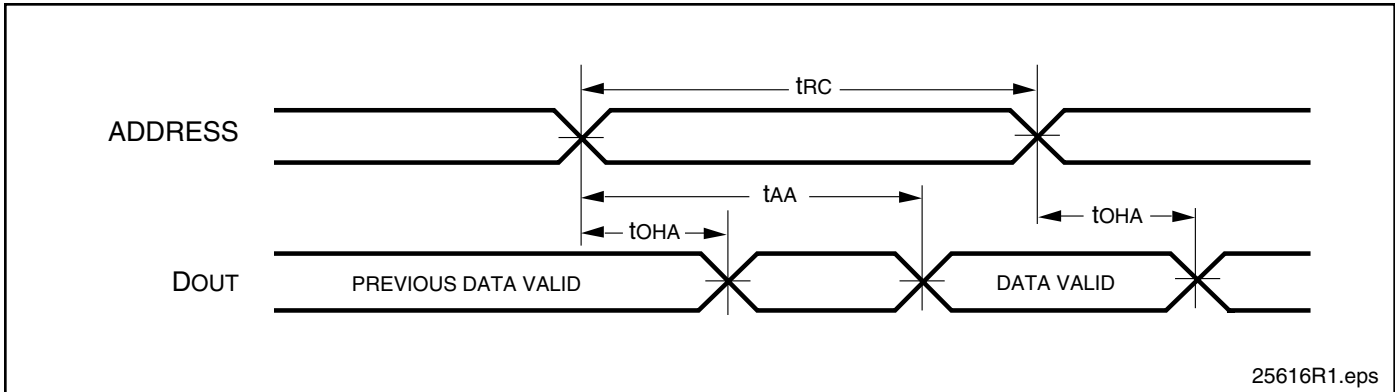
READ CYCLE NO. 2[1,3] ($\overline{CS1}$, $\overline{OE}$, AND $\overline{UB}/\overline{LB}$ Controlled)

51216LL Read 2.eps
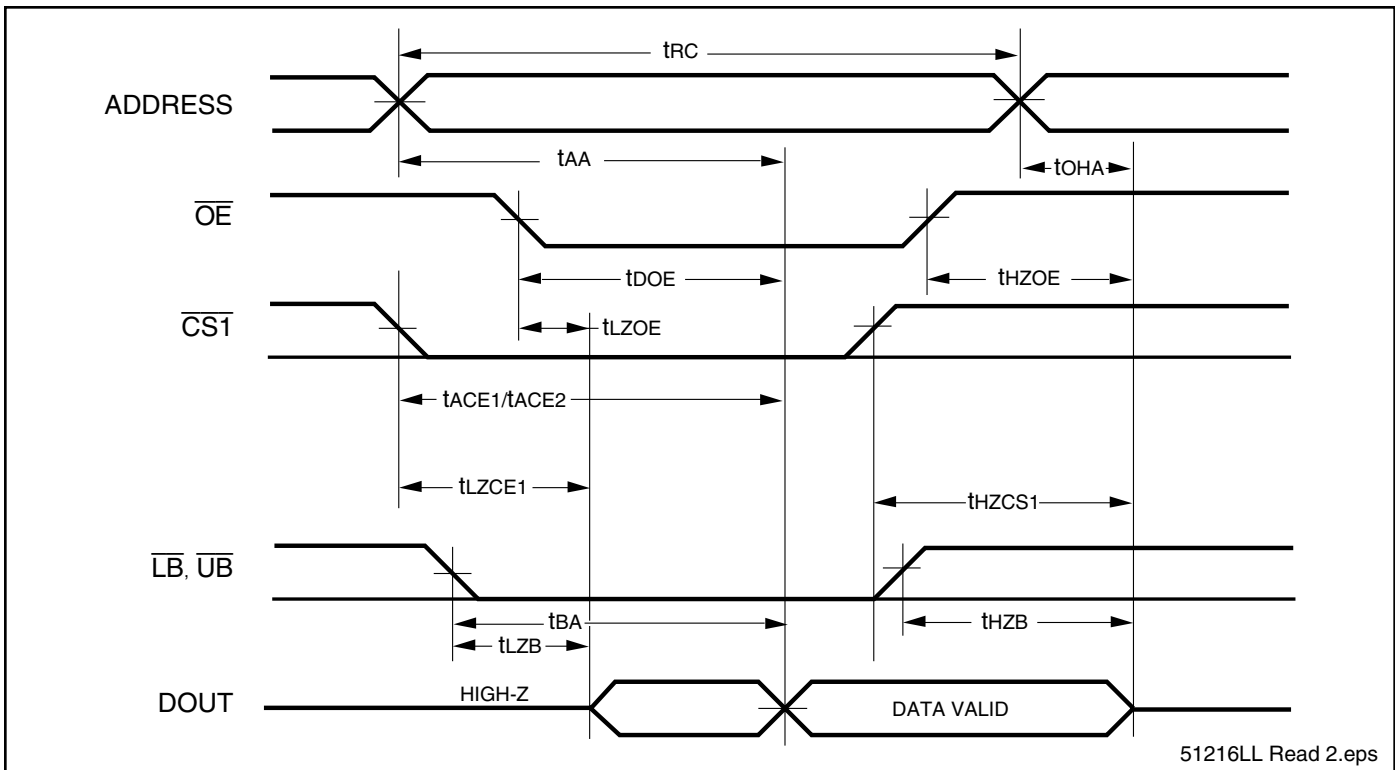
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB} = V_{IL}$. $\overline{WE}=V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

## WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{SCS1}	CS1 to Write End	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	LB, UB Valid to End of Write	45	—	60	—	ns
t_{PWE}	WE Pulse Width	40	—	50	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	WE LOW to High-Z Output	—	20	—	20	ns
t_{LZWE}[3]	WE HIGH to Low-Z Output	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
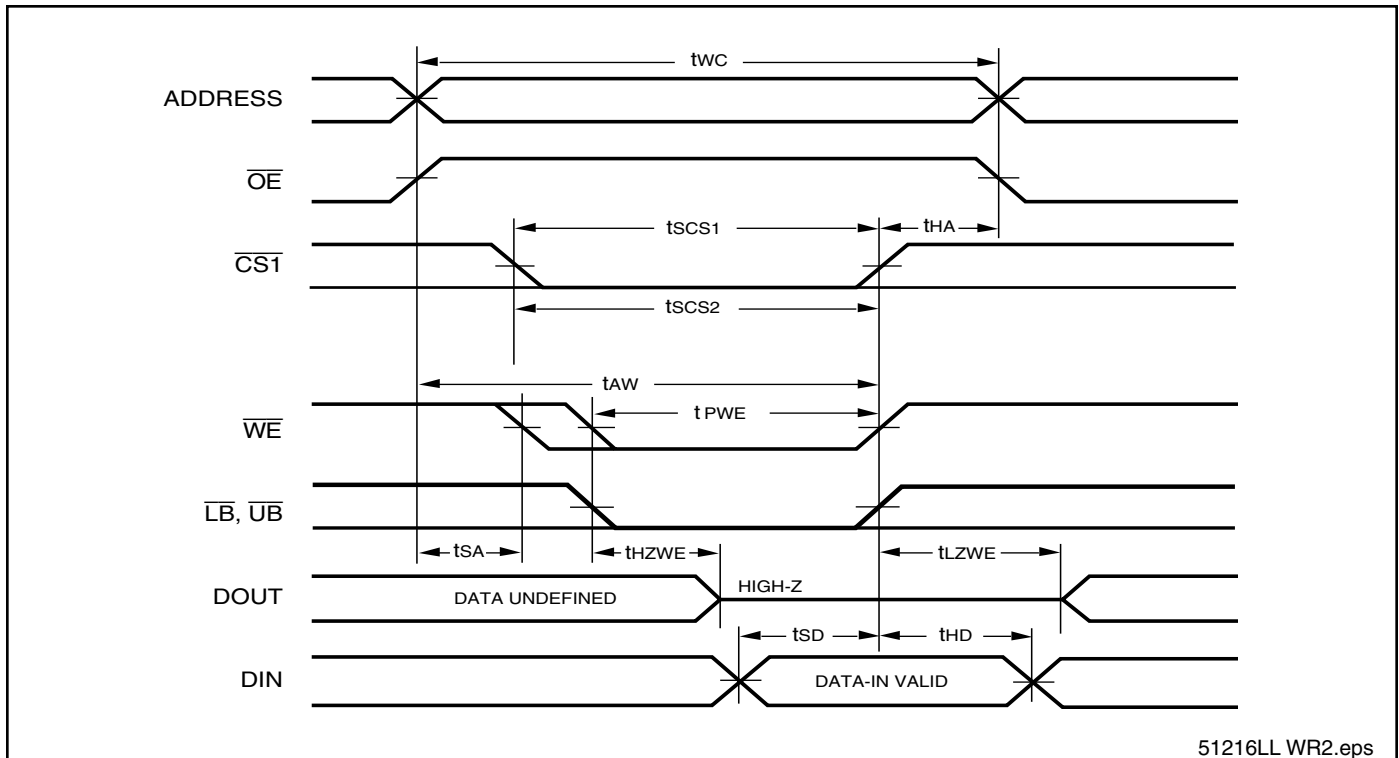
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)
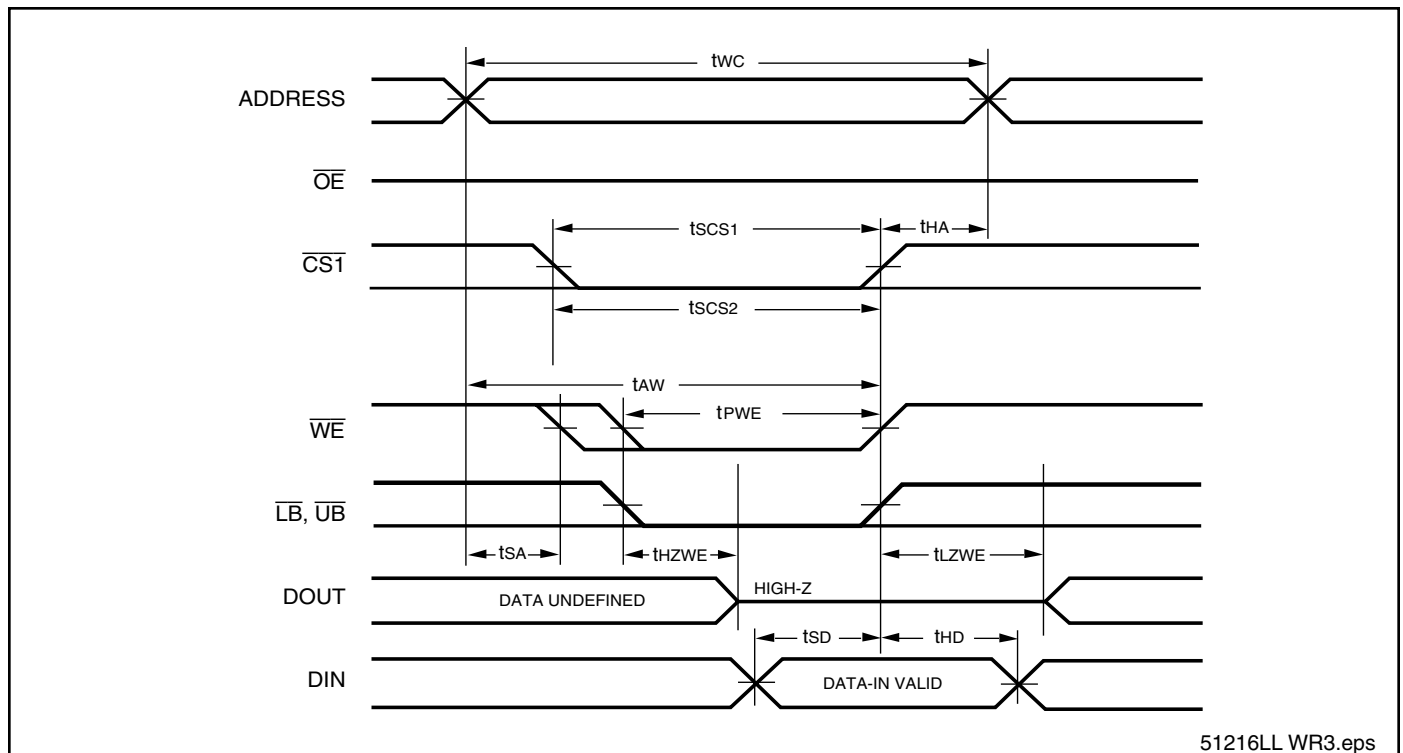

51216LLWRITE 1.eps
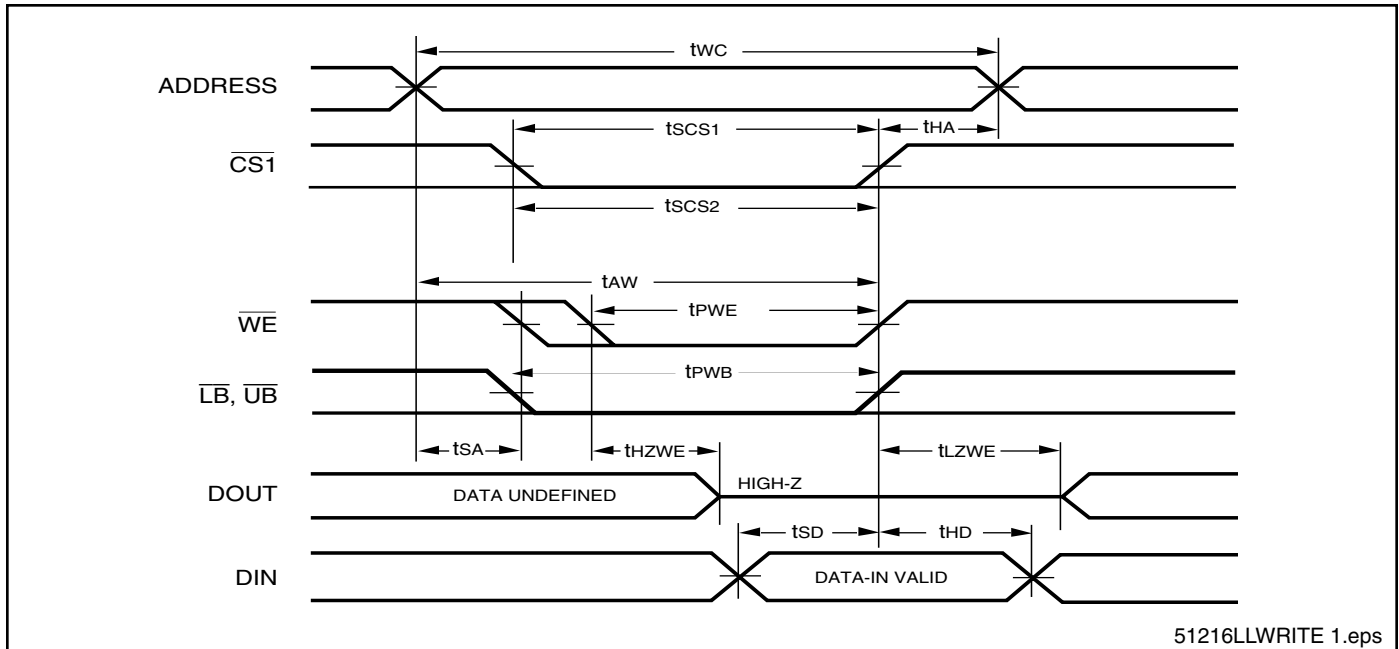
Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = $(\overline{CS1})$ [$(\overline{LB}) = (\overline{UB})$] $(\overline{WE})$.
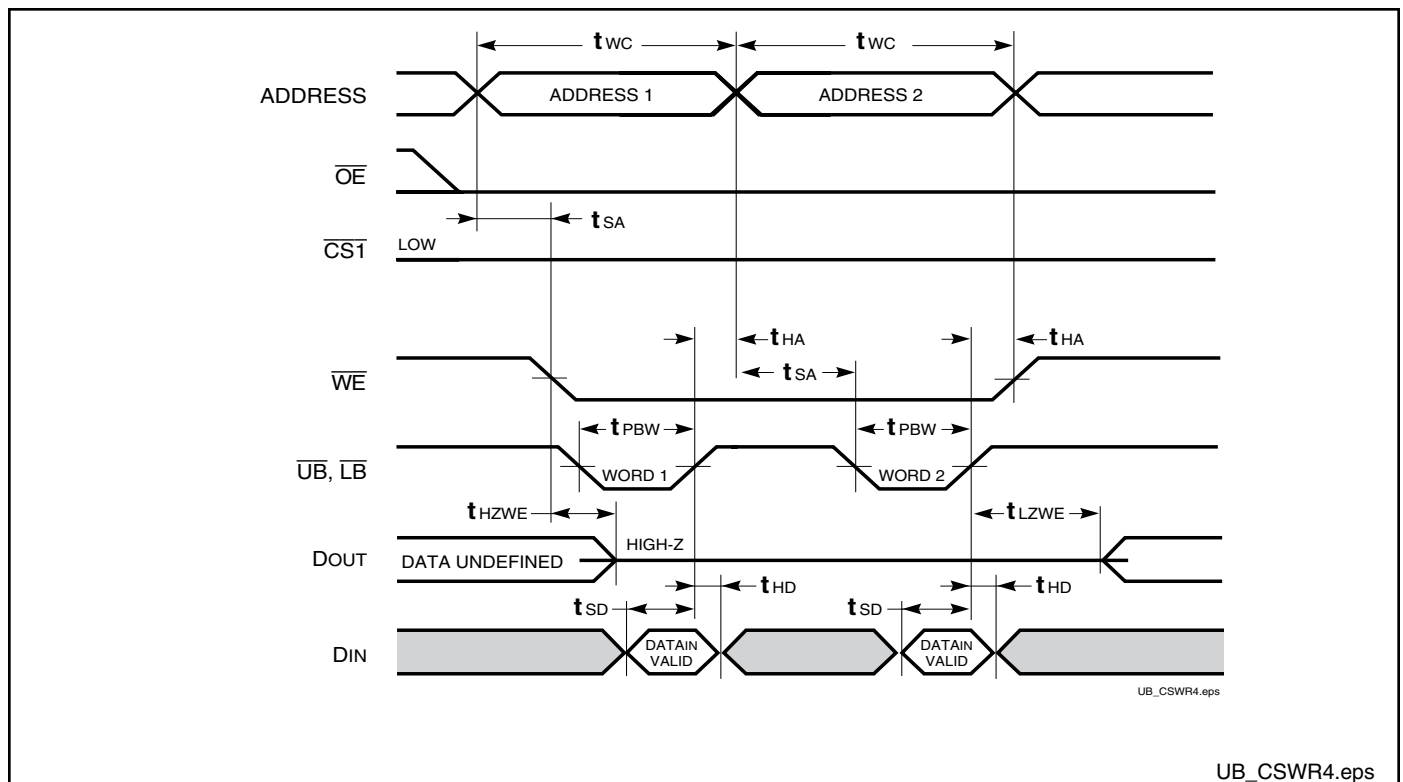
WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)

51216LL WR2.eps

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WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

51216LL WR3.eps

WRITE CYCLE NO. 4 ($\overline{UB}/\overline{LB}$ Controlled)

UB_CSWR4.eps

DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 1.2V, $\overline{CS1} \geq V_{DD}$ – 0.2V	A1	—	20	µA
			A2	—	40	µA
			A3	—	60	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)

51216LT_DR.eps
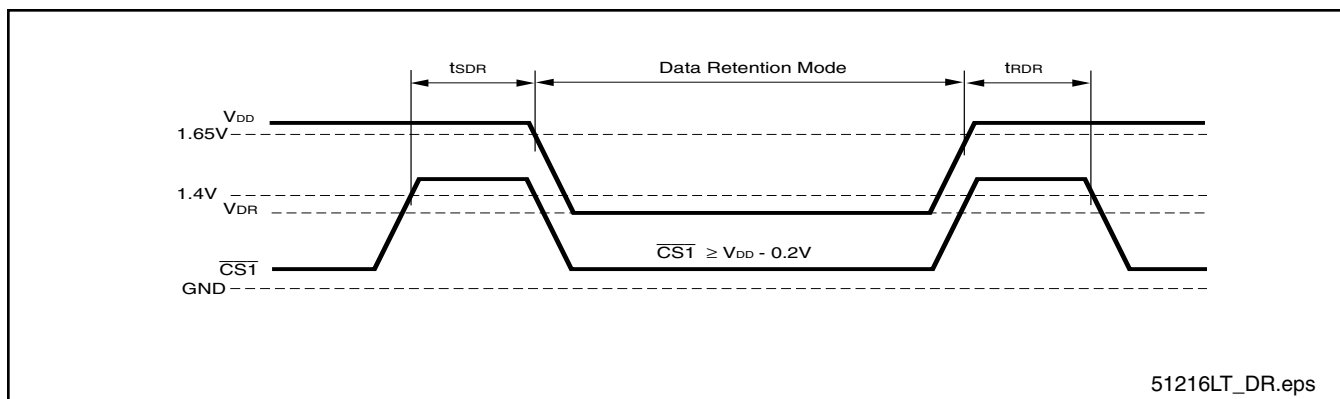
ORDERING INFORMATION: IS65WV25616ALL (1.65V-2.2V)

Temperature Range (A1): –40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616ALL-70CTLA1	44-pin TSOP-II, Copper Leadframe, Lead-free

Temperature Range (A2): –40°C to +105°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616ALL-70CTLA2	44-pin TSOP-II, Copper Leadframe, Lead-free

Temperature Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616ALL-70CTLA3	44-pin TSOP-II, Copper Leadframe, Lead-free

**ORDERING INFORMATION: IS65WV25616BLL (2.5V-3.6V)**

Temperature Range (A1): –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS65WV25616BLL-55CTLA1	44-pin TSOP-II, Copper Leadframe, Lead-free
	IS65WV25616BLL-55BA1	48-ball BGA
	IS65WV25616BLL-55BLA1	48-ball BGA, Lead-free

Temperature Range (A2): –40°C to +105°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616BLL-70CTLA2	44-pin TSOP-II, Copper Leadframe, Lead-free
	IS65WV25616BLL-70BA2	48-ball BGA
	IS65WV25616BLL-70BLA2	48-ball BGA, Lead-free

Temperature Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
70	IS65WV25616BLL-70CTLA3	44-pin TSOP-II, Copper Leadframe, Lead-free
	IS65WV25616BLL-70BA3	48-ball BGA
	IS65WV25616BLL-70BLA3	48-ball BGA, Lead-free
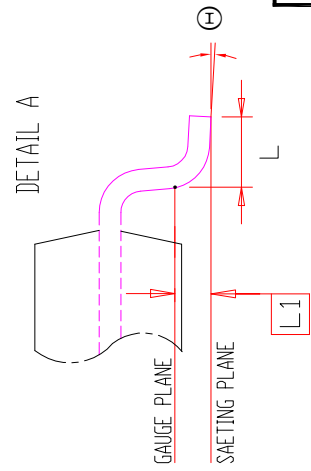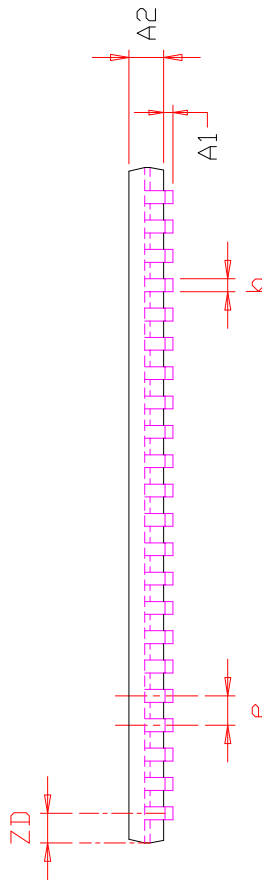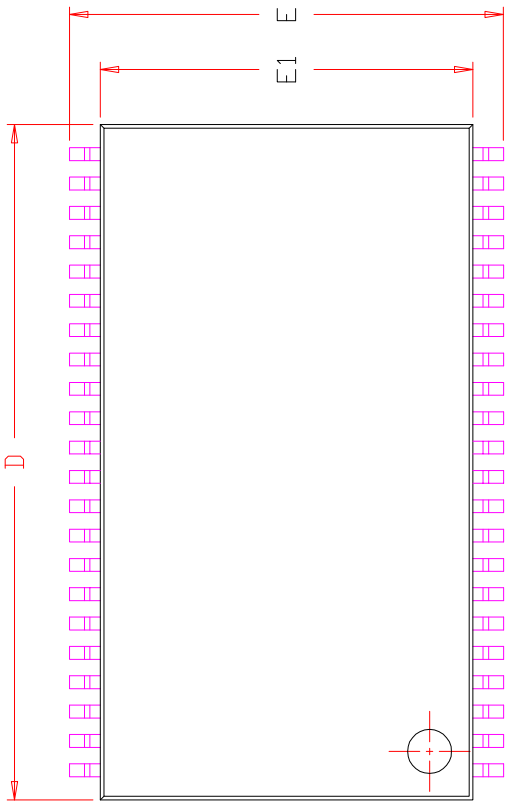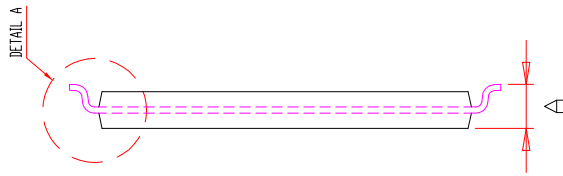
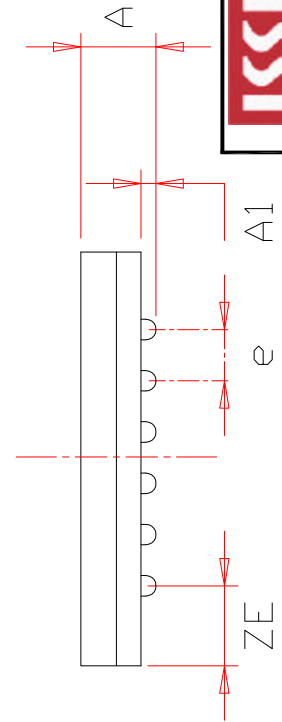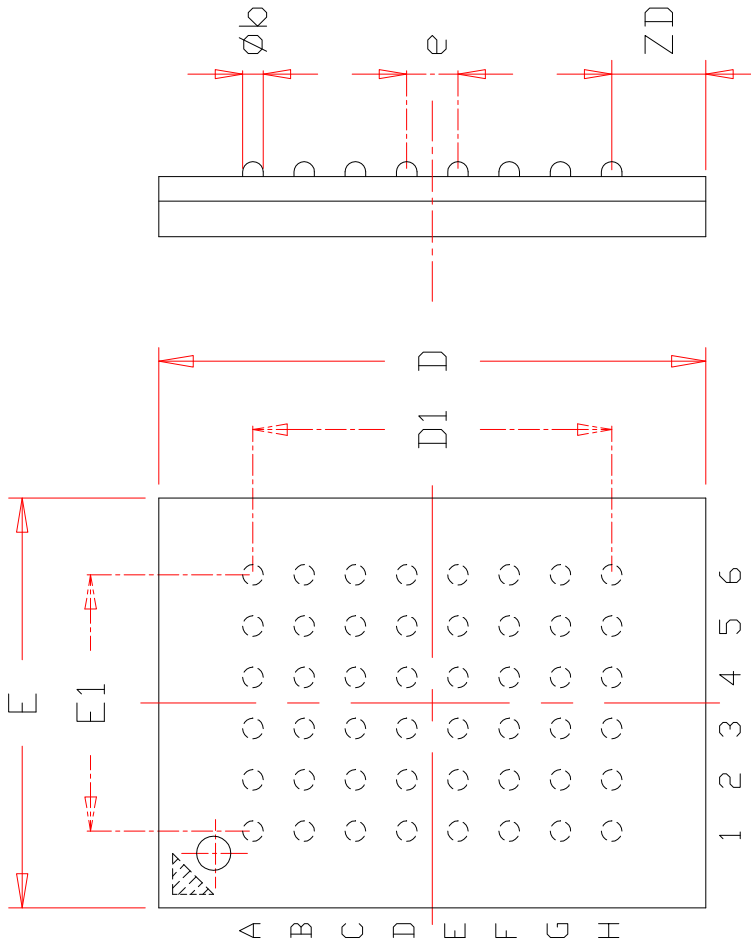| SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
Θ	0	—	8°	0	—	8°

NOTE :

1. CONTROLLING DIMENSION : MM

2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

DETAIL A

44L 400mil TSOP-2
Package Outline

TITLE	REV.	DATE
44L 400mil TSOP-2 Package Outline	F	06/04/2008

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25 BSC			0.207 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC.			0.030 BSC.		
ZD	1.375 REF.			0.054 REF.		
ZE	1.125 REF.			0.044 REF.		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

ISSI	**TITLE**	**48L 6x8mm TF-BGA** Package Outline	**REV.** **C**	**DATE** 08/12/2008

TOP VIEW