MC74LCX573

Low-Voltage CMOS Octal Transparent Latch Flow Through Pinout

With 5 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

The MC74LCX573 is a high performance, non−inverting octal transparent latch operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX573 inputs to be safely driven from 5.0 V devices.

The MC74LCX573 contains 8 D−type latches with 3−state standard outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH−to−LOW transition of LE. The 3−state standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are enabled. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches. The LCX573 flow through design facilitates easy PC board layout.

Features

- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5.0 V Tolerant − Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
  - Human Body Model >2000 V
  - Machine Model >200 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
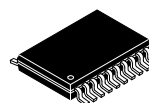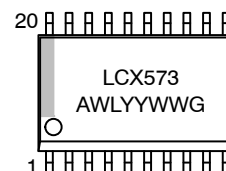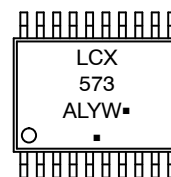
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http://onsemi.com

MARKING DIAGRAMS
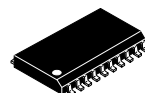
SOIC−20 WB
DW SUFFIX
CASE 751D

20
LCX573
AWLYYWWG
1

TSSOP−20
DT SUFFIX
CASE 948E

LCX
573
ALYW∎

A	=	Assembly Location
L, WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week
G or ∎	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.
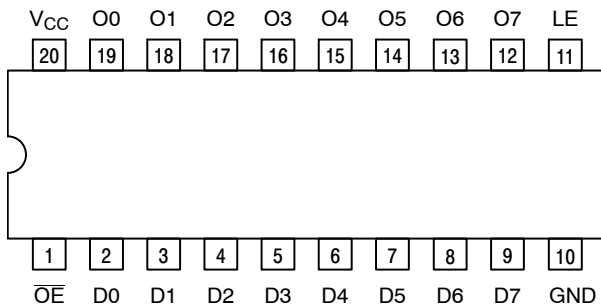
MC74LCX573

Figure 1. Pinout (Top View)

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs
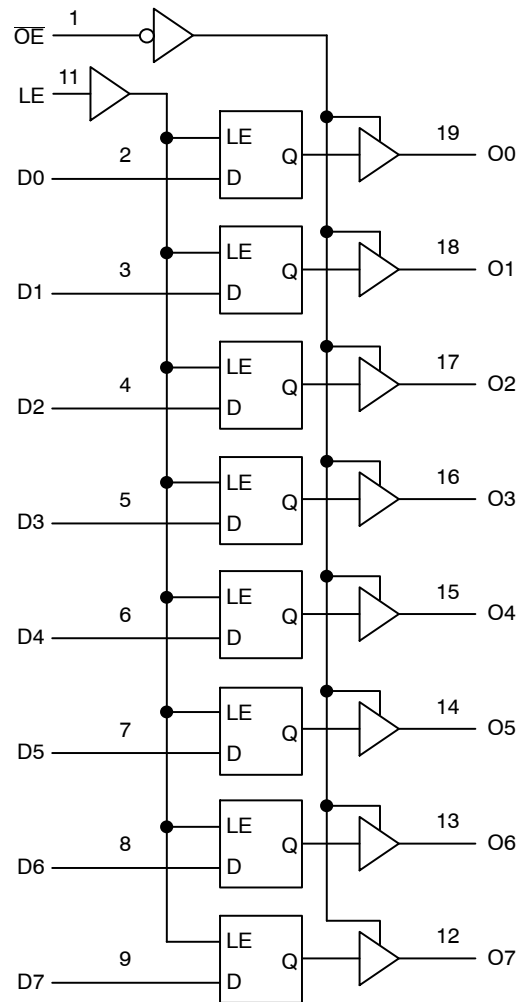
Figure 2. Logic Diagram

TRUTH TABLE

Inputs			Outputs	
$\overline{OE}$	LE	Dn	On	**Operating Mode**
L L	H H	H L	H L	Transparent (Latch Disabled); Read Latch
L L	L L	h l	H L	Latched (Latch Enabled) Read Latch
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H H	H H	H L	Z Z	Transparent (Latch Disabled); Disabled Outputs
H H	L L	h l	Z Z	Latched (Latch Enabled); Disabled Outputs

H = High Voltage Level;
h = High Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Latch Enable High–to–Low Transition
NC = No Change, State Prior to the Latch Enable High–to–Low Transition
X = High or Low Voltage Level or Transitions are Acceptable
Z = High Impedance State
For I_{CC} Reasons DO NOT FLOAT Inputs

MC74LCX573

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
V_{CC}	DC Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	$−0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$−0.5 \leq V_O \leq +7.0$	Output in 3−State	V
		$−0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I_{IK}	DC Input Diode Current	−50	$V_I <$ GND	mA
I_{OK}	DC Output Diode Current	−50	$V_O <$ GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage Operating Data Retention Only	 2.0 1.5	 2.5, 3.3 2.5, 3.3	 3.6 3.6	V
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3−State)	 0 0		 V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current V_{CC} = 3.0 V − 3.6 V V_{CC} = 2.7 V − 3.0 V V_{CC} = 2.3 V − 2.7 V			 −24 −12 −8	mA
I_{OL}	LOW Level Output Current V_{CC} = 3.0 V − 3.6 V V_{CC} = 2.7 V − 3.0 V V_{CC} = 2.3 V − 2.7 V			 +24 +12 +8	mA
T_A	Operating Free−Air Temperature	−55		+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V	0		10	ns/V

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74LCX573DWG	SOIC−20 (Pb−Free)	38 Units / Rail
MC74LCX573DWR2G	SOIC−20 (Pb−Free)	1000 Tape & Reel
MC74LCX573DTG	TSSOP−20 (Pb−Free)	75 Units / Rail
MC74LCX573DTR2G	TSSOP−20 (Pb−Free)	2500 Tape & Reel
NLV74LCX573DTR2G*	TSSOP−20 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	$T_A = -55°C$ to $+125°C$ Min	$T_A = -55°C$ to $+125°C$ Max	Units
V_{IH}	HIGH Level Input Voltage (Note 2)	$2.3\,V \leq V_{CC} \leq 2.7\,V$	1.7		1.7		V
		$2.7\,V \leq V_{CC} \leq 3.6\,V$	2.0		2.0		
V_{IL}	LOW Level Input Voltage (Note 2)	$2.3\,V \leq V_{CC} \leq 2.7\,V$		0.7		0.7	V
		$2.7\,V \leq V_{CC} \leq 3.6\,V$		0.8		0.8	
V_{OH}	HIGH Level Output Voltage	$2.3 \leq V_{CC} \leq 3.6\,V$; $I_{OL} = 100\,\mu A$	$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
		$V_{CC} = 2.3\,V$; $I_{OH} = -8\,mA$	1.8		1.8		
		$V_{CC} = 2.7\,V$; $I_{OH} = -12\,mA$	2.2		2.2		
		$V_{CC} = 3.0\,V$; $I_{OH} = -18\,mA$	2.4		2.4		
		$V_{CC} = 3.0\,V$; $I_{OH} = -24\,mA$	2.2		2.2		
V_{OL}	LOW Level Output Voltage	$2.3 \leq V_{CC} \leq 3.6\,V$; $I_{OL} = 100\,\mu A$		0.2		0.2	V
		$V_{CC} = 2.3\,V$; $I_{OL} = 8\,mA$		0.6		0.6	
		$V_{CC} = 2.7\,V$; $I_{OL} = 12\,mA$		0.4		0.4	
		$V_{CC} = 3.0\,V$; $I_{OL} = 16\,mA$		0.4		0.4	
		$V_{CC} = 3.0\,V$; $I_{OL} = 24\,mA$		0.55		0.60	
I_{OZ}	3-State Output Current	$V_{CC} = 3.6\,V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_{OUT} = 0$ to $5.5\,V$		± 5		± 5	μA
I_{OFF}	Power Off Leakage Current	$V_{CC} = 0$, $V_{IN} = 5.5\,V$ or $V_{OUT} = 5.5\,V$		10		10	μA
I_{IN}	Input Leakage Current	$V_{CC} = 3.6\,V$, $V_{IN} = 5.5\,V$ or GND		± 5		± 5	μA
I_{CC}	Quiescent Supply Current	$V_{CC} = 3.6\,V$, $V_{IN} = 5.5\,V$ or GND		10		10	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.3 \leq V_{CC} \leq 3.6\,V$; $V_{IH} = V_{CC} - 0.6\,V$		500		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS $t_R = t_F = 2.5$ ns; $R_L = 500\,\Omega$

			Limits $T_A = -55°C$ to $+125°C$						
			$V_{CC} = 3.3\,V \pm 0.3\,V$ $C_L = 50\,pF$		$V_{CC} = 2.7\,V$ $C_L = 50\,pF$		$V_{CC} = 2.5\,V \pm 0.2\,V$ $C_L = 30\,pF$		
Symbol	Parameter	Waveform	Min	Max	Min	Max	Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	1	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	1.5 1.5	9.6 9.6	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	3	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	1.5 1.5	10.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH and LOW Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	1.5 1.5	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	1.5 1.5	7.8 7.8	ns
t_s	Setup TIme, HIGH or LOW D_n to LE	3	2.5		2.5		4.0		
t_h	Hold TIme, HIGH or LOW D_n to LE	3	1.5		1.5		2.0		
t_w	LE Pulse Width, HIGH	3	3.3		3.3		4.0		
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note 3)			1.0 1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Units
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 4)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		0.8		V
		V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		0.6		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 4)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		−0.8		V
		V_{CC} = 2.5 V, C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V		−0.6		V

4. Number of outputs defined as "n". Measured with "n−1" outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	25	pF
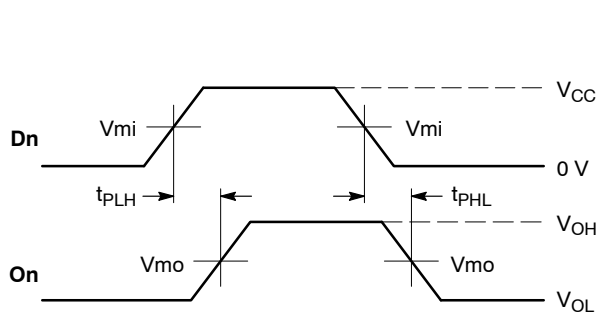
WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns
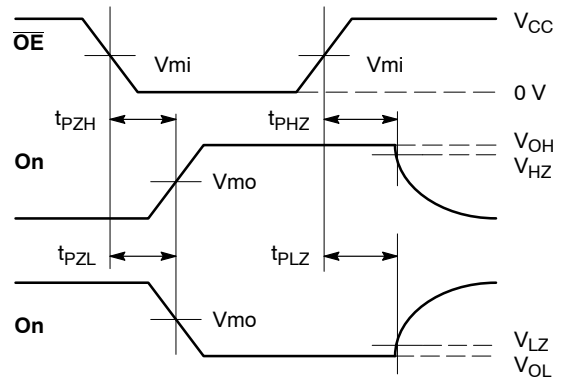
WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Symbol	V_{CC}		
	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V
Vmi	1.5 V	1.5 V	V_{CC}/2
Vmo	1.5 V	1.5 V	V_{CC}/2
V_{HZ}	V_{OL} + 0.3 V	V_{OL} + 0.3 V	V_{OL} + 0.15 V
V_{LZ}	V_{OL} − 0.3 V	V_{OL} − 0.3 V	V_{OL} − 0.15 V
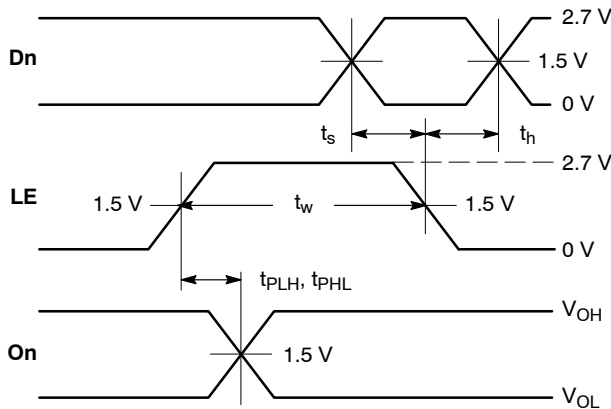
WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns except when noted

Figure 3. AC Waveforms

MC74LCX573
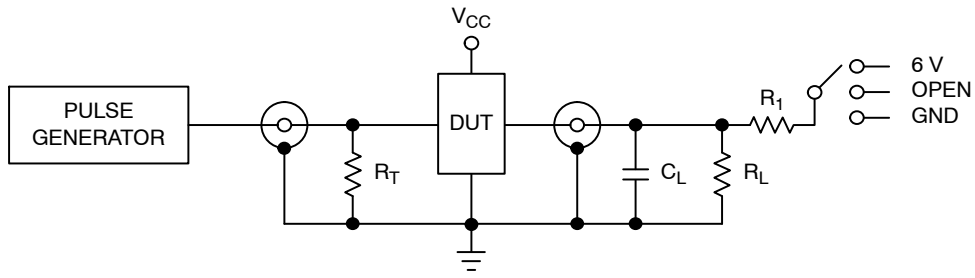
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V at V_{CC} = 3.3 ± 0.3 V 6 V at V_{CC} = 2.5 ± 0.2 V
Open Collector/Drain t_{PLH} and t_{PHL}	6 V
t_{PZH}, t_{PHZ}	GND

C_L = 50 pF at V_{CC} = 3.3 ± 0.3 V or equivalent (includes jig and probe capacitance)
C_L = 30 pF at V_{CC} = 2.5 ± 0.2 V or equivalent (includes jig and probe capacitance)
R_L = R_1 = 500 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 4. Test Circuit
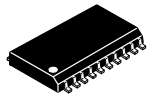
SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015

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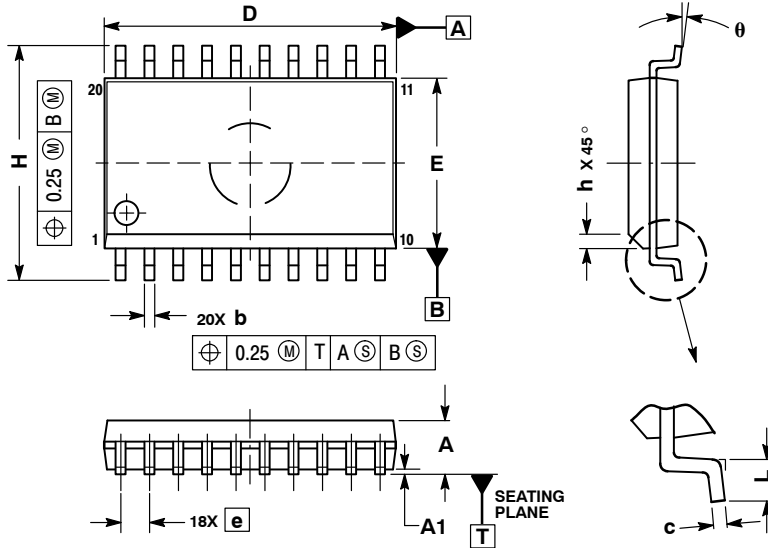
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

**RECOMMENDED
SOLDERING FOOTPRINT***

DIMENSIONS: MILLIMETERS
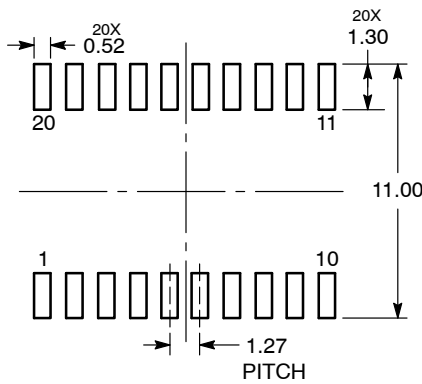
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***
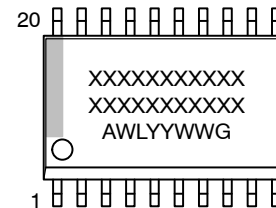
XXXXX = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
YY   = Year
WW   = Work Week
G   = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present.

DOCUMENT NUMBER:	**98ASB42343B**		
DESCRIPTION:	**SOIC−20 WB**		**PAGE 1 OF 1**

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1
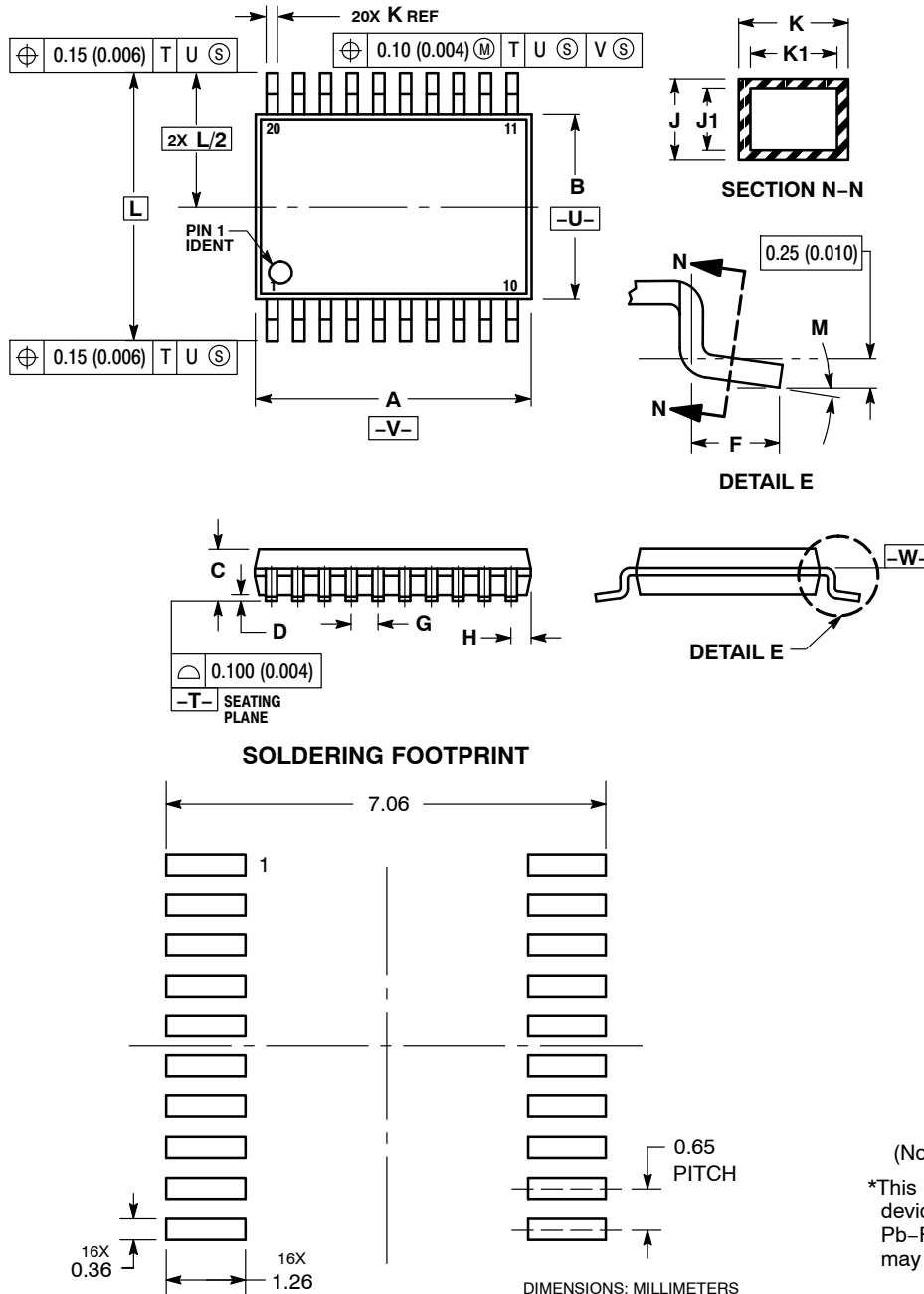
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

SECTION N−N

DETAIL E

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SEATING PLANE

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM***

XXXX
XXXX
ALYW▪
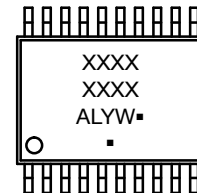
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

DOCUMENT NUMBER:	98ASH70169A		
DESCRIPTION:	TSSOP−20 WB		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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