

Notification Number:	20151012000	Notification Date:	10/15/2015
Title:	Datasheet update for DAC3484		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.

The product datasheet(s) is updated as seen in the change revision history below:



DAC3484

SLAS749D – MARCH 2011 – REVISED SEPTEMBER 2015

www.ti.com

Changes from Revision C (August 2012) to Revision D

Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1
• Added 196-ball 12x12mm BGA package to Description	1
• Added additional operation requirement for SLEEP pin if SLEEP pin is set to logic HIGH before and during device power up and initialization.	7
• Added additional circuit configuration for unused terminals - IOUTAP/N, IOUTBP/N, IOUTCP/N, IOUTDP/N	9
• Added additional operation requirement for SLEEP pin if SLEEP pin is set to logic HIGH before and during device power up and initialization.	10
• Changed DACCLKP/N Differential voltage TYP value from 1.0 V to 0.8 V	14
• Changed the parameter name Single-Ended Swing Level to Single-Ended Input Level to better reflect the specification for minimum recommended single-ended voltage level.	14
• Changed OSTRP/N Differential voltage TYP value from 1.0 V to 0.8 V	14
• Changed the parameter name Single-Ended Swing Level to Single-Ended Input Level to better reflect the specification for minimum recommended single-ended voltage level.	14
• Changed Standard high swing note for <i>Electrical Characteristics – Digital Specifications</i>	14
• Added Minimum voltage note for <i>Electrical Characteristics – Digital Specifications</i>	14
• Added LMK0480x family to note for <i>Timing Requirements – Digital Specifications</i>	16
• Added text to Input FIFO section	32
• Changed syncsel_fifoout(3:0) description in Input FIFO section to clarify the FIFO read pointer reset capture method and limitation.....	33
• Added Note to Input FIFO section	33
• Added LMK0480x family to Input FIFO section	33
• Changed text in Single Sync Source Mode to clarify the latency limitation of Single Sync Source Mode.....	35
• Added the effect of bypassing the FIFO in the Bypass Mode section to clarify the operation of the FIFO, LVDS	

FRAME, and LVDS SYNC in FIFO Bypass Mode.	35
• Added package information for LPF pin in PLL Mode section	37
• Changed table reference in FIR Filters section	38
• Added text to Data Pattern Checker section with additional operating recommendations.	49
• Added reference to application report in DAC3484 Alarm Monitoring section	53
• Added note to Figure 80	54
• Added <i>Unused LVDS Port Termination</i> section	55
• Changed information to Multi-Device Operation: Single Sync Source mode section to clarify the latency limitation of Single Sync Source Mode.	61
• Changed Figure 90 to clarify the latency limitation of Single Sync Source Mode.	62
• Changed the NCO setting description in the Example Start-up Sequence Section to reflect the example register writes.	64
• Added A32 to A32 for DAC3484IRKD and N9 for DAC3484IZAY in register config3 bit 0 description	70
• Changed alarm_lparity to alarm_fparity in register config7	72
• Changed QMC offset registers to QMC correction registers in register config16	74
• Added SLEEP pin information to register config27 bit 11	77
• Changed 1.2VDIG to DIGVDD in register config27 bits 5:0	77
• Changed 1.2VCLK to CLKVDD in register config27 bits 5:0	77
• Added pin description for both packages in register config35	80
• Added reference to Digital Input Timing Specifications Table in register config36	80
• Added text to register config45 bit 0 description	81

The datasheet number will be changing.

Device Family	Change From:	Change To:
DAC3484	SLAS749C	SLAS749D

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/dac3484>

Reason for Change:

To more accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this Notification:

None.

Product Affected:

DAC3484IRKD25	DAC3484IRKDT	DAC3484IZAYR
DAC3484IRKDR	DAC3484IZAY	

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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