- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 µA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**

- **Low Input Offset Voltage**
  950 µV Max at T_A = 25°C (TLV226xA)
- **Wide Supply Voltage Range**
  2.7 V to 8 V
- **Macromodel Included**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

description

The TLV2262 and TLV2264 are dual and quad low voltage operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single or split supply applications. The TLV226x family offers a compromise between the micropower TLV225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. This family is fully characterized at 3 V and 5 V and is optimized for low-voltage applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 µA (typ) of supply current per amplifier.

The TLV226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV226xA family is available and has a maximum input offset voltage of 950 µV.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 1

The TLV2262/4 also makes great upgrades to the TLV2332/4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.
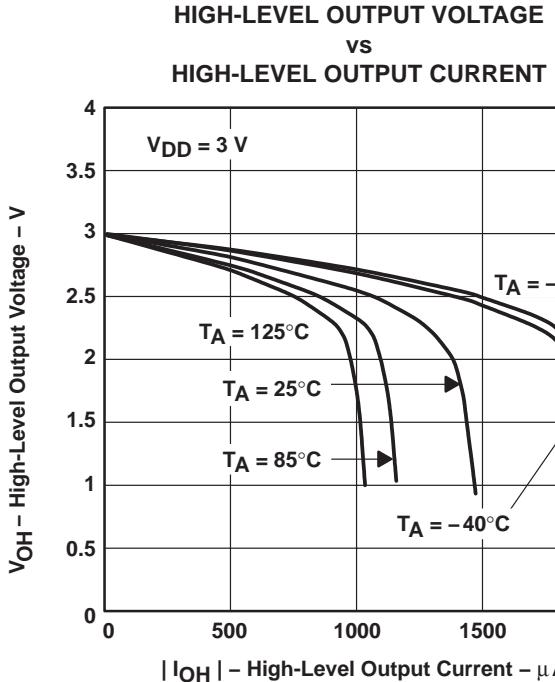
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TEXAS INSTRUMENTS

TLV2262 AVAILABLE OPTIONS

T_A	V_IOmax AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CERAMIC FLATPACK (U)
0°C to 70°C	2.5 mV	TLV2262CD	—	—	TLV2262CP	TLV2262CPWLE	—
−40°C to 125°C	950 µV 2.5 mV	TLV2262AID TLV2262ID	— —	— —	TLV2262AIP TLV2262IP	TLV2262AIPWLE —	— —
−40°C to 125°C	950 µV 2.5 mV	TLV2262AQD TLV2262QD	— —	— —	— —	— —	— —
−55°C to 125°C	950 µV 2.5 mV	— —	TLV2262AMFK TLV2262MFK	TLV2262AMJG TLV2262MJG	— —	— —	TLV2262AMU TLV2262MU

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2262CDR).
‡ The PW package is available only left-end taped and reeled.
§ Chips are tested at 25°C.
¶ For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

TLV2264 AVAILABLE OPTIONS

T_A	V_IOmax AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	CERAMIC FLATPACK (W)
−40°C to 125°C	950 µV 2.5 mV	TLV2264AID TLV2264ID	— —	— —	TLV2264AIN TLV2264IN	TLV2264AIPWLE —	— —
−40°C to 125°C	950 µV 2.5 mV	TLV2264AQD TLV2264QD	— —	— —	— —	— —	— —
−55°C to 125°C	950 µV 2.5 mV	— —	TLV2264AMFK TLV2264MFK	TLV2264AMJ TLV2264MJ	— —	— —	TLV2264AMW TLV2264MW

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2262IDR).
‡ The PW package is available only left-end taped and reeled.
§ Chips are tested at 25°C.
¶ For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

TEXAS INSTRUMENTS

TLV2262C, TLV2262AC
TLV2262I, TLV2262AI
TLV2262Q, TLV2262AQ
D, P, OR PW PACKAGE
(TOP VIEW)

1OUT	1	8 V_{DD+}
1IN−	2	7 2OUT
1IN+	3	6 2IN−
V_{DD-}/GND	4	5 2IN+
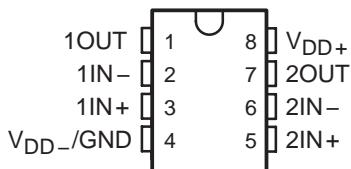
TLV2262M, TLV2262AM
JG PACKAGE
(TOP VIEW)

1OUT	1	8 V_{DD+}
1IN−	2	7 2OUT
1IN+	3	6 2IN−
V_{DD-}/GND	4	5 2IN+
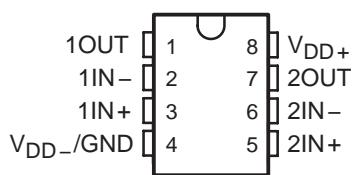
TLV2662M, TLV2262AM
U PACKAGE
(TOP VIEW)

NC	●1	10 NC
1OUT	2	9 V_{CC+}
1IN −	3	8 2OUT
1IN +	4	7 2IN −
V_{CC-}/GND	5	6 2IN +
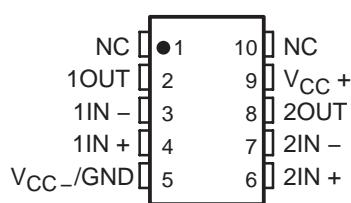
TLV2262M, TLV2262AM
FK PACKAGE
(TOP VIEW)

Top pins: NC, 1OUT, NC, V_{DD+}, NC (pins 3 2 1 20 19)

NC	4	18 NC
1IN −	5	17 2OUT
NC	6	16 NC
1IN +	7	15 2IN −
NC	8	14 NC

Bottom pins: 9 10 11 12 13 — NC, V_{DD-}/GND, NC, 2IN+, NC
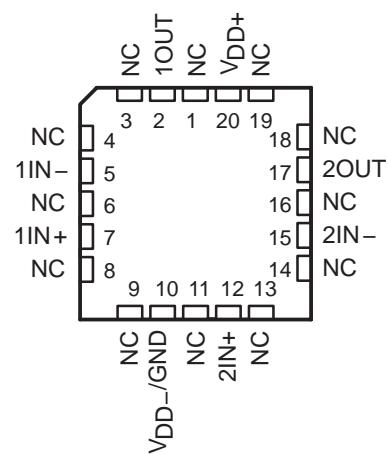
TLV2264I, TLV2264AI
TLV2264Q, TLV2264AQ
D, N, OR PW PACKAGE
(TOP VIEW)

1OUT	1	14 4OUT
1IN−	2	13 4IN−
1IN+	3	12 4IN+
V_{DD+}	4	11 V_{DD-}/GND
2IN+	5	10 3IN+
2IN−	6	9 3IN−
2OUT	7	8 3OUT
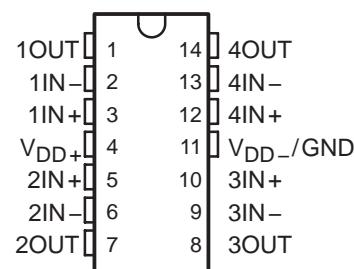
TLV2264M, TLV2264AM
J OR W PACKAGE
(TOP VIEW)

1OUT	1	14 4OUT
1IN−	2	13 4IN−
1IN+	3	12 4IN+
V_{DD+}	4	11 V_{DD-}/GND
2IN+	5	10 3IN+
2IN−	6	9 3IN−
2OUT	7	8 3OUT
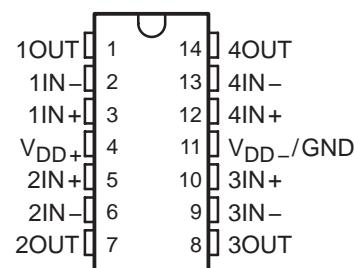
TLV2264M, TLV2264AM
FK PACKAGE
(TOP VIEW)
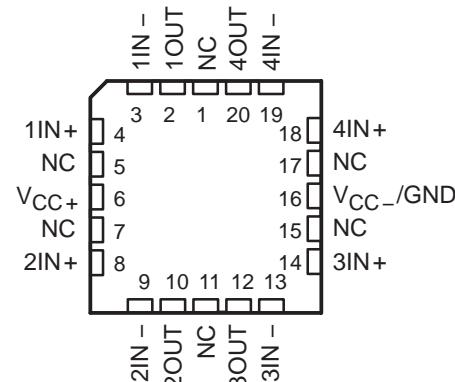
Top pins: 1IN −, 1OUT, NC, 4OUT, 4IN − (pins 3 2 1 20 19)

1IN+	4	18 4IN+
NC	5	17 NC
V_{CC+}	6	16 V_{CC-}/GND
NC	7	15 NC
2IN+	8	14 3IN+

Bottom pins: 9 10 11 12 13 — 2IN −, 2OUT, NC, 3OUT, 3IN −

3

TLV226x, TLV226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS
SLOS186C – FEBRUARY 1997 – REVISED AUGUST 2006

equivalent schematic (each amplifier)
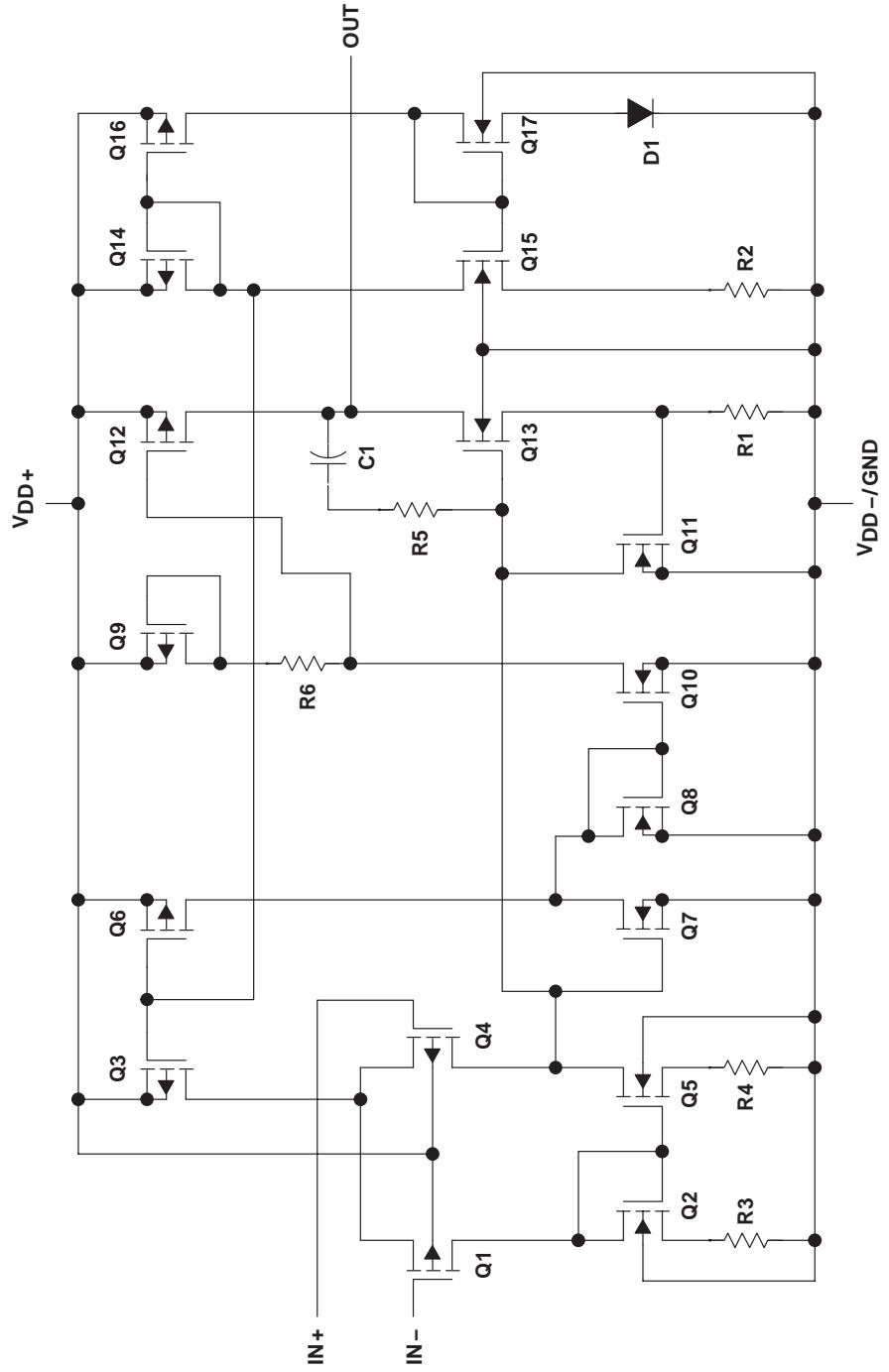
ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLV2252	TLV2254
Transistors	38	76
Resistors	28	54
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1) . . . . 16 V
Differential input voltage, V_{ID} (see Note 2) . . . . $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) . . . . $V_{DD-}-0.3$ V to V_{DD+}
Input current, I_I (each input) . . . . ±5 mA
Output current, I_O . . . . ±50 mA
Total current into V_{DD+} . . . . ±50 mA
Total current out of V_{DD-} . . . . ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) . . . . unlimited
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: I suffix . . . . −40°C to 125°C
                                      Q suffix . . . . −40°C to 125°C
                                       M suffix . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
           2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought
               below $V_{DD-} - 0.3$ V.
           3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum
               dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D–8	725 mW	5.8 mW/°C	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
J	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	—	210 mW
N	1150 mW	9.2 mW/°C	598 mW	—
P	1000 mW	8.0 mW/°C	520 mW	200 mW
PW–8	525 mW	4.2 mW/°C	273 mW	105 mW
PW–14	700 mW	5.6 mW/°C	364 mW	—
U	700 mW	5.5 mW/°C	—	150 mW
W	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions

	I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$ (see Note 1)	2.7	8	2.7	8	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-1.3$	V_{DD-}	$V_{DD+}-1.3$	V_{DD-}	$V_{DD+}-1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-1.3$	V_{DD-}	$V_{DD+}-1.3$	V_{DD-}	$V_{DD+}-1.3$	V
Operating free-air temperature, T_A	−40	125	−40	125	−55	125	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

TLV2262I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262I MIN	TLV2262I TYP	TLV2262I MAX	TLV2262AI MIN	TLV2262AI TYP	TLV2262AI MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $|V_{IO}|$ ≤ 5 mV		25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		2.99			2.99		V
		I_{OH} = −100 µA		25°C	2.85			2.85			
				Full range	2.825			2.825			
		I_{OH} = −400 µA		25°C	2.7			2.7			
				Full range	2.65			2.65			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 50 µA		25°C		10			10		mV
		V_{IC} = 1.5 V, I_{OL} = 500 µA		25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V, I_{OL} = 1 mA		25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	30			30			
			R_L = 1 MΩ‡	25°C		100			100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	100		dB
				Full range	80			80			

† Full range is – 40°C to 125°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2262I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262I			TLV2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is – 40°C to 125°C.

TLV2262I operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262I			TLV2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		395			395		kHz
t_S	Settling time	A_V = – 1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		55°			55°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 1.5 V

TLV2262I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2262I MIN	TLV2262I TYP	TLV2262I MAX	TLV2262AI MIN	TLV2262AI TYP	TLV2262AI MAX	UNIT
V_{IO}	Input offset voltage		25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5	60		0.5	60	pA
			85°C			150			150	
			Full range			800			800	
I_{IB}	Input bias current		25°C		1	60		1	60	pA
			85°C			150			150	
			Full range			800			800	
V_{ICR}	Common-mode input voltage range	$|V_{IO}|$ ≤5 mV, R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA	25°C		4.99			4.99		V
		I_{OH} = −100 μA	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		I_{OH} = −400 μA	25°C	4.7	4.85		4.7	4.85		
			Full range	4.6			4.6			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
			Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
			Full range	55			55			
		R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_O	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2262I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262I			TLV2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is – 40°C to 125°C.

TLV2262I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262I			TLV2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_S	Settling time	A_V = – 1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

TLV2264I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264I			TLV2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD±}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S= 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
$α_{VIO}$	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $|V_{IO}|$ ≤5 mV		25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.99			2.99		V
		I_{OH} = −100 μA		25°C	2.85			2.85			
				Full range	2.825			2.825			
		I_{OH} = −400 μA		25°C	2.7			2.7			
				Full range	2.65			2.65			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 50 μA		25°C		10			10		mV
		V_{IC} = 1.5 V, I_{OL} = 500 μA		25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V, I_{OL} = 1 mA		25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	30			30			
			R_L = 1 MΩ‡	25°C		100			100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($ΔV_{DD}/ΔV_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	100		dB
				Full range	80			80			

† Full range is − 40°C to 125°C.
‡ Referenced to 1.5 V
NOTE 4:   Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLV2264I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2264I			TLV2264AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 1.5 V, No load	25°C		0.8	1		0.8	1	mA
			Full range			1			1	

† Full range is – 40°C to 125°C.

TLV2264I operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264I			TLV2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.7 V to 1.7 V, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		µV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		395			395		kHz
t_s	Settling time	A_V = –1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		µs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		55°			55°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 1.5 V

TLV2264I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A [†]	TLV2264I MIN	TLV2264I TYP	TLV2264I MAX	TLV2264AI MIN	TLV2264AI TYP	TLV2264AI MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \leq 5$ mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99			4.99		V
		I_{OH} = −100 µA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 µA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.6			4.6			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ[‡]	25°C	80	170		80	170		V/mV
				Full range	55			55			
			R_L = 1 MΩ[‡]	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	95		dB
				Full range	80			80			

[†] Full range is − 40°C to 125°C.
[‡] Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2264I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2264I			TLV2264AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load	25°C		0.8	1		0.8	1	mA
			Full range			1			1	

† Full range is – 40°C to 125°C.

TLV2264I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264I			TLV2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_S	Settling time	A_V = – 1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is – 40°C to 125°C.
‡ Referenced to 2.5 V

TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$|V_{IO}| \leq$ 5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.99			2.99		V
		I_{OH} = −100 μA		25°C	2.85			2.85			
				Full range	2.82			2.82			
		I_{OH} = −400 μA		25°C	2.7			2.7			
				Full range	2.55			2.55			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 μA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		100	150		100	150	
				Full range			165			165	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200	300		200	300	
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	25			25			
			R_L = 1 MΩ‡	25°C		100			100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, $V_{IC} = V_{DD}/2$, No load		25°C	80	95		80	100		dB
				Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current	V_O = 1.5 V, No load	25°C		400	500		400	500	μA
			Full range			500			500	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLV2262Q and TLV2262M operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 1.7 V, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		395			395		kHz
t_S	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
$φ_m$	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		55°			55°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V

TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5	60		0.5	60	pA
			125°C			800			800	
I_{IB}	Input bias current		25°C		1	60		1	60	pA
			125°C			800			800	
V_{ICR}	Common-mode input voltage range	$|V_{IO}|$ ≤5 mV, R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA	25°C		4.99			4.99		V
		I_{OH} = −100 μA	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		I_{OH} = −400 μA	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
			Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
			Full range	50			50			
		R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

NOTE 4:   Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.

TLV2262Q and TLV2262M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V

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TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $|V_{IO}|$ ≤5 mV		25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.99			2.99		V
		I_{OH} = −100 μA		25°C	2.85			2.85			
				Full range	2.82			2.82			
		I_{OH} = −400 μA		25°C	2.7			2.7			
				Full range	2.6			2.6			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 μA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		100	150		100	150	
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200	300		200	300	
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	25			25			
			R_L = 1 MΩ‡	25°C		100			100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio (ΔV$_{DD}$/ΔV$_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	100		dB
				Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, V$_{DD}$ = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T$_A$†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I$_{DD}$	Supply current (four amplifiers)	V$_O$ = 1.5 V, No load	25°C		0.8	1		0.8	1	mA
			Full range			1			1	

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.

TLV2264Q and TLV2264M operating characteristics at specified free-air temperature, V$_{DD}$ = 3 V

PARAMETER		TEST CONDITIONS		T$_A$†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V$_O$ = 0.5 V to 1.7 V, C$_L$ = 100 pF‡	R$_L$ = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V$_n$	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
V$_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I$_n$	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V$_O$ = 0.5 V to 2.5 V, f = 20 kHz, R$_L$ = 50 kΩ‡	A$_V$ = 1	25°C		0.03%			0.03%		
			A$_V$ = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C$_L$ = 100 pF‡	R$_L$ = 50 kΩ‡,	25°C		0.67			0.67		MHz
B$_{OM}$	Maximum output-swing bandwidth	V$_{O(PP)}$ = 1 V, R$_L$ = 50 kΩ‡,	A$_V$ = 1, C$_L$ = 100 pF‡	25°C		395			395		kHz
t$_S$	Settling time	A$_V$ = –1, Step = 1 V to 2 V, R$_L$ = 50 kΩ‡, C$_L$ = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
φ$_m$	Phase margin at unity gain	R$_L$ = 50 kΩ‡,	C$_L$ = 100 pF‡	25°C		55°			55°		
	Gain margin			25°C		11			11		dB

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 1.5 V

TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
			Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5	60		0.5	60	pA
			125°C			800			800	
I_{IB}	Input bias current		25°C		1	60		1	60	pA
			125°C			800			800	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert$ ≤5 mV, R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA	25°C		4.99			4.99		V
		I_{OH} = −100 μA	25°C	4.85	4.94		4.85	4.94		
			Full range	4.82			4.82			
		I_{OH} = −400 μA	25°C	4.7	4.85		4.7	4.85		
			Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
			Full range			0.15			0.15	
		V_{IC} = 2.5 V, I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
			Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡ 25°C	80	170		80	170		V/mV
			Full range	50			50			
			R_L = 1 MΩ‡ 25°C		550			550		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	83		70	83		dB
			Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, V_DD = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLV2264Q and TLV2264M operating characteristics at specified free-air temperature, V_DD = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_S	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TYPICAL CHARACTERISTICS

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THD + N	Total harmonic distortion plus noise	vs Frequency	54
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	55 56
ϕ_m	Phase margin	vs Frequency vs Load capacitance	26, 27 57
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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

841 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 1.5$ V
$T_A = 25°C$
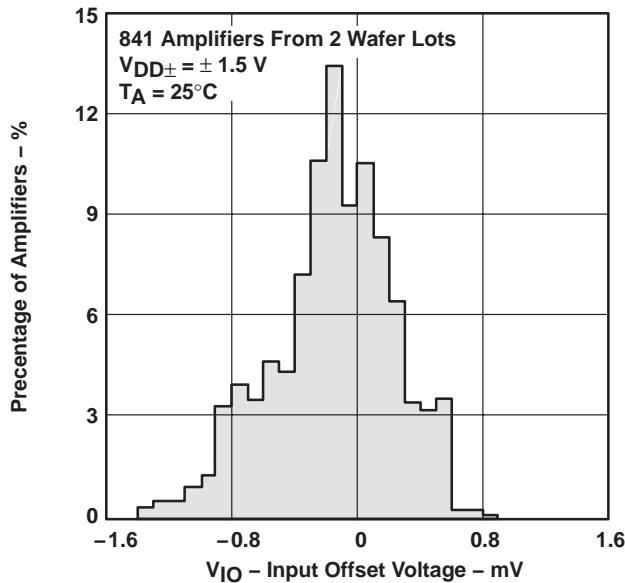
Figure 2

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

841 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 2.5$ V
$T_A = 25°C$
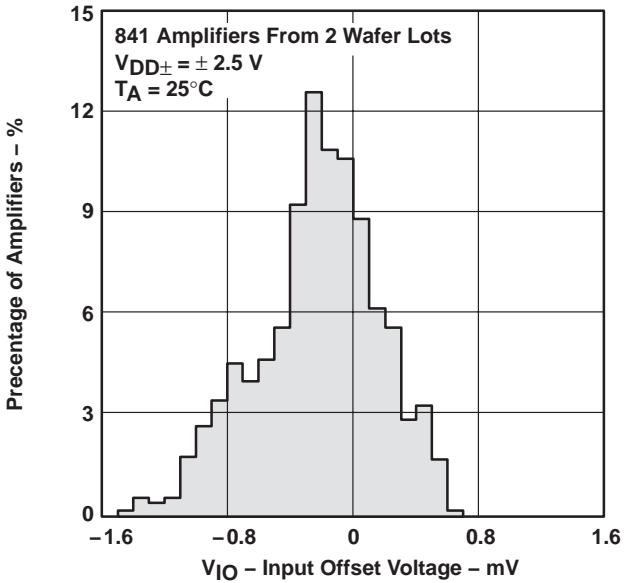
Figure 3

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE

2272 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 1.5$ V
$T_A = 25°C$
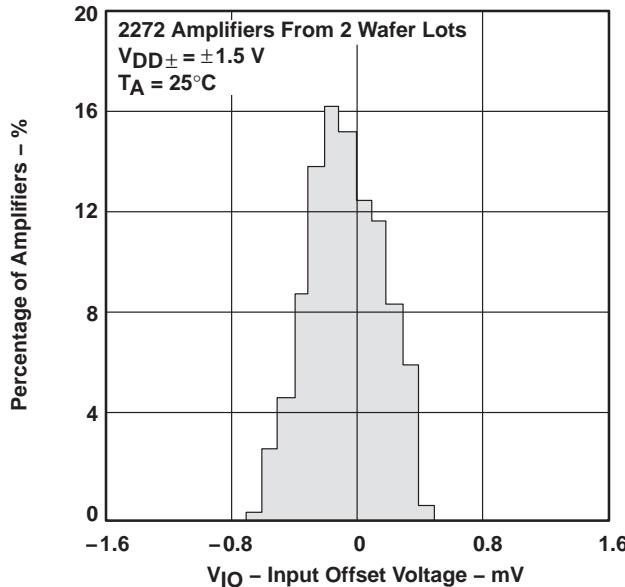
Figure 4

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE
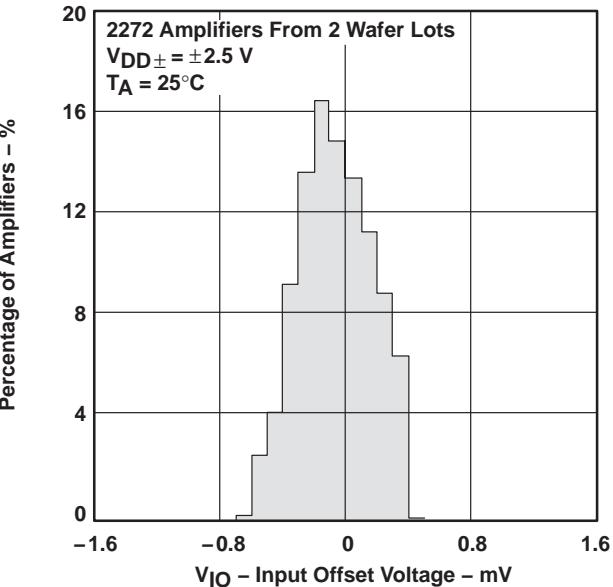
2272 Amplifiers From 2 Wafer Lots
$V_{DD\pm} = \pm 2.5$ V
$T_A = 25°C$

Figure 5

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TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE

V_{DD} = 3 V
R_S = 50 Ω
T_A = 25°C

Figure 6

INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE

V_{DD} = 5 V
R_S = 50 Ω
T_A = 25°C

Figure 7

DISTRIBUTION OF TLV2262 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

128 Amplifiers From 2 Wafer Lots
$V_{DD\pm}$ = ±1.5 V
P Package
T_A = 25°C to 85°C

Figure 8

DISTRIBUTION OF TLV2262 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

128 Amplifiers From 2 Wafer Lots
$V_{DD\pm}$ = ±2.5 V
P Package
T_A = 25°C to 85°C
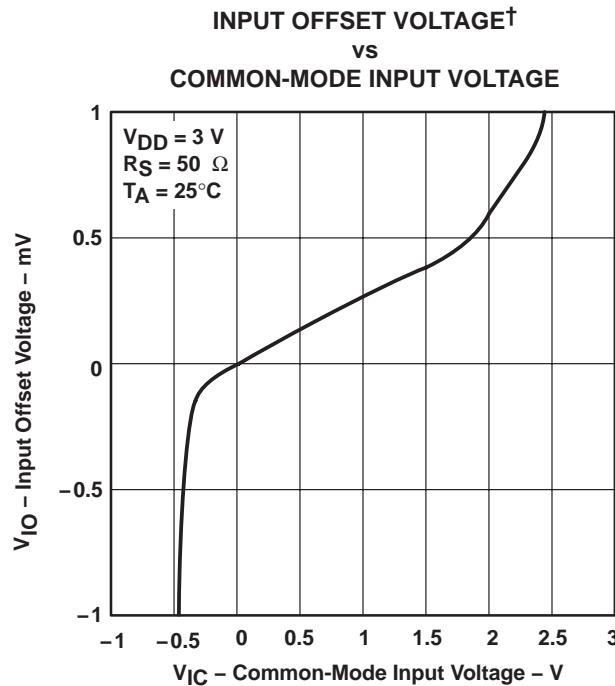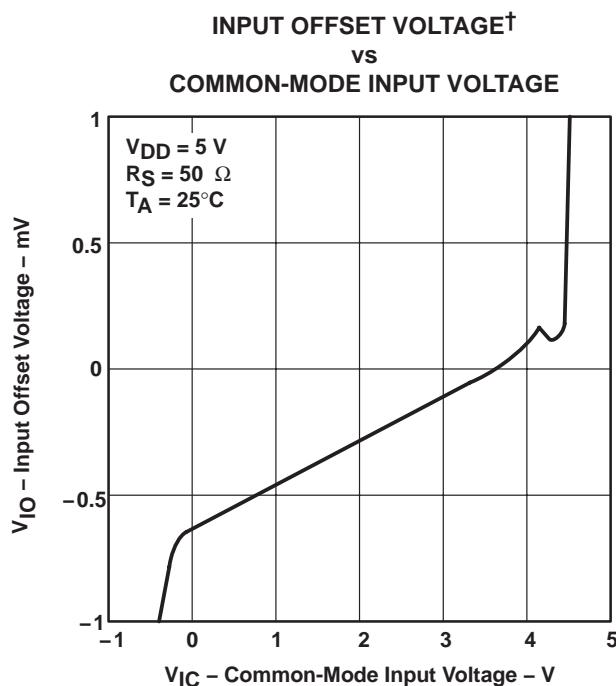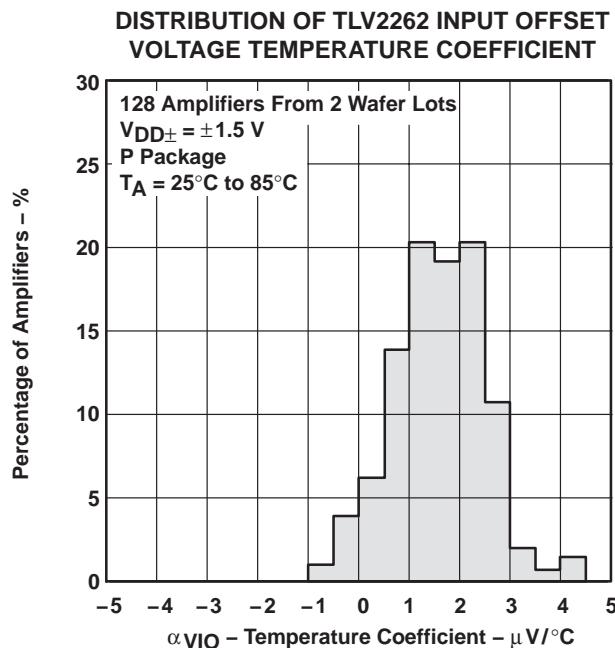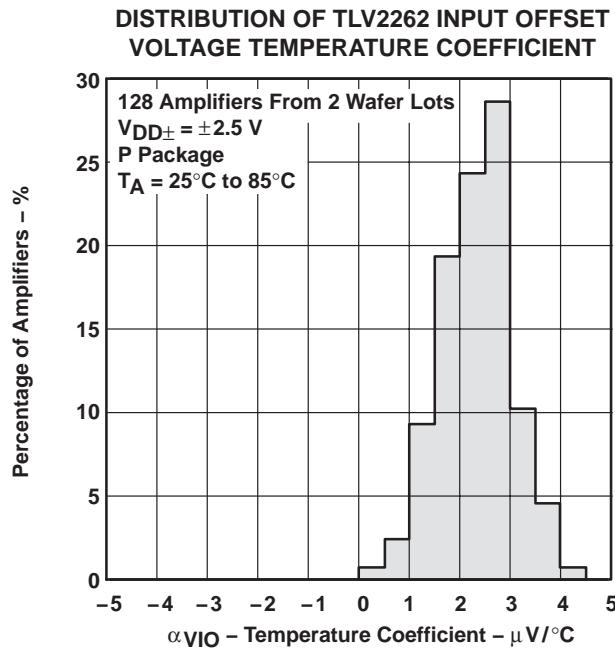
Figure 9

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2264 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

128 Amplifiers From
2 Wafer Lots
$V_{DD\pm} = \pm 1.5$ V
N Package
$T_A = 25°C$ to $125°C$

α_{VIO} – Temperature Coefficient
of Input Offset Voltage – $\mu V/°C$

Percentage of Amplifiers – %

Figure 10

DISTRIBUTION OF TLV2264 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

128 Amplifiers From
2 Wafer Lots
$V_{DD\pm} = \pm 2.5$ V
N Package
$T_A = 25°C$ to $125°C$

α_{VIO} – Temperature Coefficient
of Input Offset Voltage – $\mu V/°C$

Percentage of Amplifiers – %

Figure 11

INPUT BIAS AND INPUT OFFSET CURRENTS†
vs
FREE-AIR TEMPERATURE

$V_{DD\pm} = \pm 2.5$ V
$V_{IC} = 0$
$V_O = 0$
$R_S = 50$ Ω

I_{IB}

I_{IO}

I_{IB} and I_{IO} – Input Bias and Input Offset Currents – pA

T_A – Free-Air Temperature – °C

Figure 12

INPUT VOLTAGE
vs
SUPPLY VOLTAGE

$R_S = 50$ Ω
$T_A = 25°C$

$| V_{IO} | \leq 5$ mV

V_I – Input Voltage – V

$|V_{DD\pm}|$ – Supply Voltage – V

Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE†‡
vs
FREE-AIR TEMPERATURE

Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 15

LOW-LEVEL OUTPUT VOLTAGE‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT
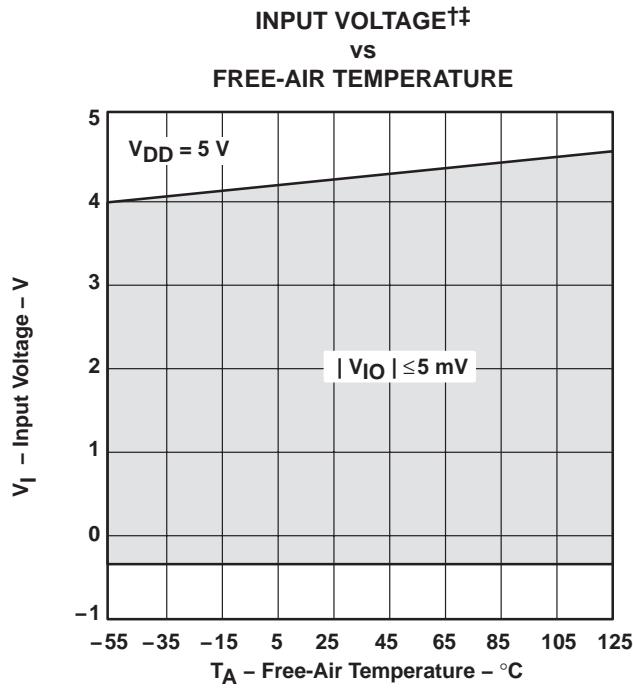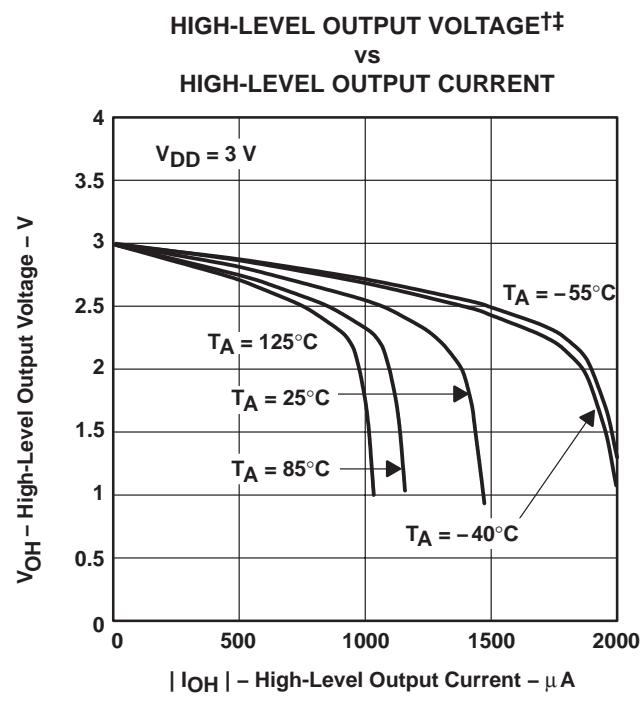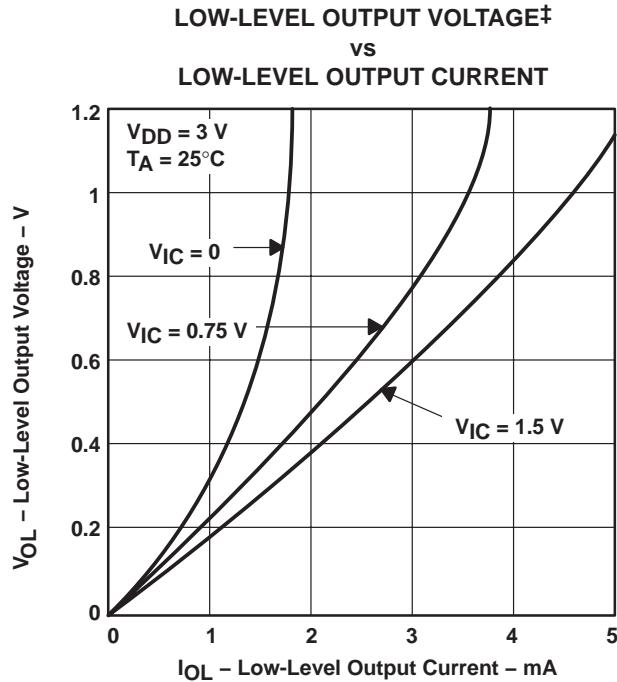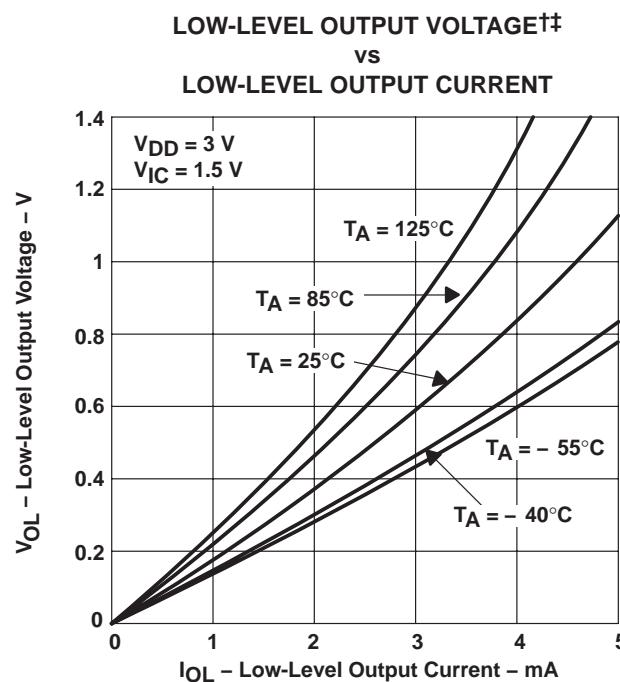
Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 18

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡
vs
FREQUENCY

Figure 20

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE
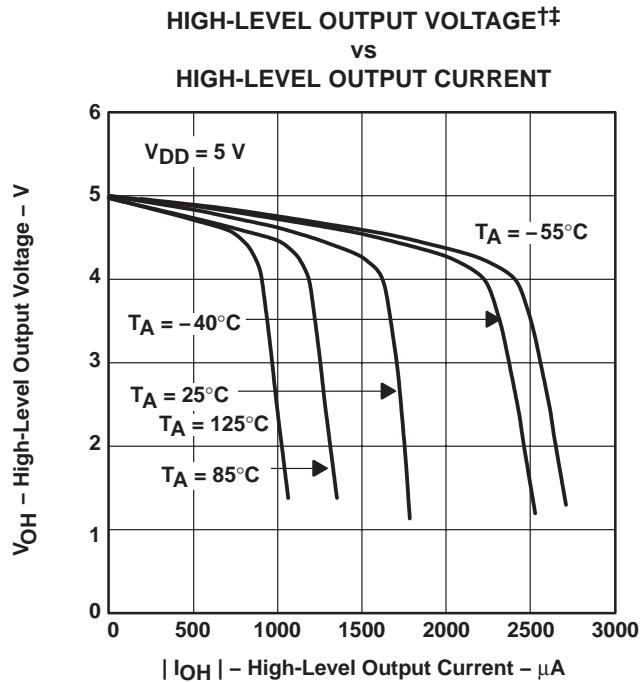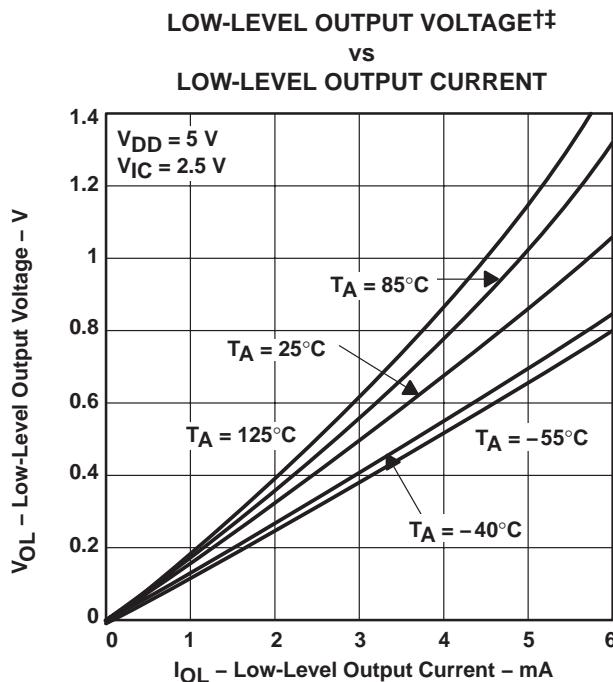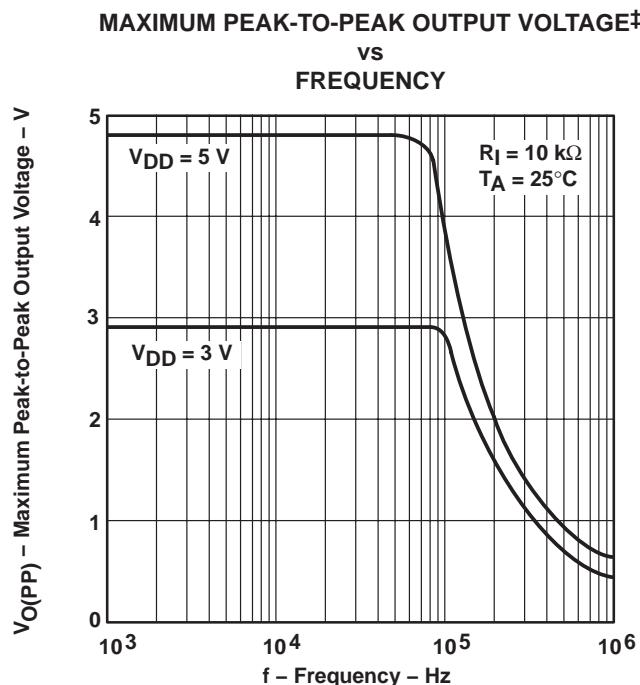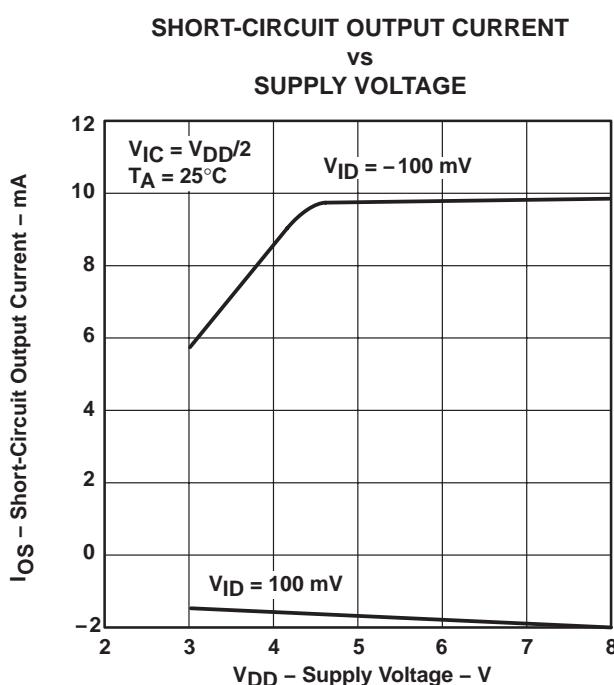
Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TLV226x, TLV226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS186C – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

Figure 22

DIFFERENTIAL INPUT VOLTAGE‡
vs
OUTPUT VOLTAGE

Figure 23

DIFFERENTIAL INPUT VOLTAGE‡
vs
OUTPUT VOLTAGE

Figure 24

DIFFERENTIAL VOLTAGE AMPLIFICATION‡
vs
LOAD RESISTANCE
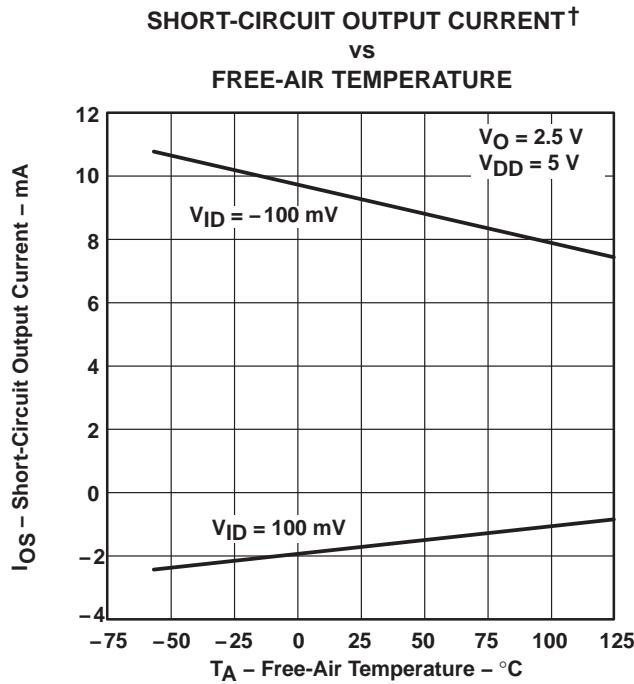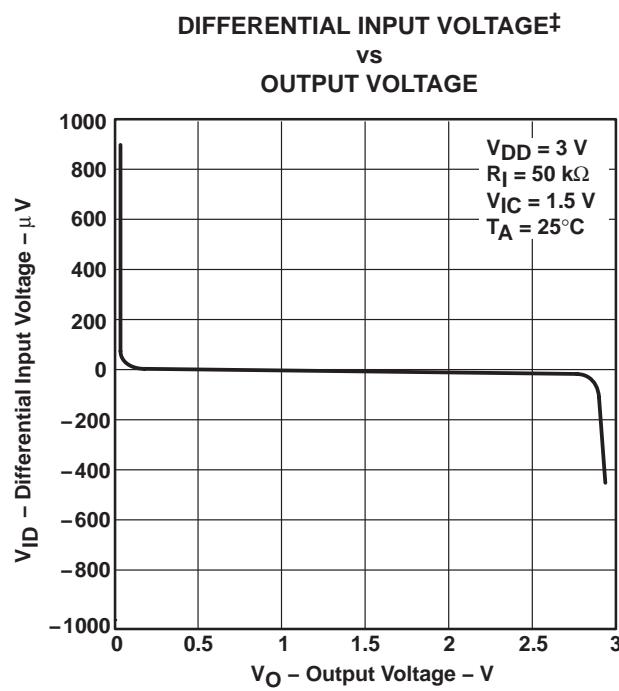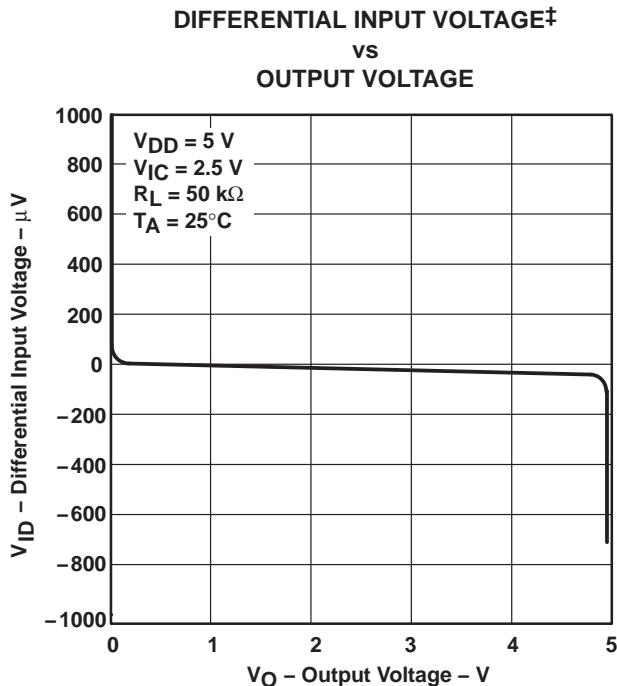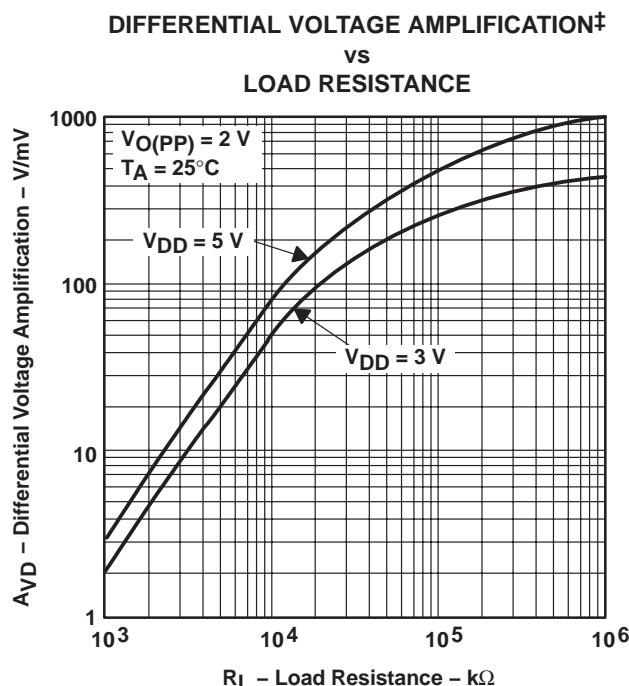
Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN†
vs
FREQUENCY**

Figure 26

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN†
vs
FREQUENCY**
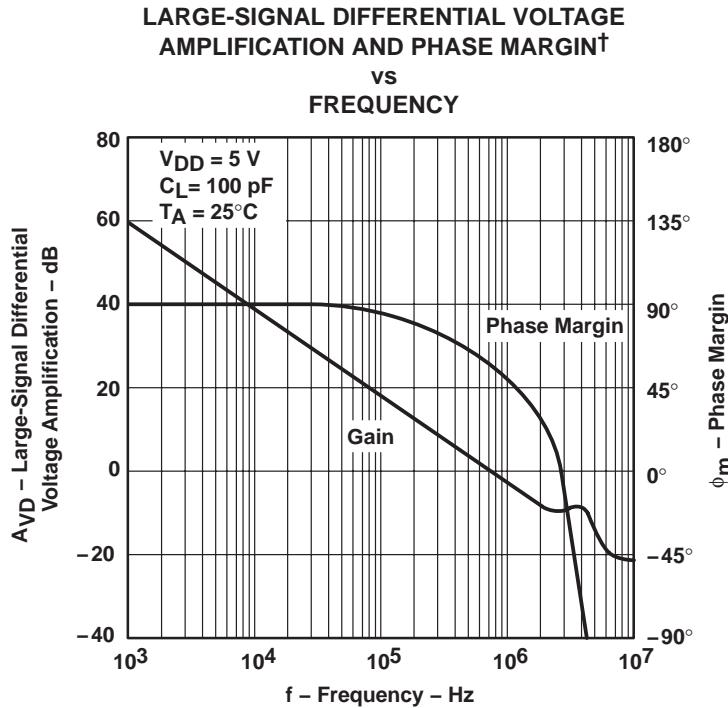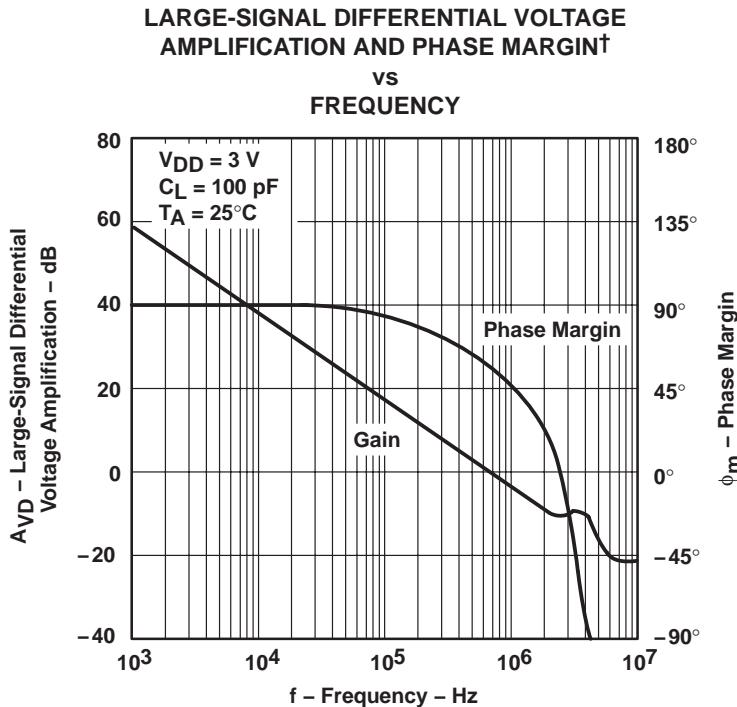
Figure 27

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TLV226x, TLV226xA
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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE

Figure 28

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE

Figure 29

OUTPUT IMPEDANCE‡
vs
FREQUENCY


Figure 30

OUTPUT IMPEDANCE‡
vs
FREQUENCY
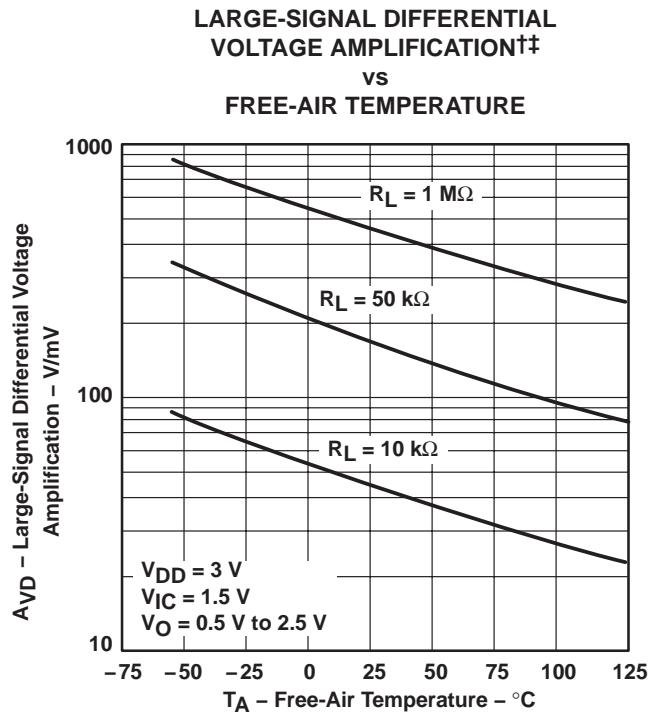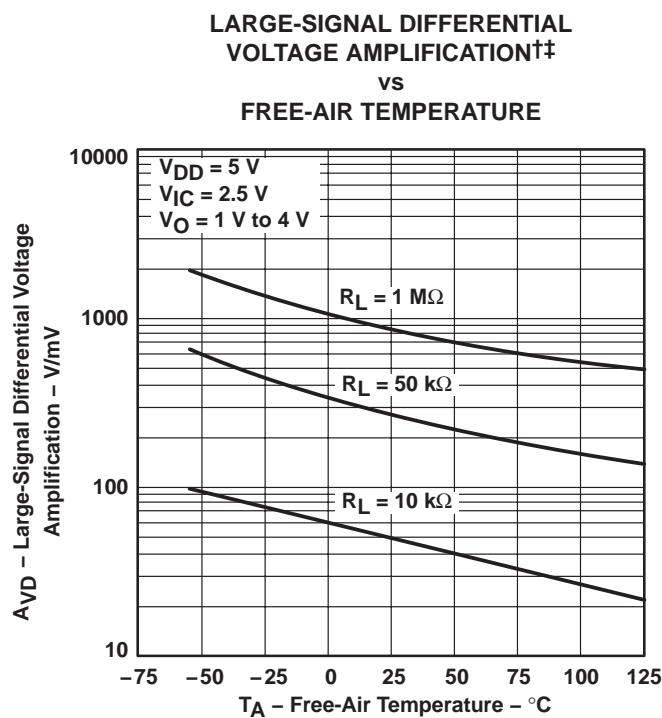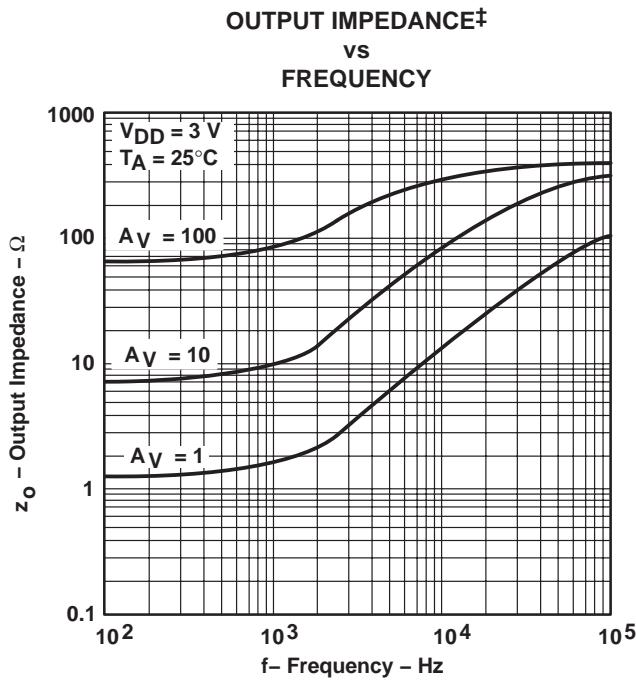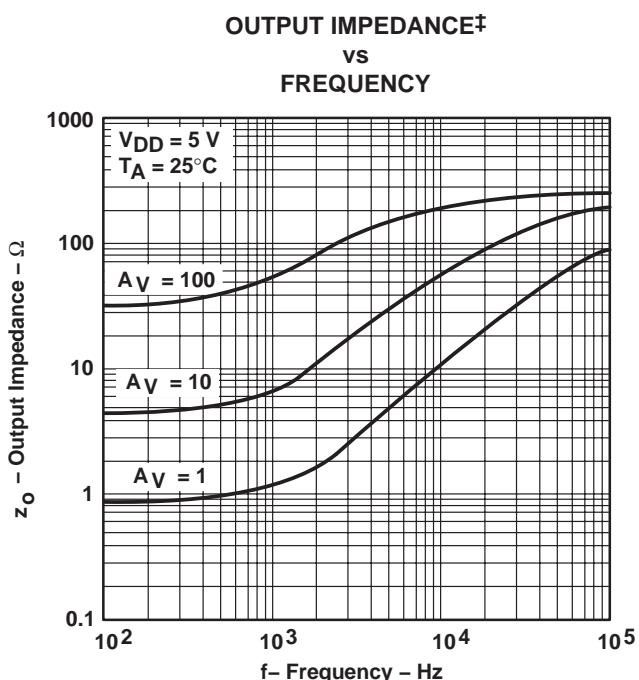
Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO†
vs
FREQUENCY

Figure 32

COMMON-MODE REJECTION RATIO†‡
vs
FREE-AIR TEMPERATURE

Figure 33

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREQUENCY

Figure 34

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREQUENCY
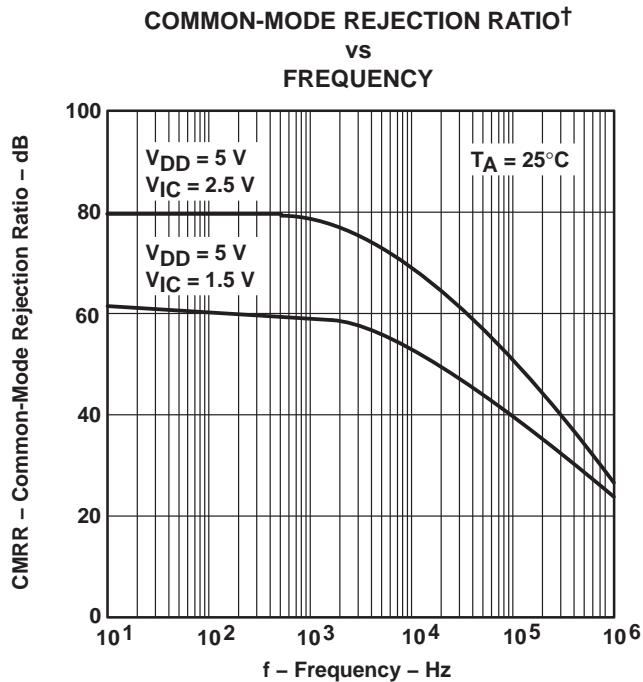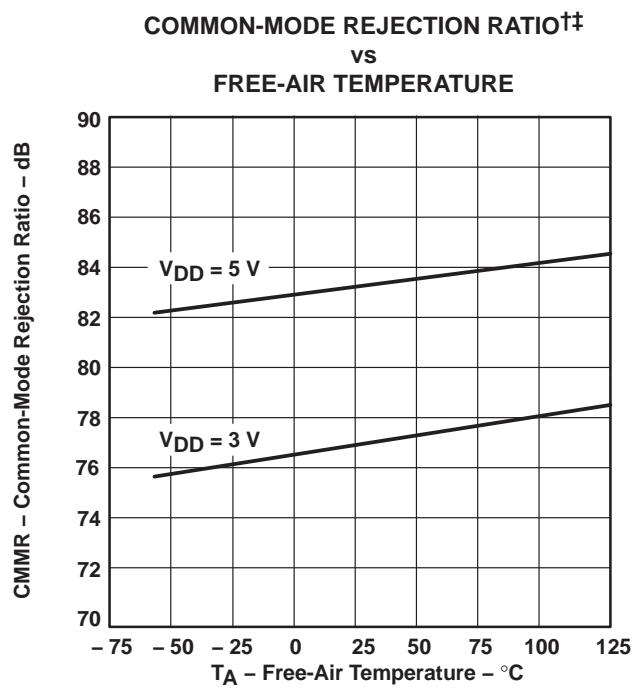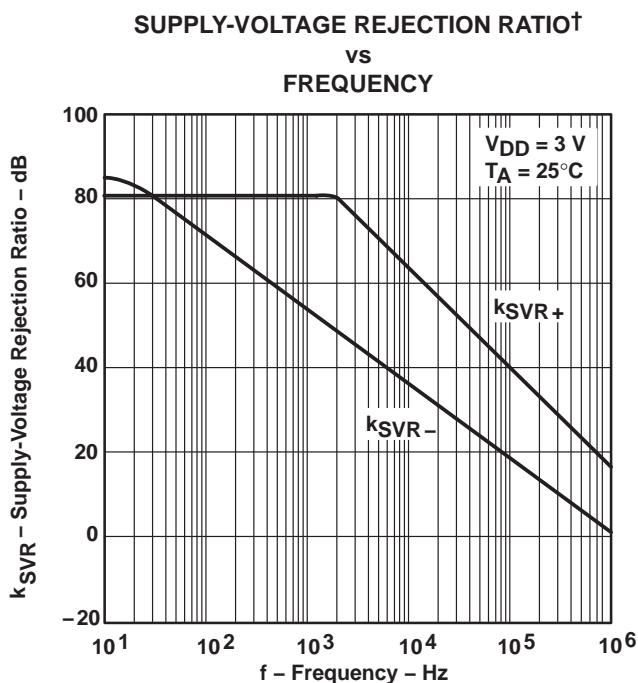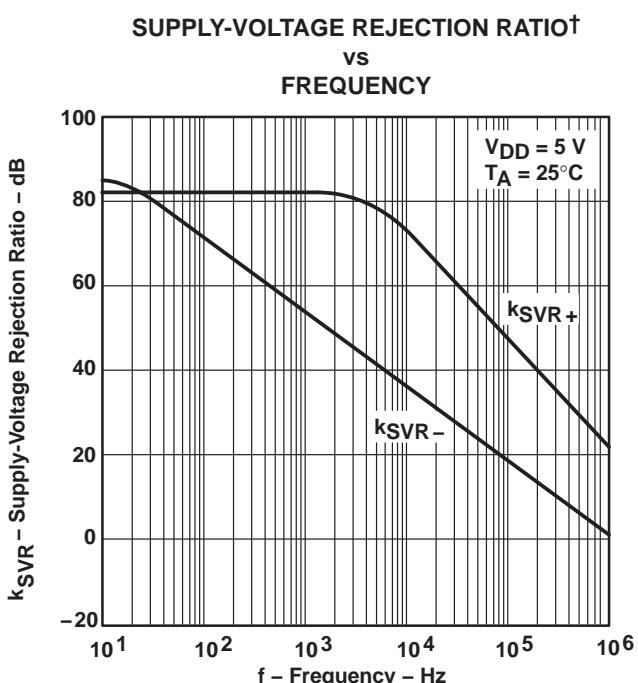
Figure 35

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

TLV2262
SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

Figure 36

TLV2264
SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

Figure 37

TLV2262
SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE

Figure 38

TLV2264
SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE
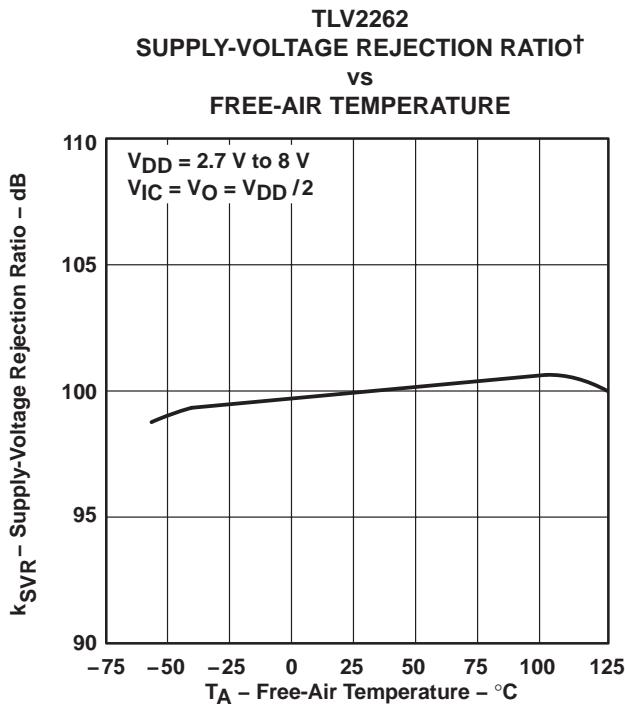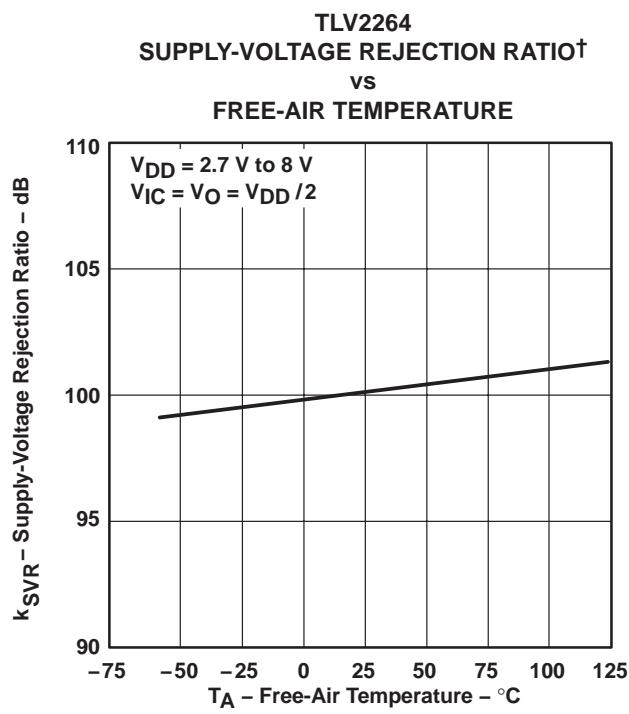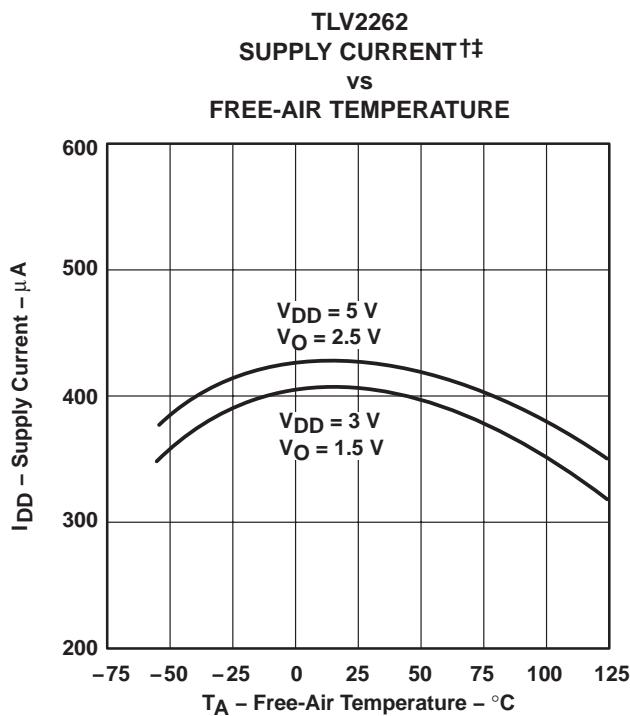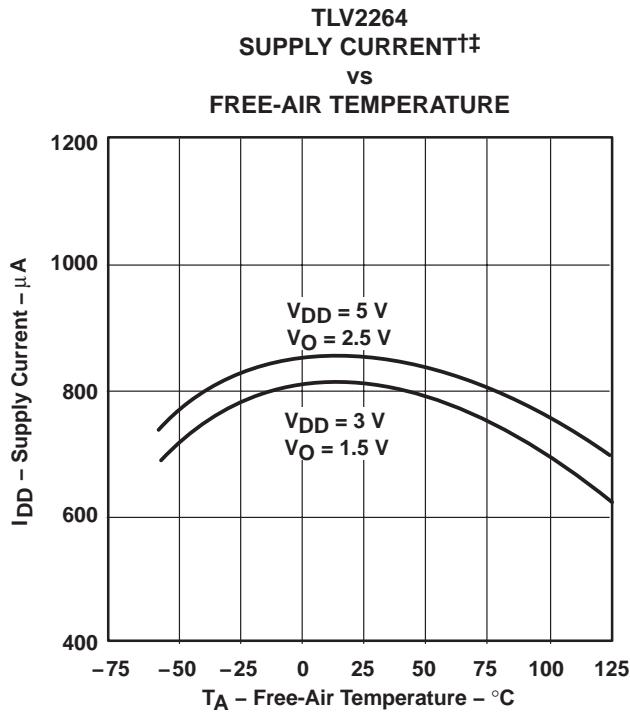
Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

SLEW RATE†
vs
LOAD CAPACITANCE

Figure 40

SLEW RATE†‡
vs
FREE-AIR TEMPERATURE

Figure 41

INVERTING LARGE-SIGNAL PULSE
**RESPONSE†**

Figure 42

INVERTING LARGE-SIGNAL PULSE
RESPONSE†
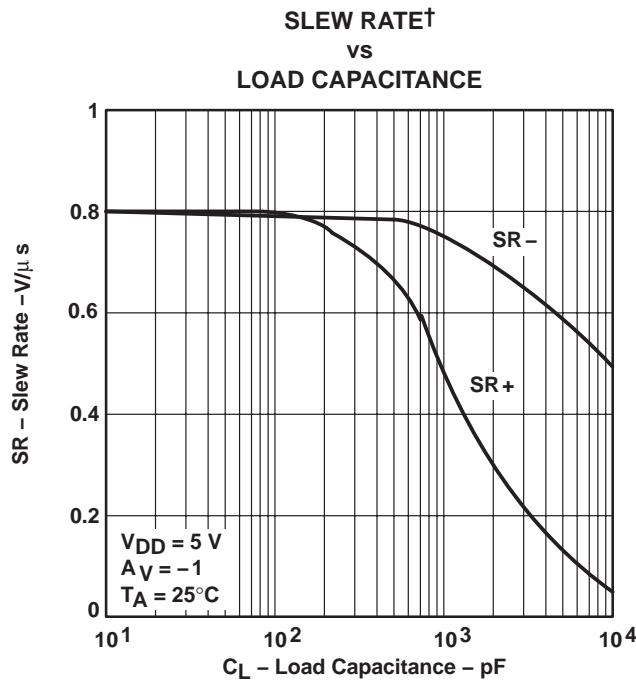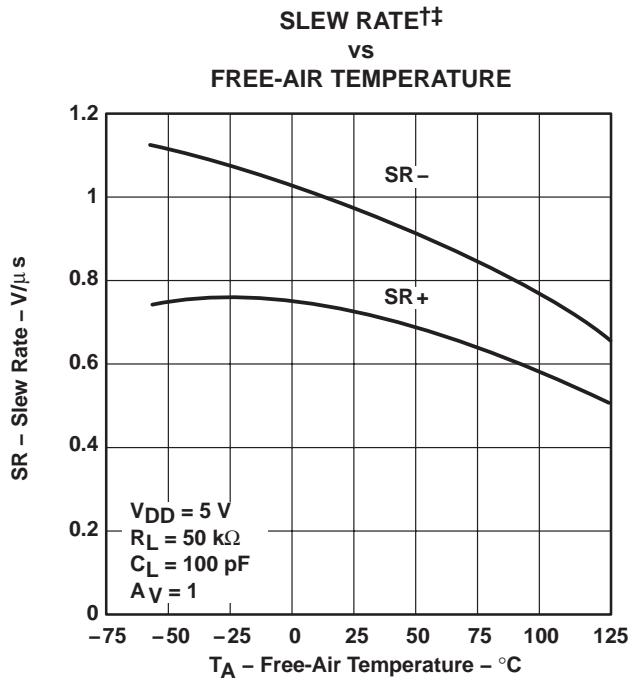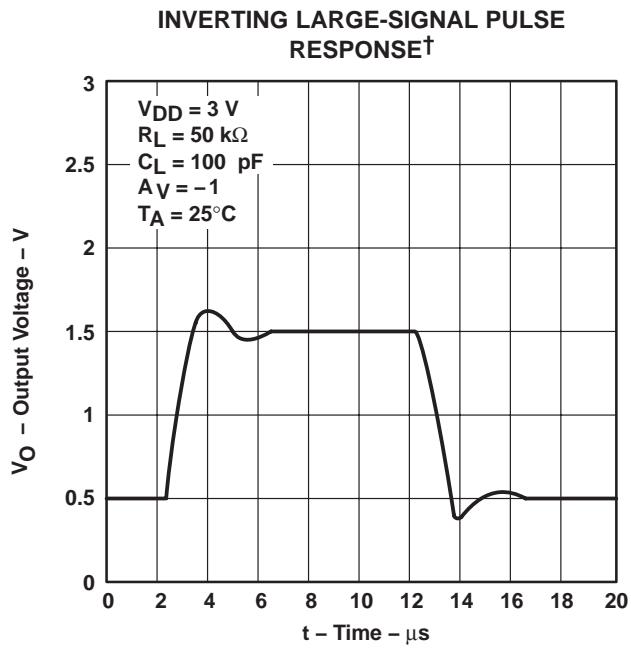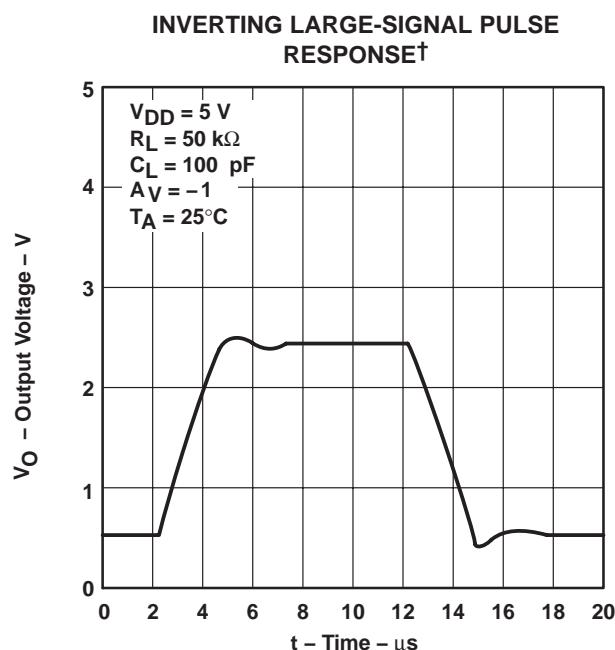
Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

V_{DD} = 3 V
R_L = 50 kΩ
C_L = 100 pF
A_V = – 1
T_A = 25°C

Figure 44

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

V_{DD} = 5 V
R_L = 50 kΩ
C_L = 100 pF
A_V = – 1
T_A = 25°C

Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE†

V_{DD} = 3 V
R_L = 50 kΩ
C_L = 100 pF
A_V = – 1
T_A = 25°C

Figure 46

INVERTING SMALL-SIGNAL PULSE RESPONSE†
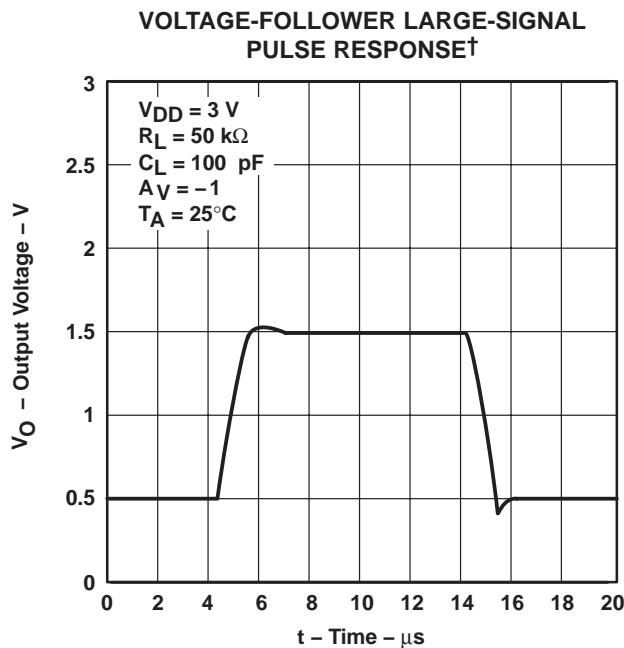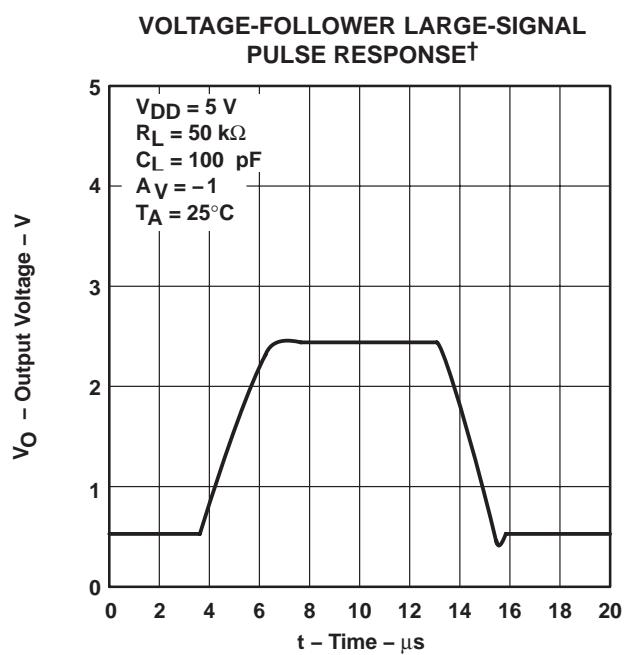
V_{DD} = 5 V
R_L = 50 kΩ
C_L = 100 pF
A_V = – 1
T_A = 25°C
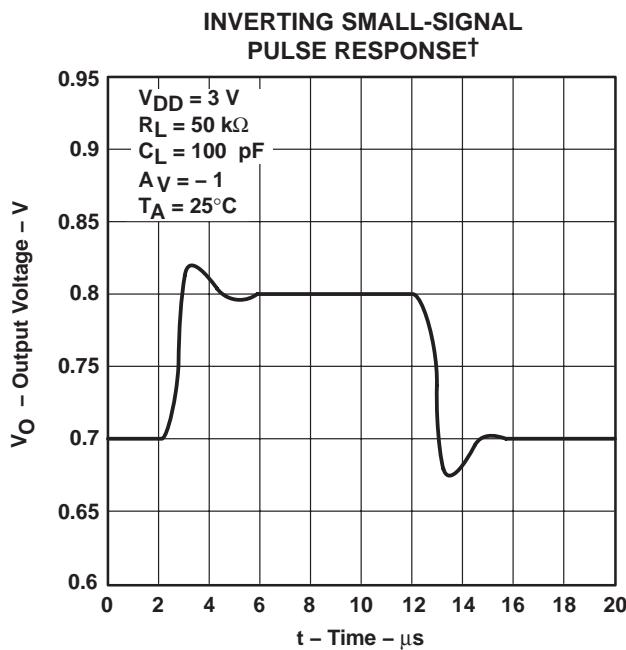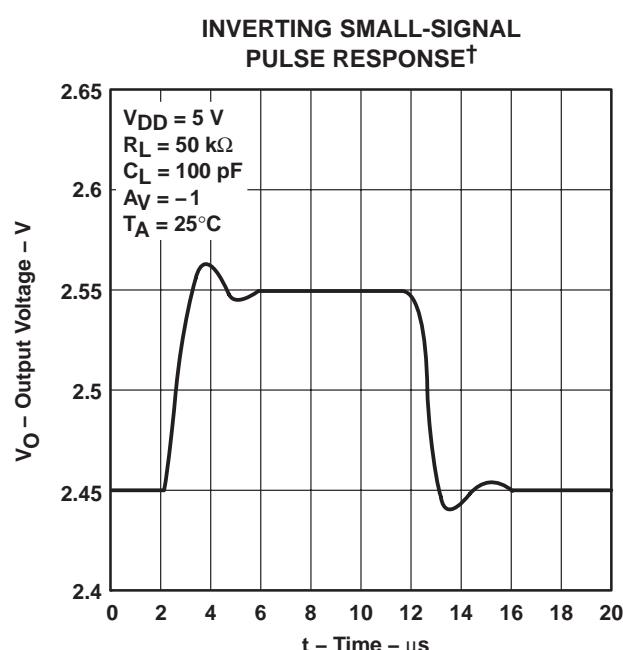
Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE†

V_{DD} = 3 V
R_L = 50 kΩ
C_L = 100 pF
A_V = 1
T_A = 25°C

Figure 48

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE†

V_{DD} = 5 V
R_L = 50 kΩ
C_L = 100 pF
A_V = 1
T_A = 25°C

Figure 49

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

V_{DD} = 3 V
R_S = 20 Ω
T_A = 25°C

Figure 50

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY
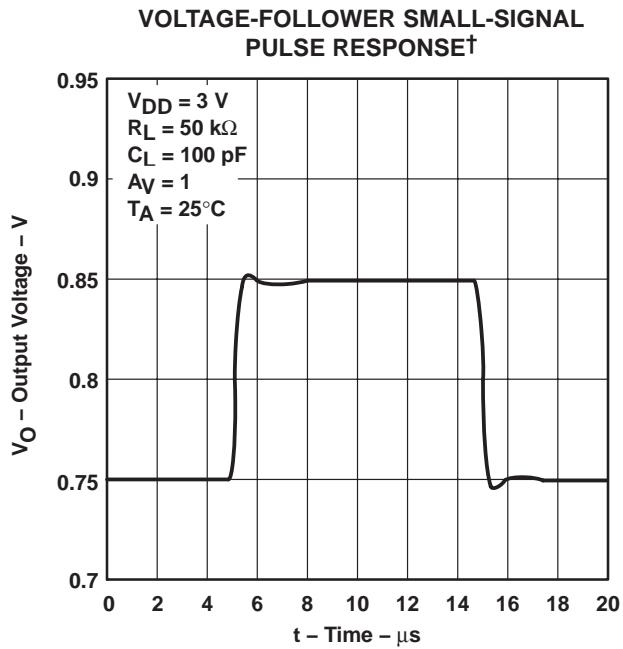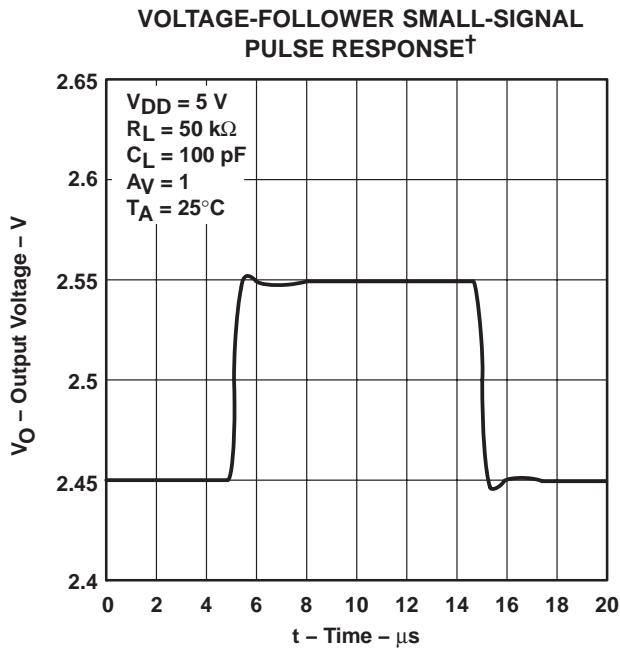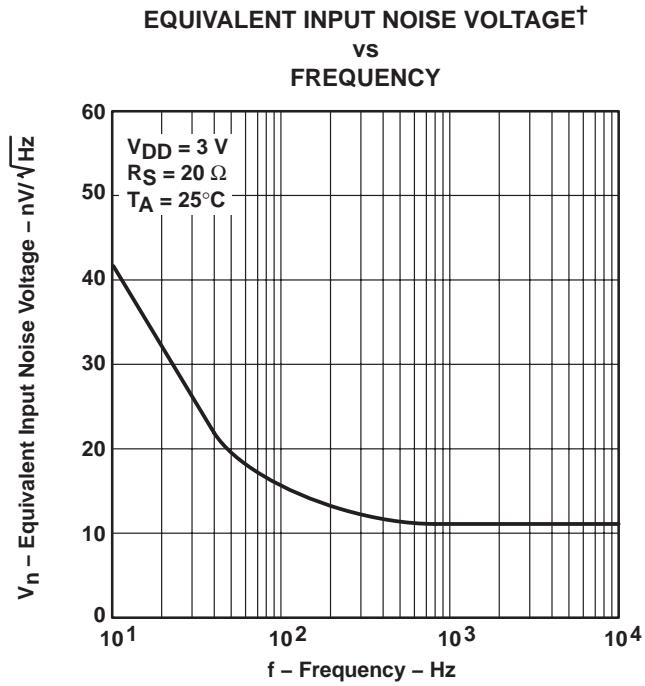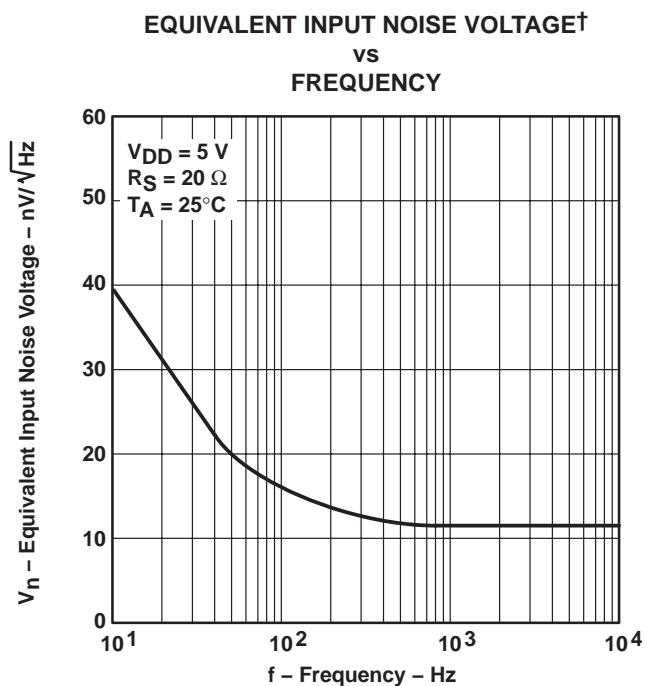
V_{DD} = 5 V
R_S = 20 Ω
T_A = 25°C

Figure 51

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

**INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD†**

Figure 52

**INTEGRATED NOISE VOLTAGE
vs
FREQUENCY**

Figure 53

**TOTAL HARMONIC DISTORTION PLUS NOISE†
vs
FREQUENCY**

Figure 54

**GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE**
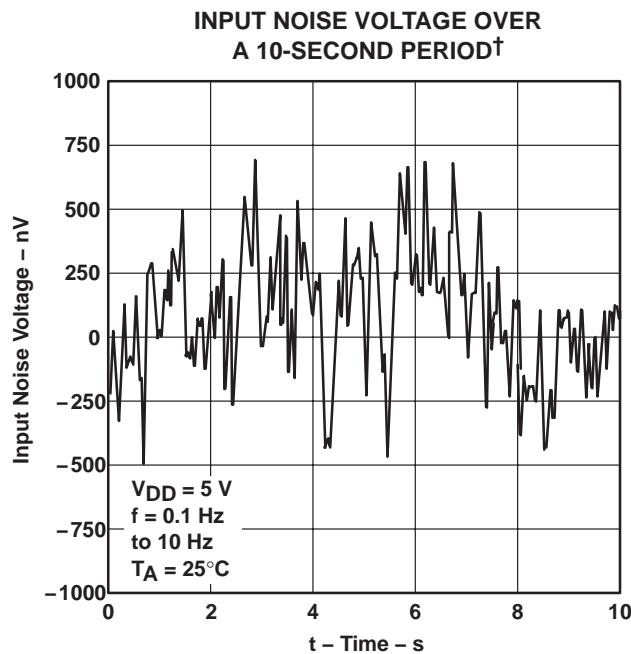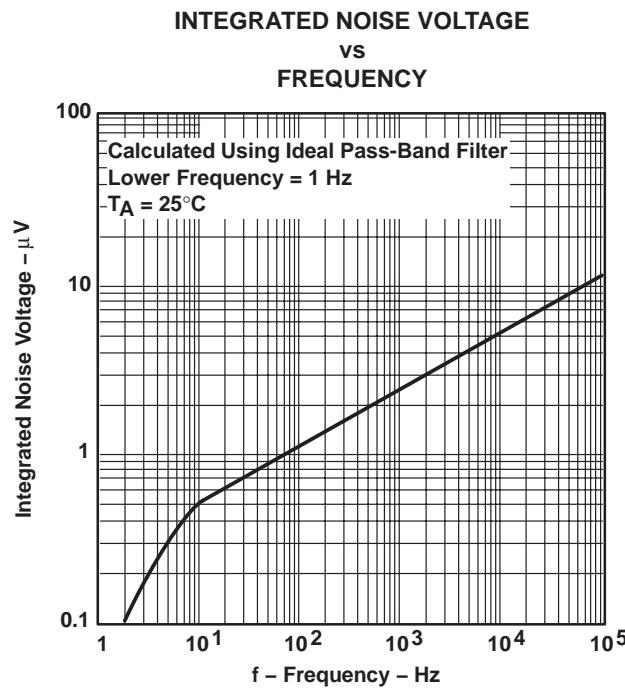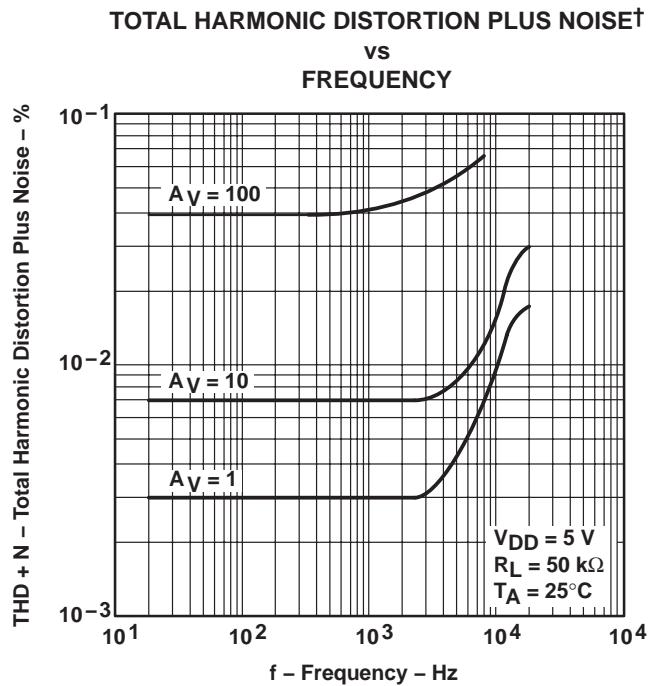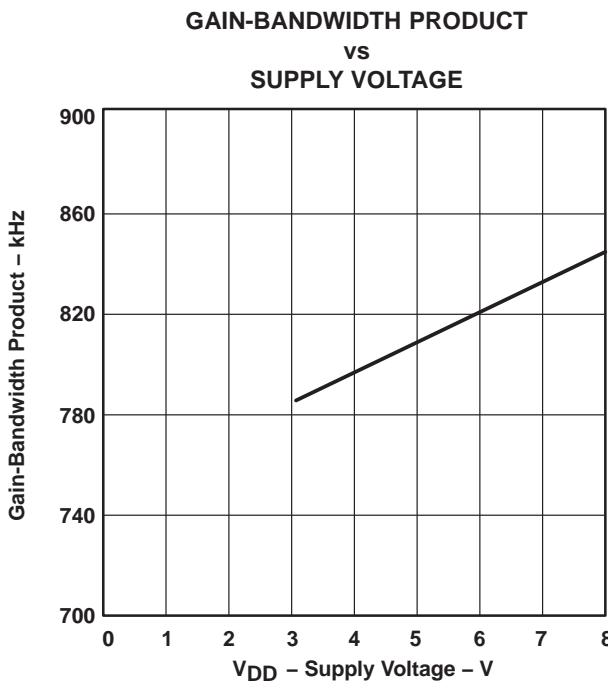
Figure 55

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

V_{DD} = 5 V
f = 10 kHz
C_L = 100 pF

Figure 56

PHASE MARGIN
vs
LOAD CAPACITANCE

T_A = 25°C

R_{null} = 100 Ω
R_{null} = 50 Ω
R_{null} = 20 Ω
R_{null} = 10 Ω
R_{null} = 0

Figure 57

GAIN MARGIN
vs
LOAD CAPACITANCE

R_L = 50 kΩ
A_V = 1
T_A = 25°C

R_{null} = 100 Ω
R_{null} = 50 Ω
R_{null} = 20 Ω
R_{null} = 10 Ω
R_{null} = 0

Figure 58

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

T_A = 25°C
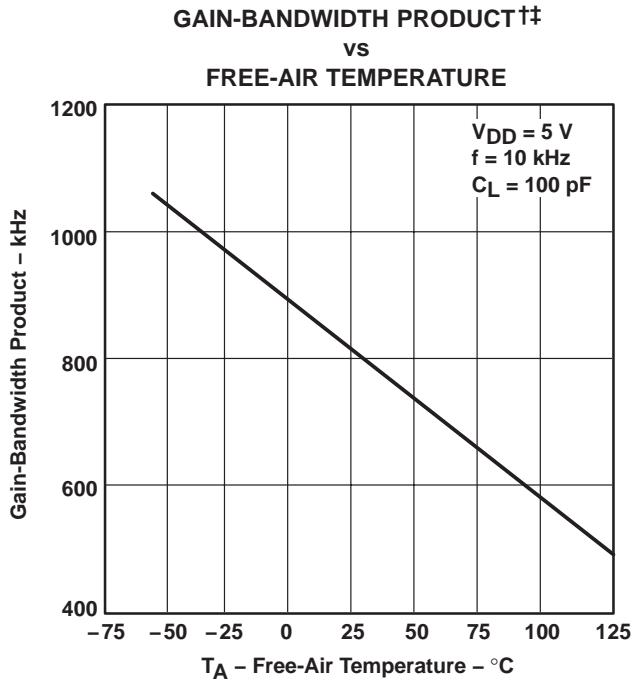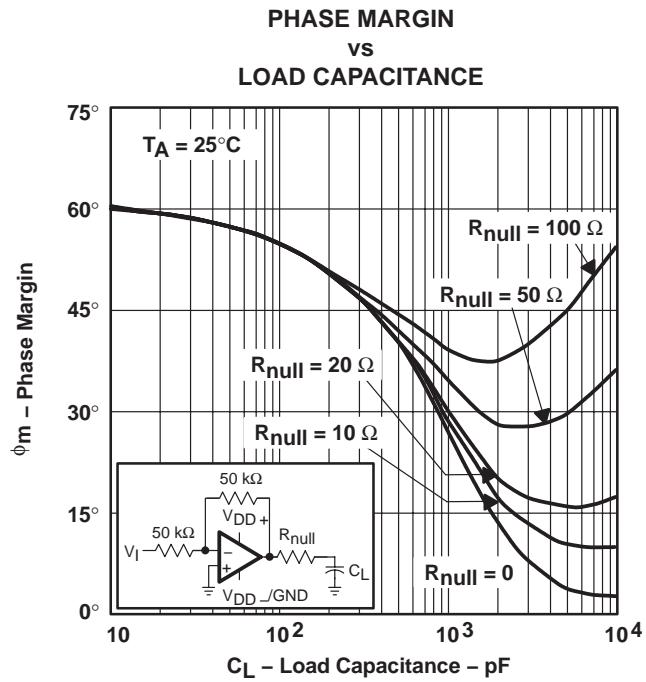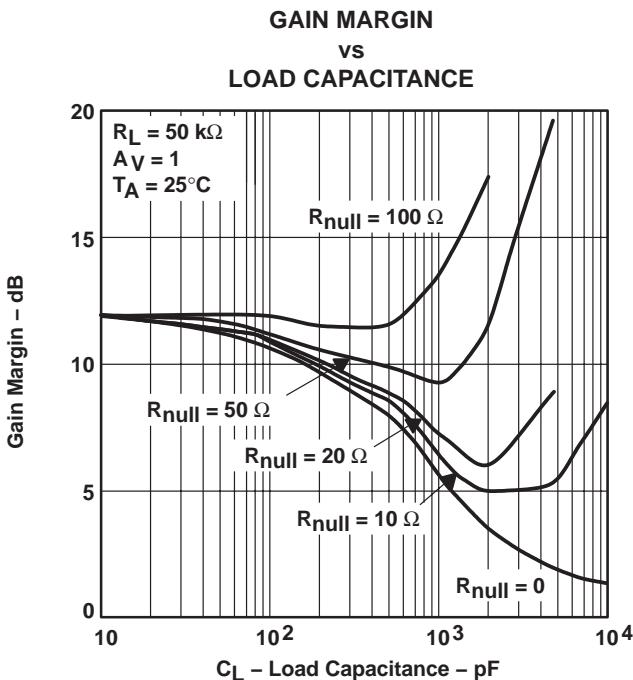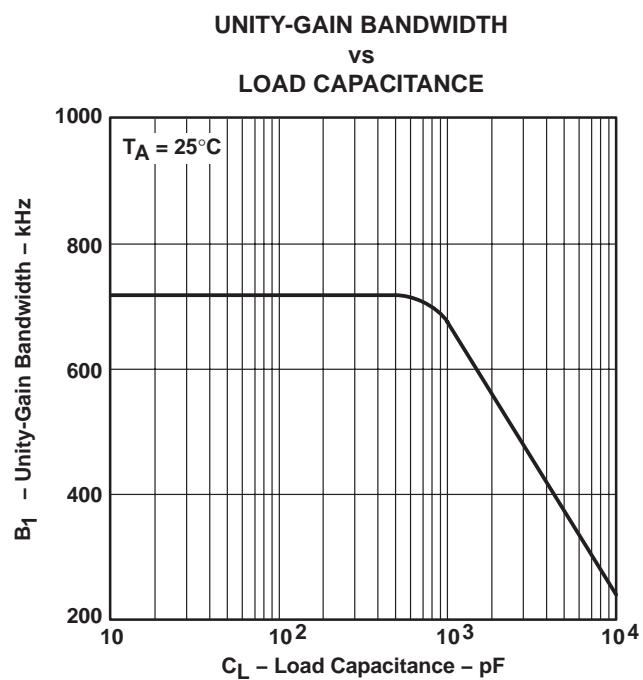
Figure 59

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE
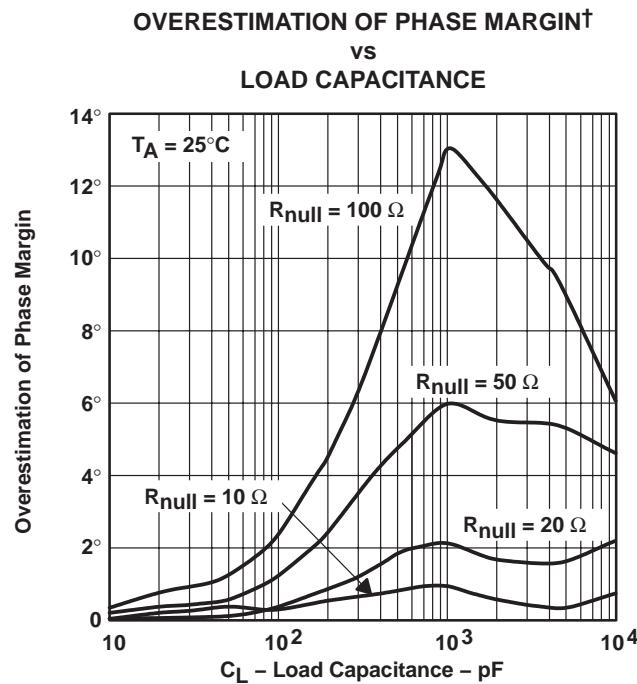
† See application information

Figure 60

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APPLICATION INFORMATION

driving large capacitive loads

The TLV226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 61) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\theta_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \tag{1}$$

Where :

$$\Delta\theta_{m1} = \text{improvement in phase margin}$$
$$\text{UGBW} = \text{unity-gain bandwidth frequency}$$
$$R_{null} = \text{output series resistance}$$
$$C_L = \text{load capacitance}$$

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation 1, UGBW must be approximated from Figure 53.

Using equation 1 alone overestimates the improvement in phase margin as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}} \tag{2}$$

Where :

$$F = \text{factor reducing frequency of pole}$$
$$g_m = \text{small-signal output transconductance (typically } 4.83 \times 10^{-3} \text{ mhos)}$$
$$R_{null} = \text{output series resistance}$$

For the TLV226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 70 MHz, at C_L = 1000 pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation 1 to better approximate the improvement in phase margin.

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APPLICATION INFORMATION

driving large capacitive loads (continued)

$$\Delta\theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \tag{3}$$

Where :

$\Delta\theta_{m2}$ = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation (2)

P_2 = unadjusted pole (70 MHz @ 10 pF, 7 MHz @ 100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.
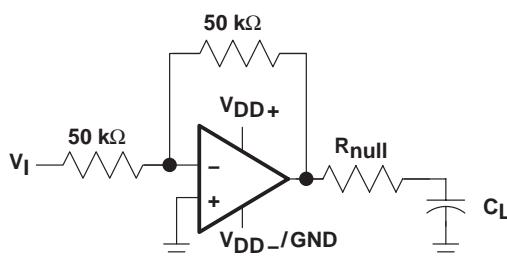
Figure 61. Series-Resistance Circuit

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 62 are generated using the TLV226x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).


```
.SUBCKT TLV226x 1 2 3 4 5
C1      11    12    5.5E−12
C2       6     7    20.00E−12
DC       5    53    DX
DE      54     5    DX
DLP     90    91    DX
DLN     92    90    DX
DP       4     3    DX
EGND    99     0    POLY (2) (3,0) (4,0) 0 .5 .5
FB       7    99    POLY (5) VB VC VE VLP
+ VLN 0 8.84E6 −10E6 10E6 10E6 −10E6
GA       6     0    11    12 62.83E−6
GCM      0     6    10    99 12.34E−9
ISS      3    10    DC 11.05E−6
HLIM    90     0    VLIM 1K
J1      11     2    10 JX
J2      12     1    10 JX
R2       6     9    100.0E3
```

```
RD1     60    11    15.92E3
RD2     60    12    15.92E3
R01      8     5    135
R02      7    99    135
RP       3     4    15.87E3
RSS     10    99    18.18E6
VAD     60     4    −.5
VB       9     0    DC 0
VC       3    53    DC .615
VE      54     4    DC .615
VLIM     7     8    DC 0
VLP     91     0    DC 1
VLN      0    92    DC 5.1
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=500.0E−15 BETA=325E−6
+ VTO=−.08)
.ENDS
```

Figure 62. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9550401QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550401QPA TLV2262M	Samples
5962-9550403QHA	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550403QHA TLV2262AM	Samples
5962-9550403QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550403QPA TLV2262AM	Samples
5962-9550404QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9550404QC A TLV2264AMJB	Samples
5962-9550404QDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9550404QD A TLV2264AMWB	Samples
TLV2262AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262A	Samples
TLV2262AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262A	Samples
TLV2262AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2262AI	Samples
TLV2262AIPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY262A	Samples
TLV2262AIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY262A	Samples
TLV2262AMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550403QPA TLV2262AM	Samples
TLV2262AMUB	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550403QHA TLV2262AM	Samples
TLV2262ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262I	Samples
TLV2262IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262I	Samples
TLV2262IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262I	Samples
TLV2262IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2262IP	Samples
TLV2262IPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2262	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2262IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2262	Samples
TLV2262MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550401QPA TLV2262M	Samples
TLV2264AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2264AI	Samples
TLV2264AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2264AI	Samples
TLV2264AIDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2264AI	Samples
TLV2264AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2264AIN	Samples
TLV2264AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264AI	Samples
TLV2264AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264AI	Samples
TLV2264AMJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9550404QCA TLV2264AMJB	Samples
TLV2264AMWB	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9550404QDA TLV2264AMWB	Samples
TLV2264AQD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264A	Samples
TLV2264ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264I	Samples
TLV2264IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264I	Samples
TLV2264IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2264IN	Samples
TLV2264IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264I	Samples
TLV2264QD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2262, TLV2262A, TLV2262AM, TLV2262M, TLV2264A, TLV2264AM :

● Catalog : TLV2262A, TLV2262, TLV2264A

● Automotive : TLV2262A-Q1, TLV2262A-Q1, TLV2264A-Q1, TLV2264A-Q1

● Military : TLV2262M, TLV2262AM, TLV2264AM

NOTE: Qualified Version Definitions:

    ● Catalog - TI's standard catalog product

    ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS
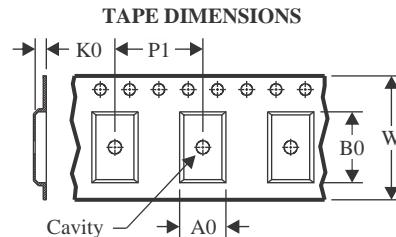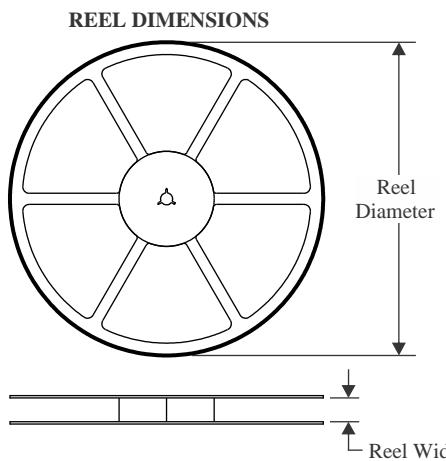
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
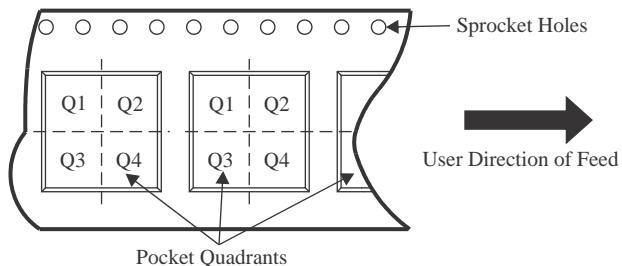
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2262AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2262AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2262IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2262IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2264AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2264AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2264IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2264IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
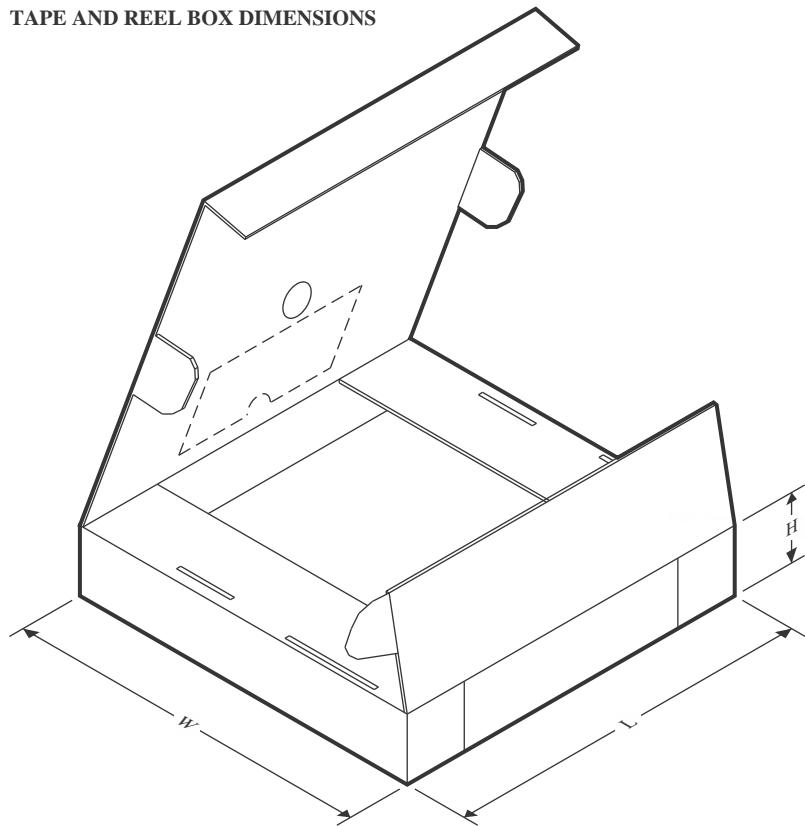
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2262AIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2262AIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2262IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2262IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2264AIDR	SOIC	D	14	2500	340.5	336.1	32.0
TLV2264AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2264IDR	SOIC	D	14	2500	340.5	336.1	32.0
TLV2264IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TUBE
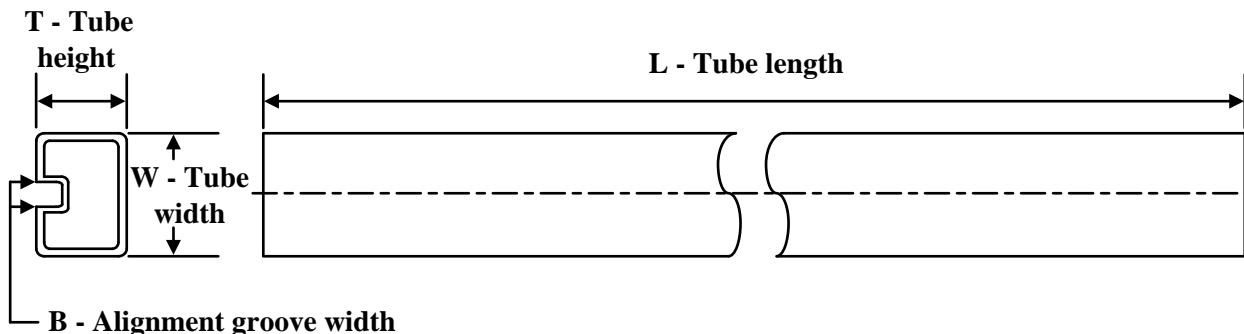
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9550403QHA	U	CFP	10	1	506.98	26.16	6220	NA
5962-9550404QDA	W	CFP	14	1	506.98	26.16	6220	NA
TLV2262AID	D	SOIC	8	75	507	8	3940	4.32
TLV2262AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2262AIPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TLV2262AMUB	U	CFP	10	1	506.98	26.16	6220	NA
TLV2262ID	D	SOIC	8	75	507	8	3940	4.32
TLV2262IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2262IPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TLV2264AID	D	SOIC	14	50	507	8	3940	4.32
TLV2264AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2264AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2264AMWB	W	CFP	14	1	506.98	26.16	6220	NA
TLV2264AQD	D	SOIC	14	50	505.46	6.76	3810	4
TLV2264ID	D	SOIC	14	50	507	8	3940	4.32
TLV2264IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2264QD	D	SOIC	14	50	505.46	6.76	3810	4

W (R–GDFP–F14) CERAMIC DUAL FLATPACK
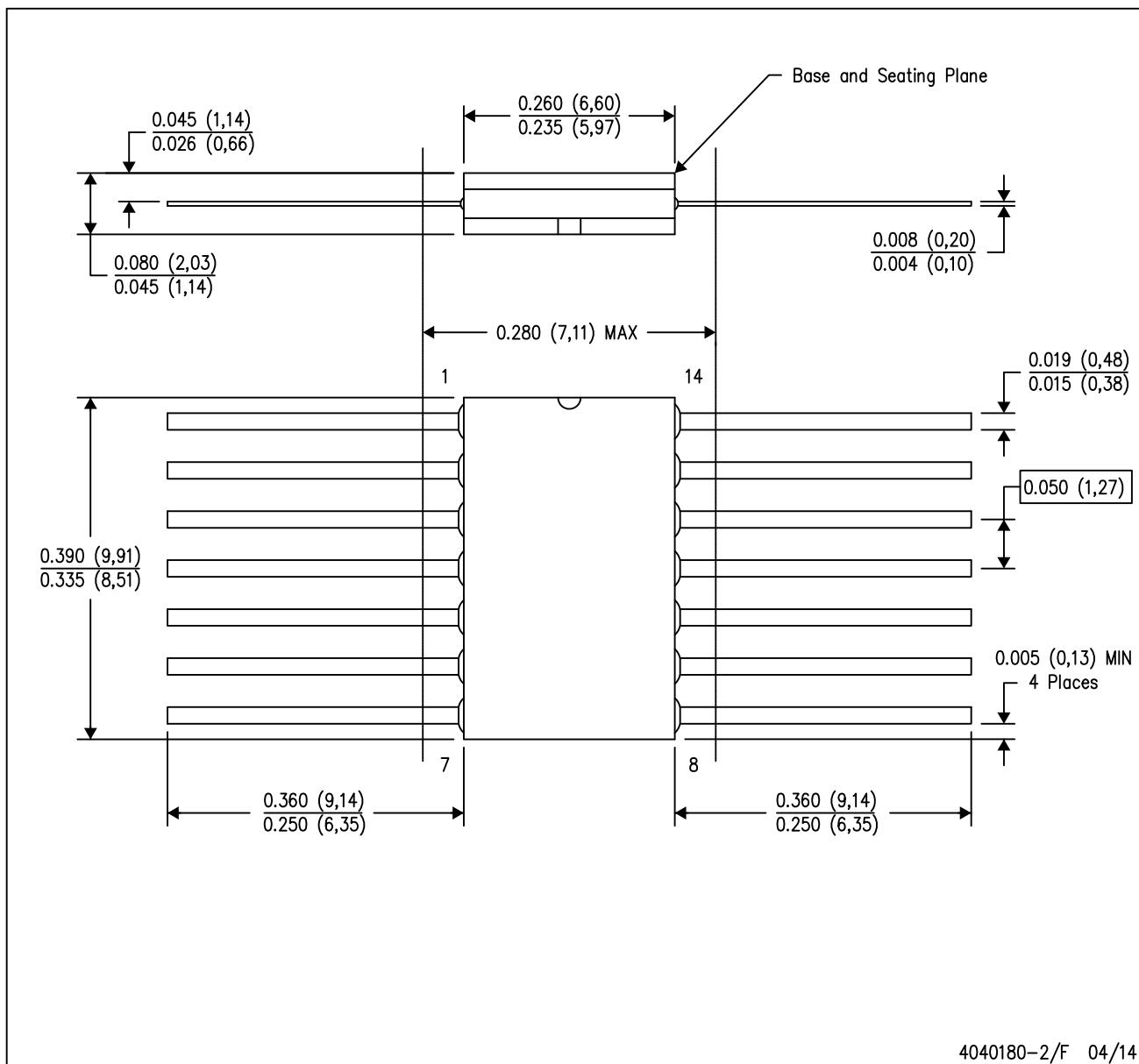
0.260 (6,60) / 0.235 (5,97)

Base and Seating Plane

0.045 (1,14) / 0.026 (0,66)

0.080 (2,03) / 0.045 (1,14)

0.008 (0,20) / 0.004 (0,10)

0.280 (7,11) MAX

1   14

0.019 (0,48) / 0.015 (0,38)

0.050 (1,27)

0.390 (9,91) / 0.335 (8,51)

0.005 (0,13) MIN
4 Places

7   8

0.360 (9,14) / 0.250 (6,35)

0.360 (9,14) / 0.250 (6,35)

4040180–2/F 04/14

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14
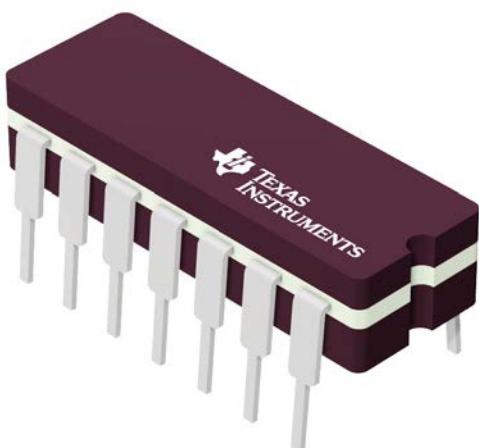
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

PIN 1 ID
(OPTIONAL)

A

1

14

12X .100
[2.54]

.754-.785
[19.15-19.94]

7

8

B

.245-.283
[6.22-7.19]

4X .005 MIN
[0.13]

.015-.060   TYP
[0.38-1.52]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕ .010 [0.25] C A B

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015   GAGE PLANE
[0.38]

0°-15°
TYP

14X .008-.014
[0.2-0.36]
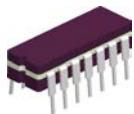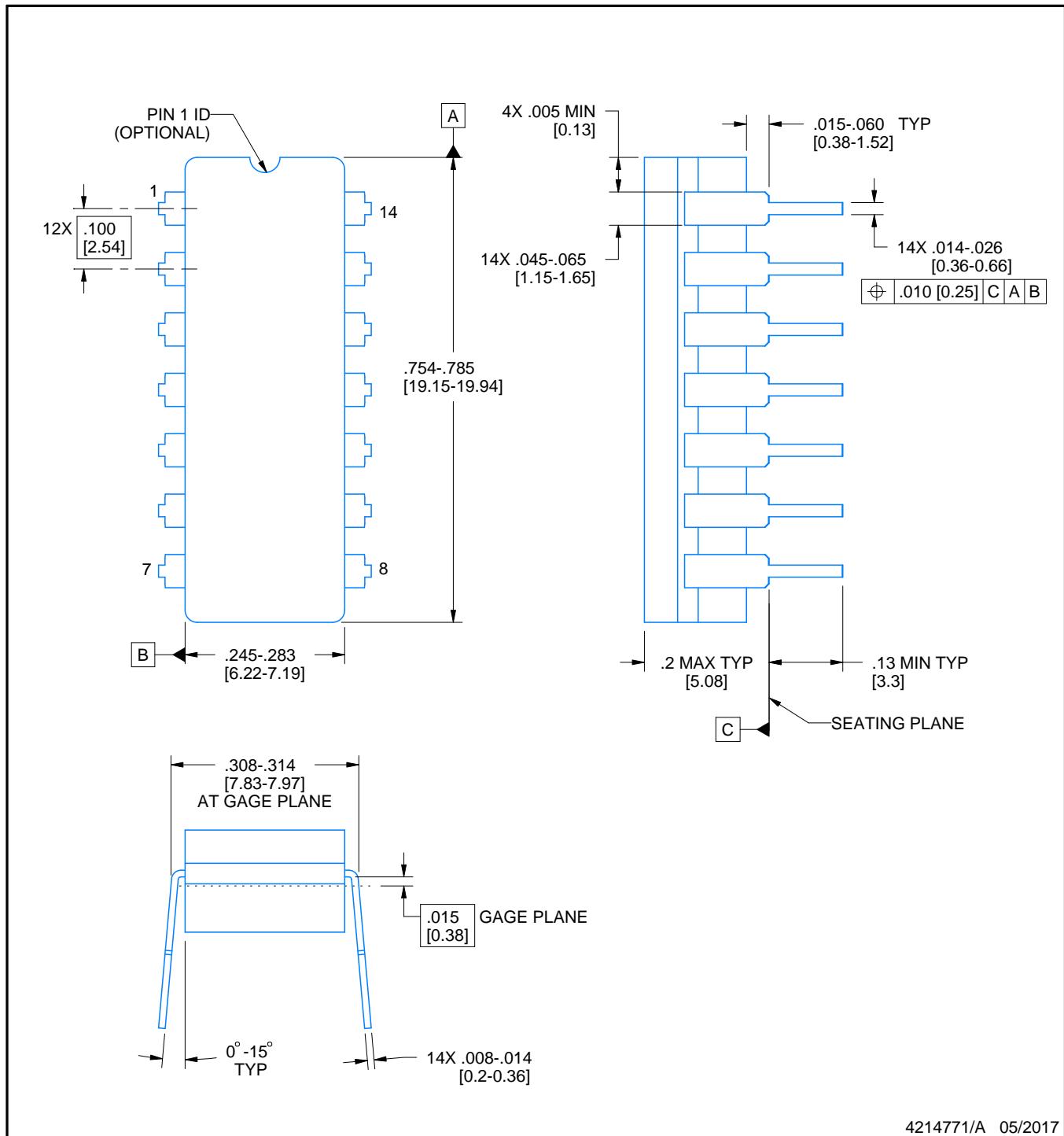
4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

SEE DETAIL A

SEE DETAIL B

(.300) TYP
[7.62]

1

14

12X (.100)
[2.54]

SYMM
℄

14X (∅ .039)
[1]

7

8

SYMM
℄
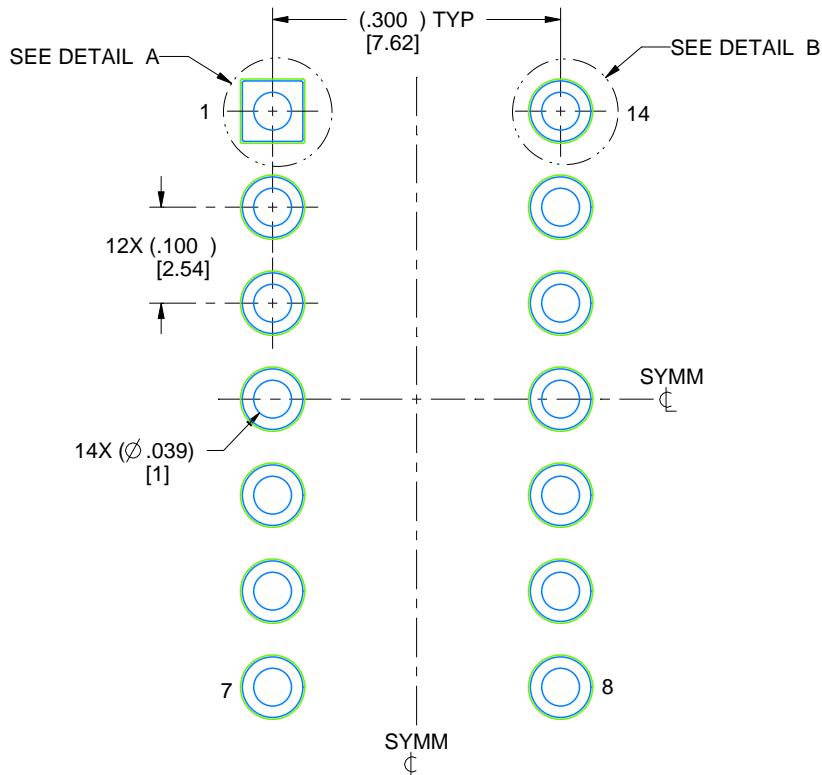
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002) TYP
[0.05]

METAL

(∅ .063)
[1.6]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

DETAIL A
SCALE: 15X

DETAIL B
13X, SCALE: 15X
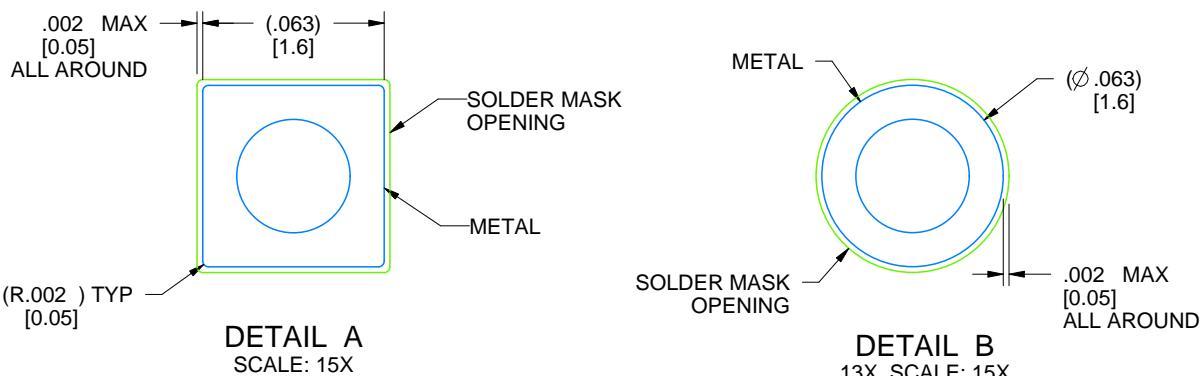
4214771/A   05/2017

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE
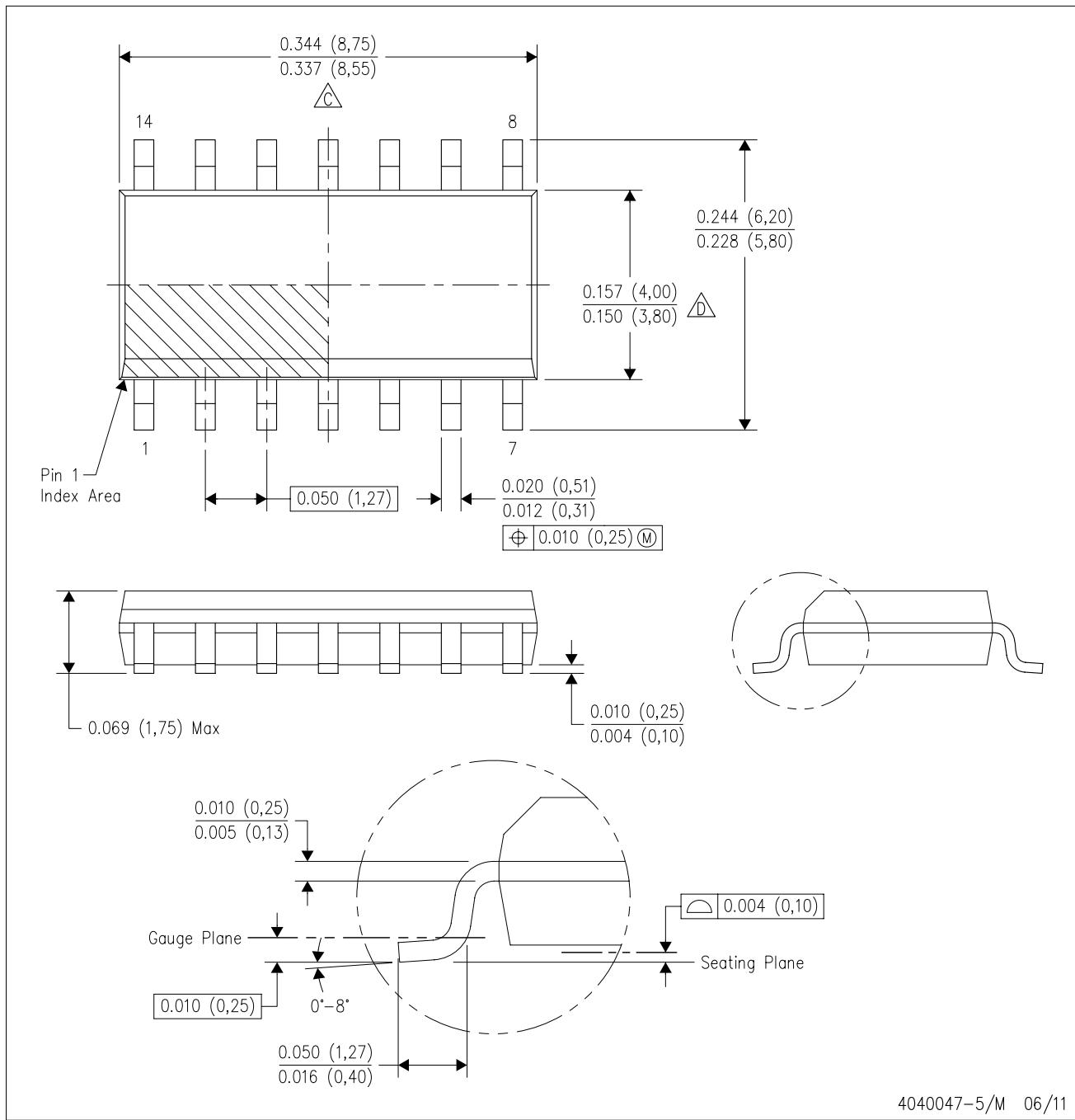
0.344 (8,75)
0.337 (8,55)

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
      ⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
      ⚠D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E. Reference JEDEC MS−012 variation AB.

PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14   8

D   4,50
4,30

6,60
6,20

1   7

5,10
4,90

C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

◠ 0,10
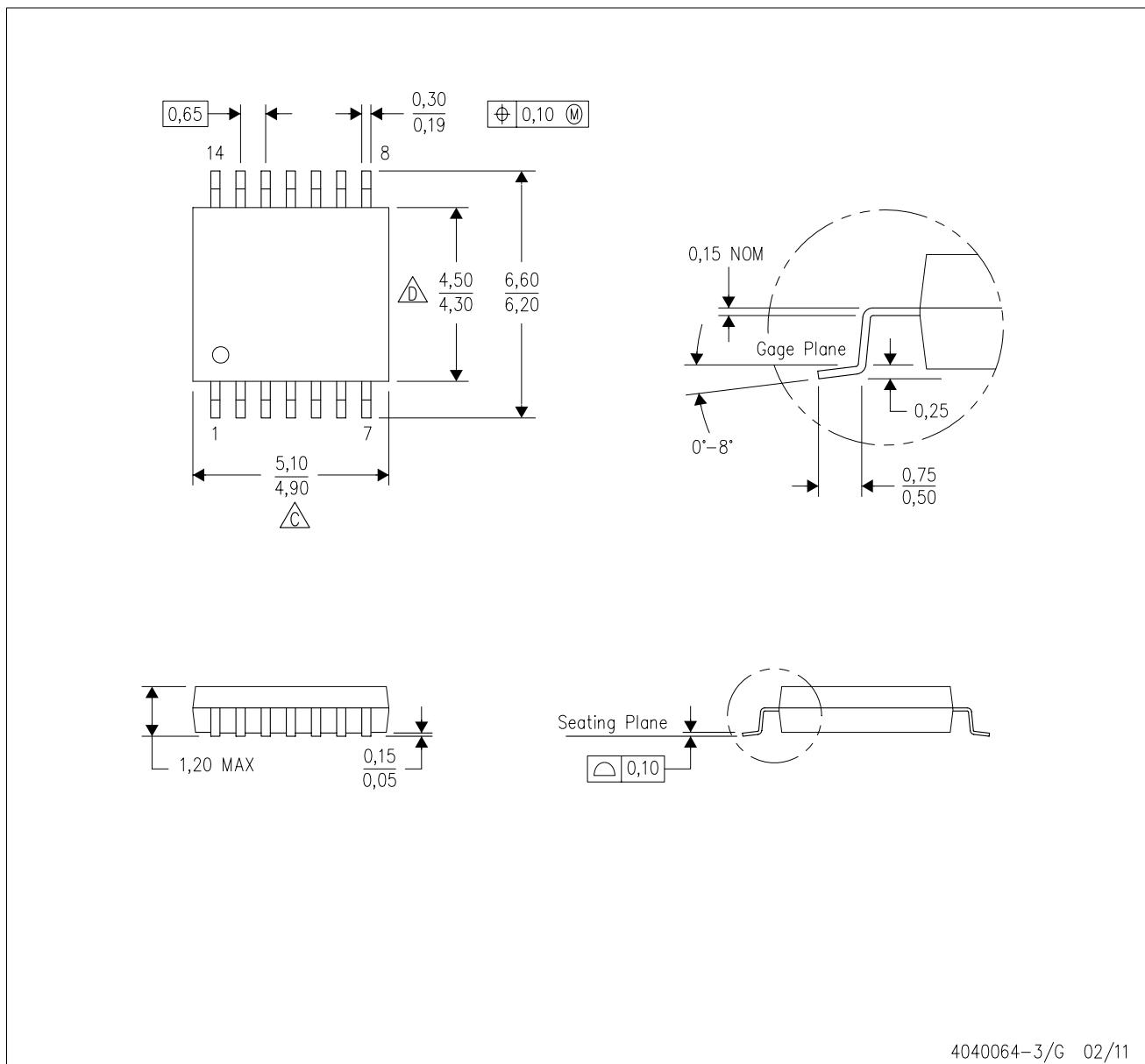
4040064−3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153

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Instruments
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.228-.244 TYP
[5.80-6.19]

PIN 1 ID AREA

A

.189-.197
[4.81-5.00]
NOTE 3

1

4

8

6X .050
[1.27]

2X
.150
[3.81]

5

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25] Ⓜ C A B

B

.150-.157
[3.81-3.98]
NOTE 4

C

SEATING PLANE

⌒ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010 TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C 02/2019
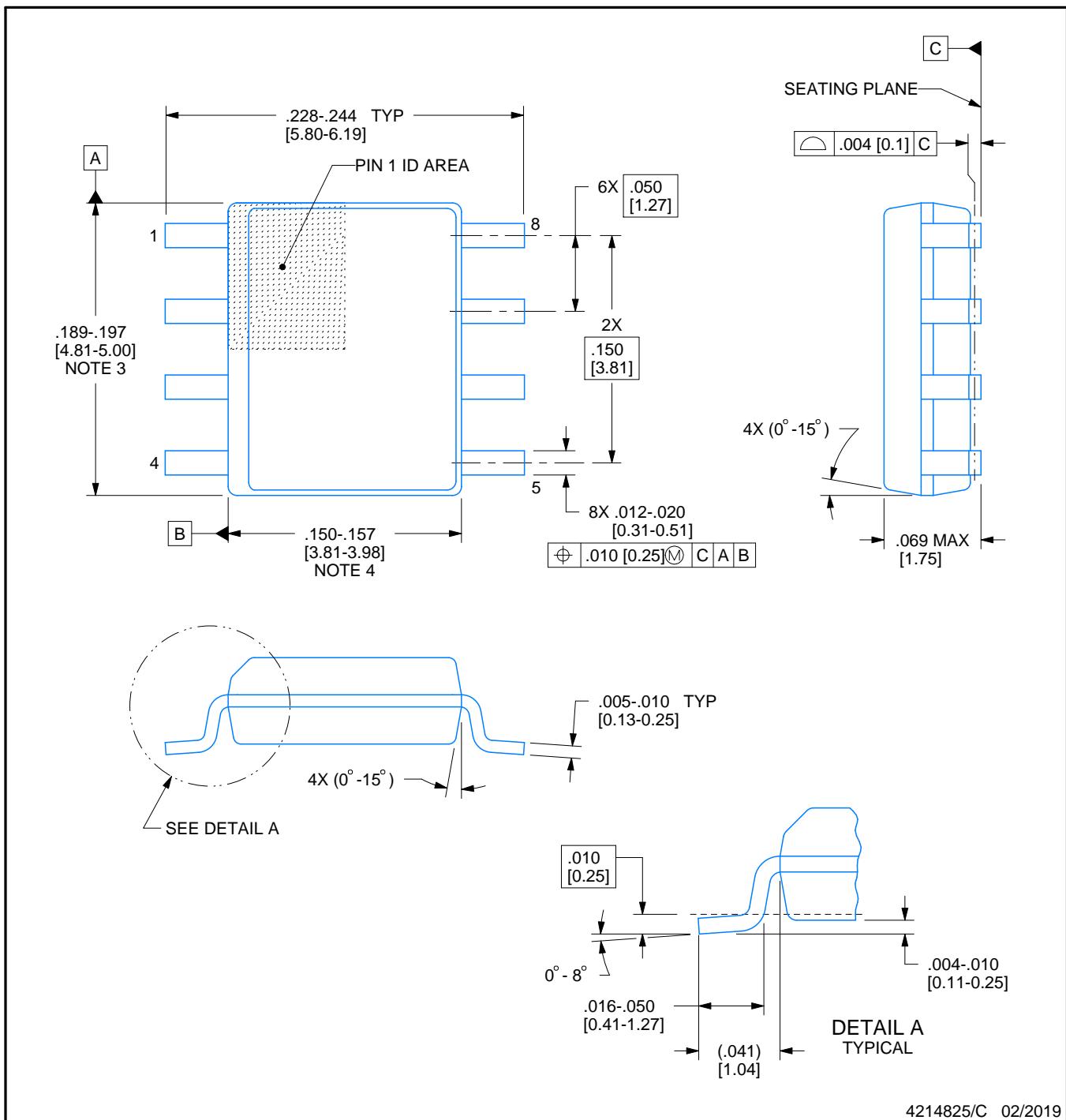
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

1

8X (.024)
[0.6]

6X (.050)
[1.27]

4

SYMM

SEE
DETAILS

8

SYMM

(R.002) TYP
[0.05]

5

(.213)
[5.4]
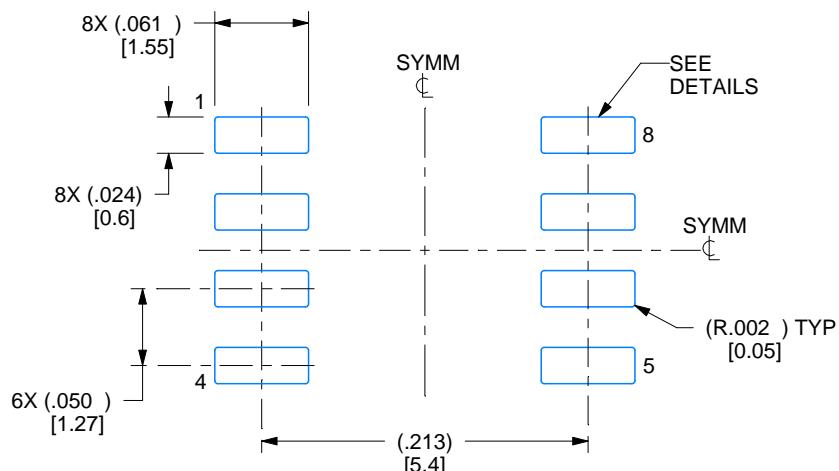
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

.0028 MIN
[0.07]
ALL AROUND

SOLDER MASK
DEFINED
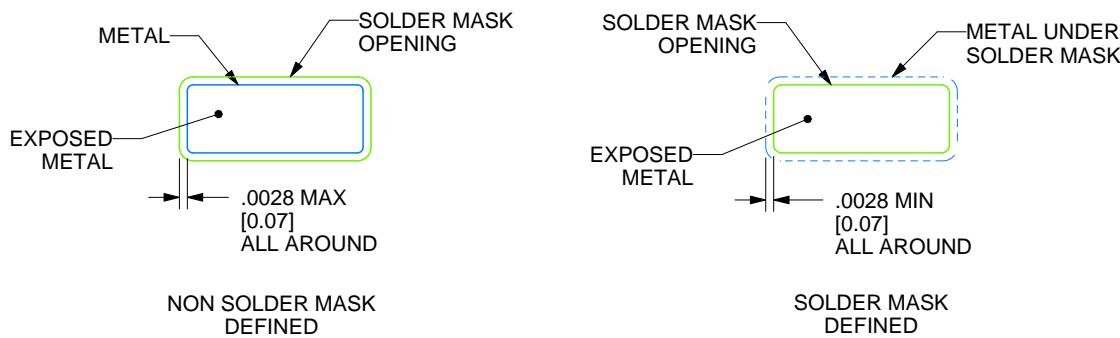
SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061) [1.55]
8X (.024) [0.6]
6X (.050) [1.27]
SYMM
SYMM
(R.002) TYP [0.05]
(.213) [5.4]
1
4
5
8
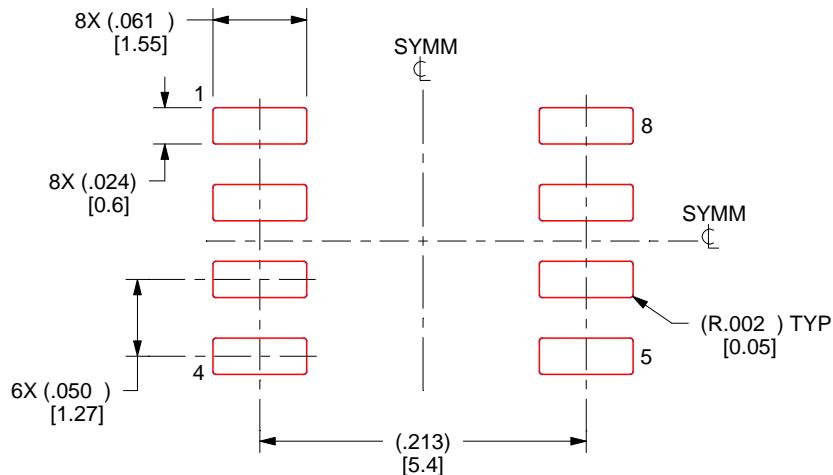
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)   **CERAMIC DUAL-IN-LINE**
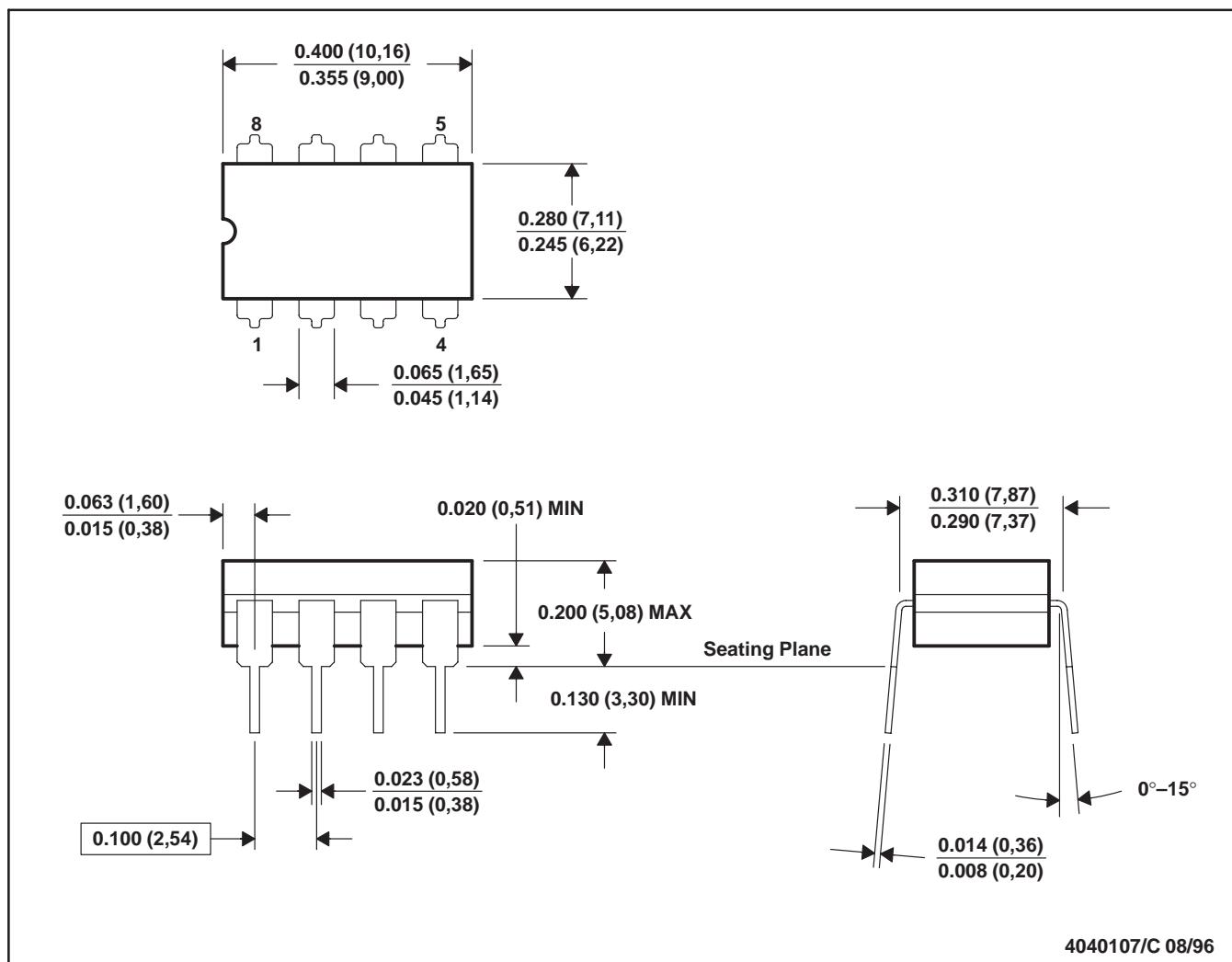
0.400 (10,16)
0.355 (9,00)

8   5

0.280 (7,11)
0.245 (6,22)

1   4

0.065 (1,65)
0.045 (1,14)

0.063 (1,60)
0.015 (0,38)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.023 (0,58)
0.015 (0,38)

0.100 (2,54)

0.310 (7,87)
0.290 (7,37)

0°–15°

0.014 (0,36)
0.008 (0,20)

4040107/C 08/96

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification.
        E. Falls within MIL STD 1835 GDIP1-T8

P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE
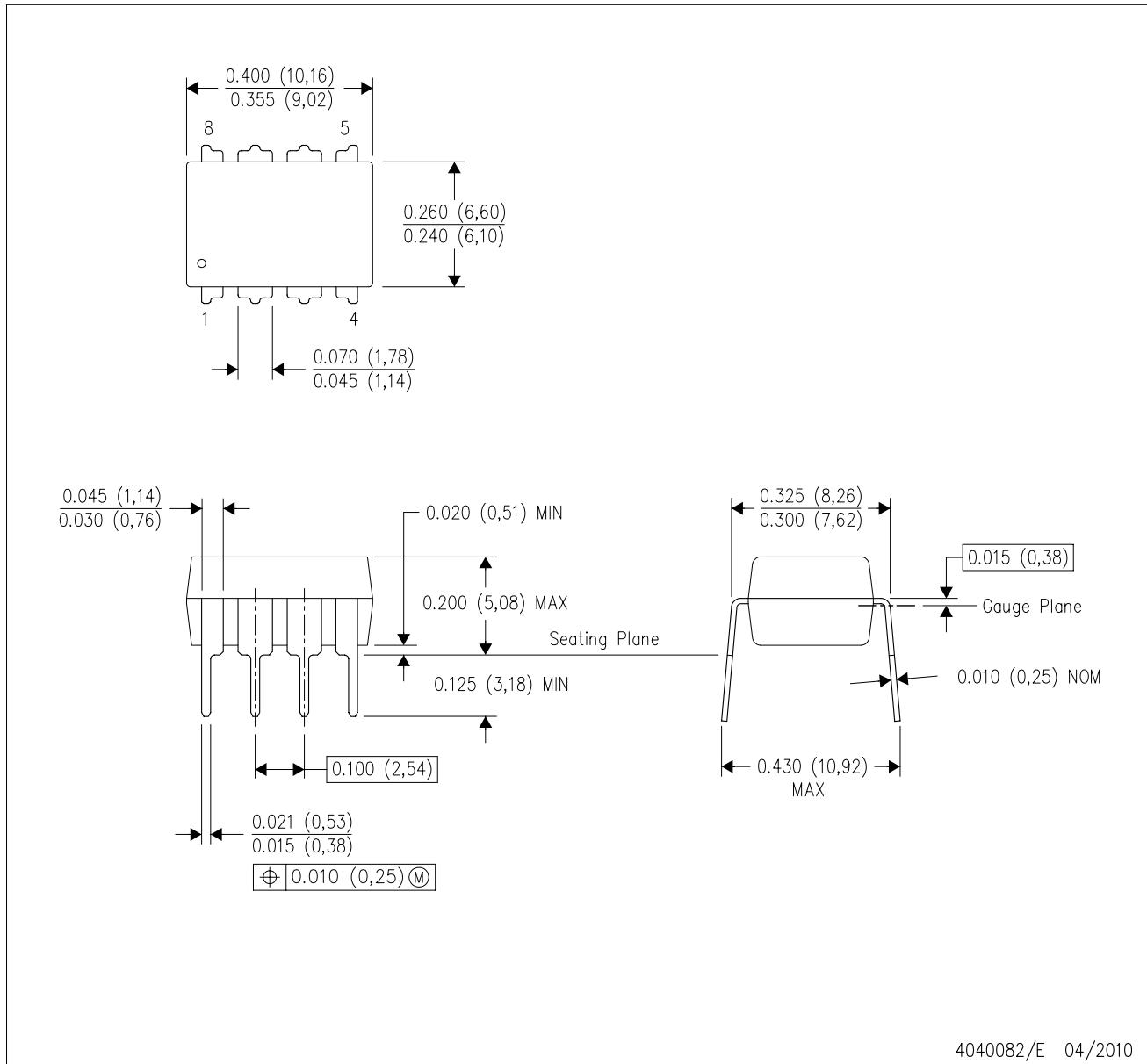
4040082/E 04/2010

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001 variation BA.

TEXAS
INSTRUMENTS
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N (R-PDIP-T**)
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE
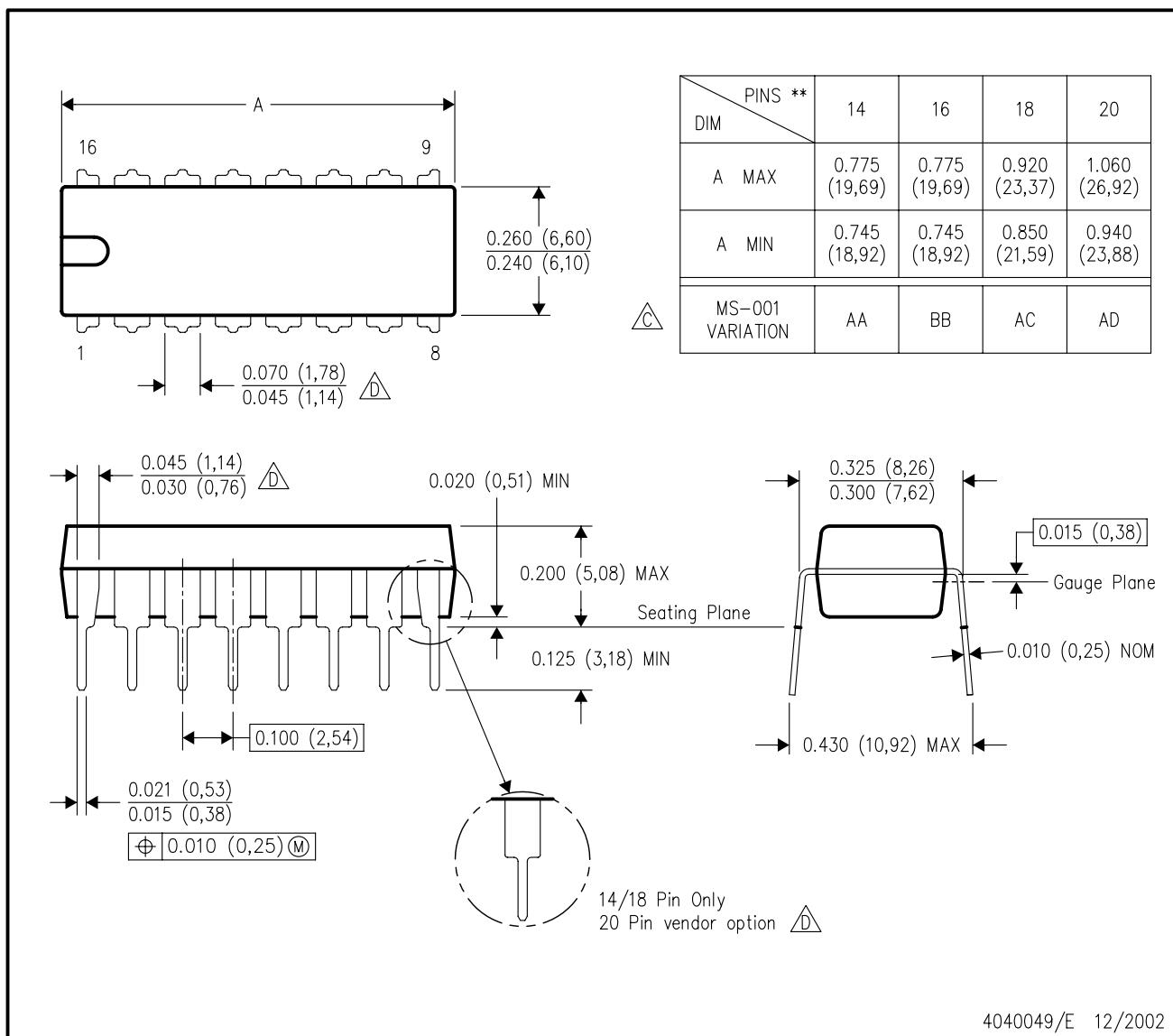
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
   D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PIN 1 ID
AREA

6.6
6.2 TYP

A

1

3.1
2.9
NOTE 3

4

B

4.5
4.3
NOTE 4

8

6X 0.65

2X

1.95

5

8X 0.30
0.19

⊕ 0.1 Ⓜ C AⓈ BⓈ

C

SEATING PLANE

◠ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4221848/A   02/2015
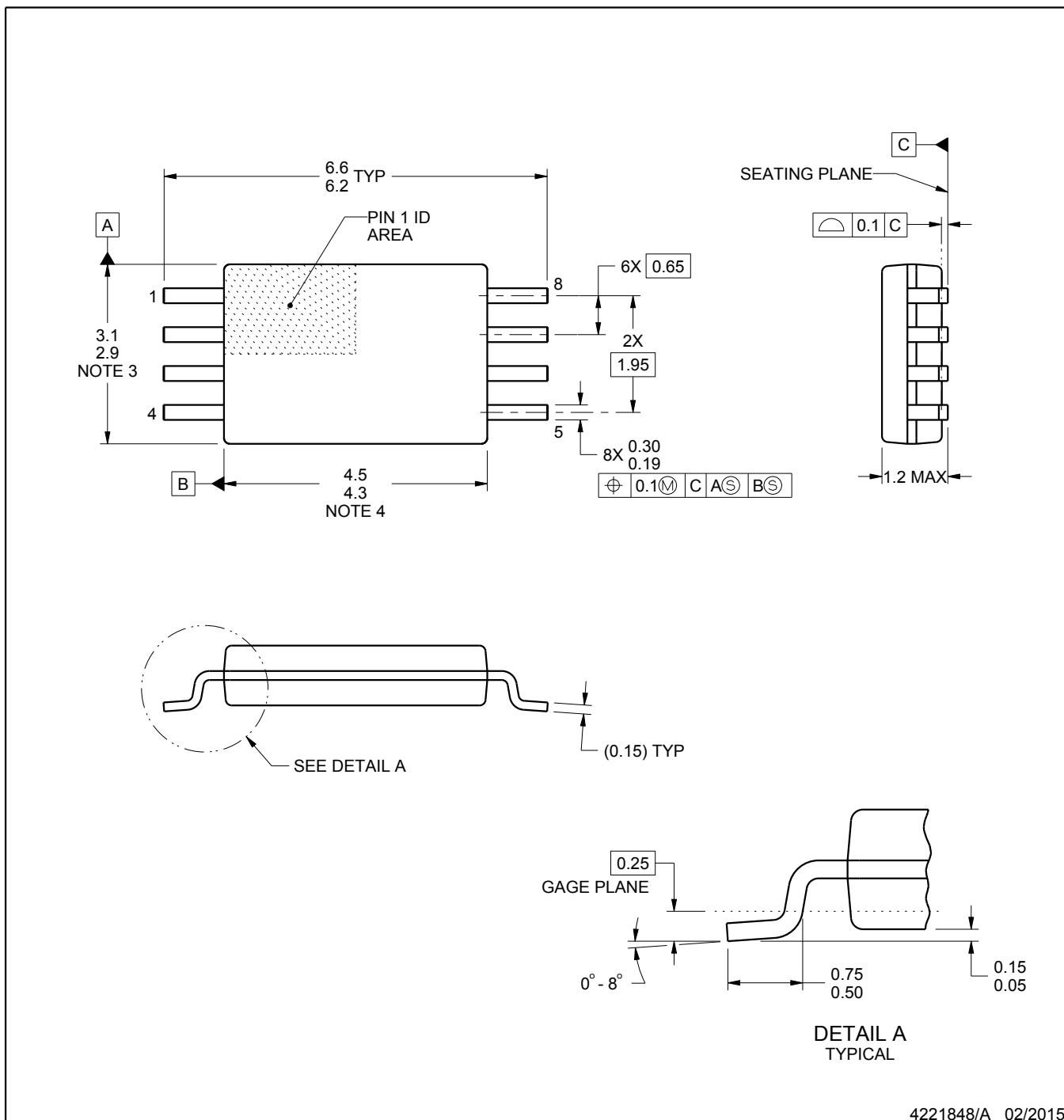
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

8X (0.45)

8X (1.5)

SYMM

(R0.05)
TYP

1

8

SYMM

6X (0.65)

4

5

(5.8)
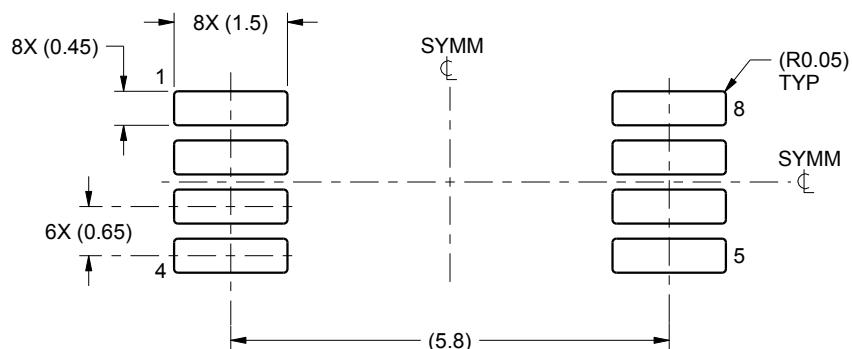
LAND PATTERN EXAMPLE
SCALE:10X
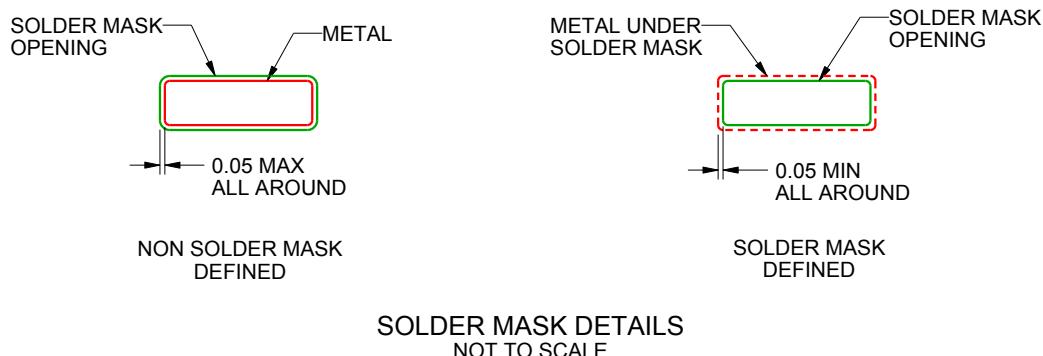
SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A   02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A   02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

TEXAS
INSTRUMENTS
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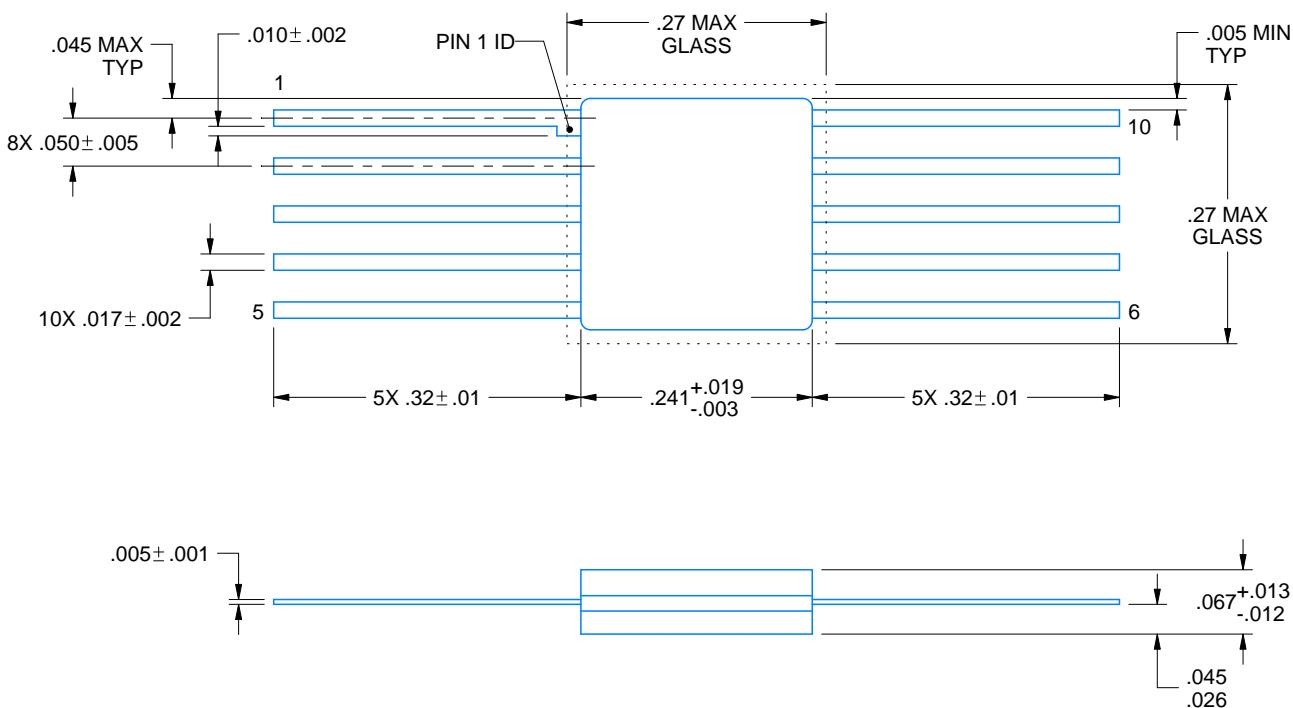
4225582/A   01/2020

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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