DEMO MANUAL DC126
High Speed Line Receiver Demo Board

LTC1520
50Mbps Precision Quad Line Receiver

DESCRIPTION

Demonstration Circuit DC126 highlights some of the key characteristics of the LTC®1520 line receiver. The LTC1520 is a high speed, precision timing, differential line receiver that can operate at data rates as high as 50Mbps. A unique architecture provides very stable propagation delays and low skew (both same-channel and channel-to-channel) over a wide input common mode range. The device operates from a single 5V supply and is designed for use in network backplanes, high speed computer buses and other applications that require precision delay between channels.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

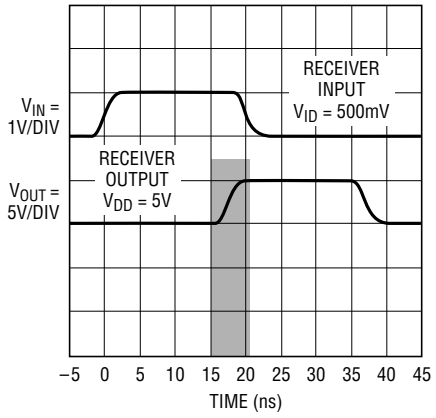
PERFORMANCE SUMMARY

Operating temperature range 0°C to 70°C, V_{DD} = 5V, unless otherwise specified.

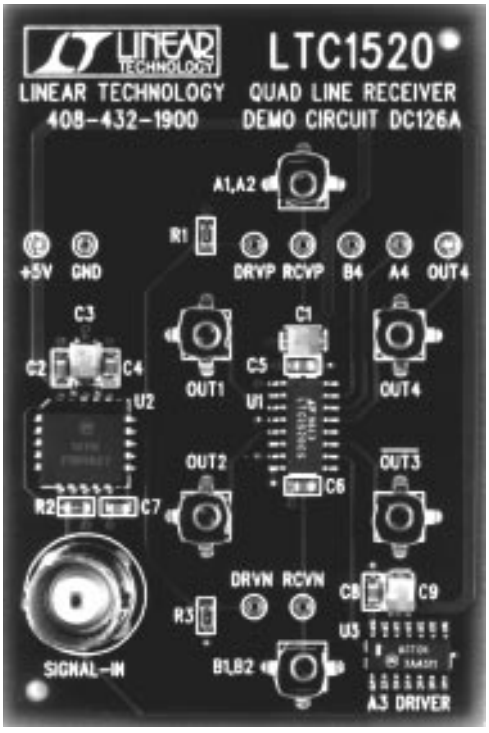
PARAMETER	MIN	TYP	MAX	UNITS
Input Common Mode Range	–0.2		V_{DD} + 0.2	V
Input-Output Propagation Delay	15	18	21	ns
$\lvert t_{LH} - t_{HL} \rvert$ Skew		0.5		ns
Channel-to-Channel Skew		0.4		ns

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

Propagation Delay Guaranteed to Fall Within Shaded Area (±3ns)



LTC1520 TA02



DM126 BD PHOTO

PACKAGE A ND SCHEMATIC DIAGRAMS

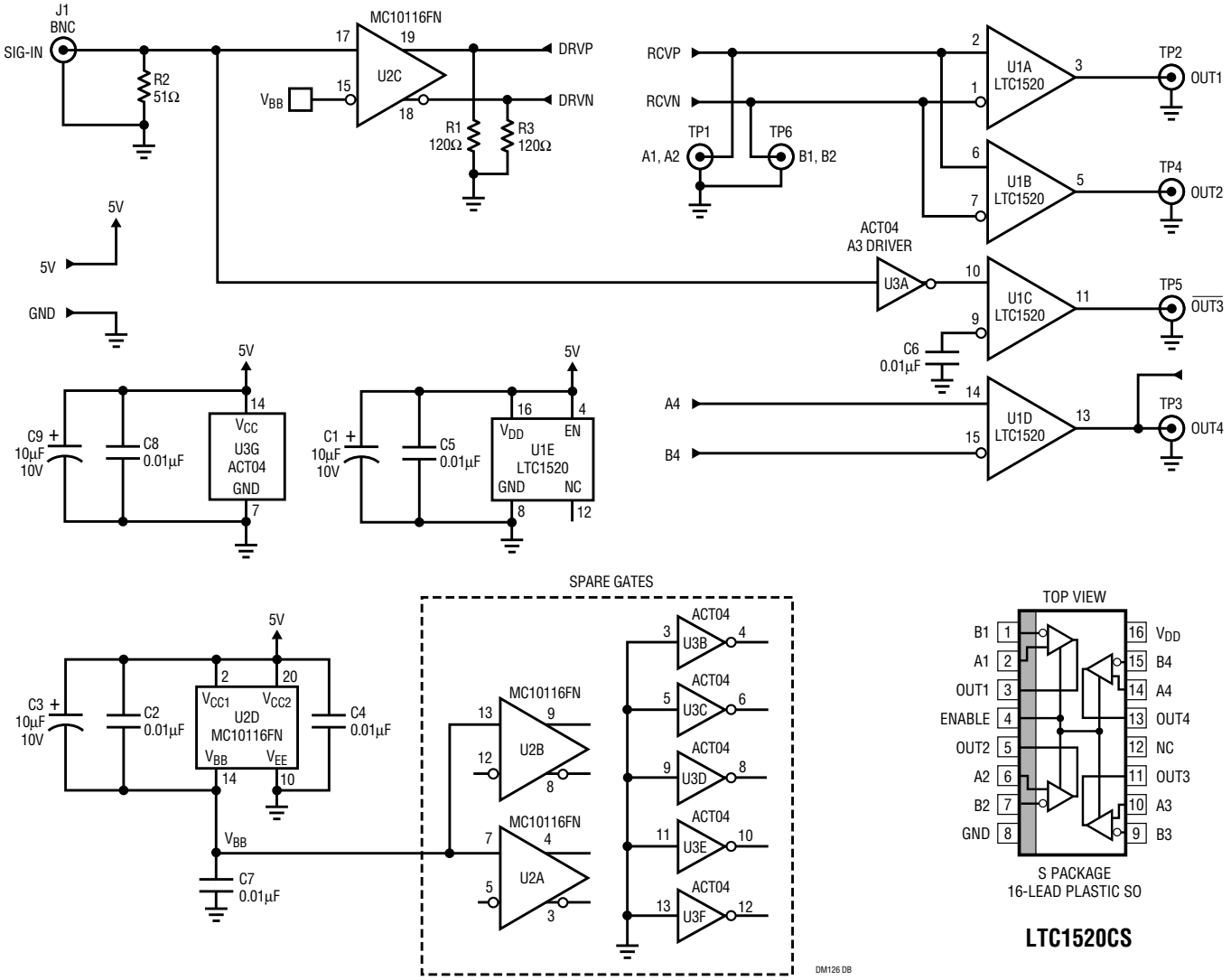


Figure 1. Demo Board Schematic

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1, C3, C9	3	TAJB106M010R	10μF 10V 20% Tantalum Capacitor	AVX	(207) 282-5111
C2, C4 to C8	6	08055C103MAT1A	0.01μF 50V 20% X7R Capacitor	AVX	(803) 946-0362
J1	1	112404	BNC 50Ω Connector	Connex	(805) 378-6464
R1, R3	2	CR21-121J-T	120Ω 1/10W 5% Chip Resistor	AVX	(803) 946-0524
R2	1	CR21-510J-T	51Ω 1/10W 5% Chip Resistor	AVX	(803) 946-0524
TP1 to TP6	6	131-4353-00	5mm Scope Probe Test Point	Tektronix	(800) 835-9433
U1	1	LTC1520CS	Quad Line Receiver SO-16 IC	LTC	(408) 432-1900
U2	1	MC10116FNR1	Triple Line Receiver PLCC-20 IC	Motorola	(602) 655-3005
U3	1	MC74ACT04DR1	Hex Inverter SO-14 IC	Motorola	(602) 655-3005

OPERATION

DC126 highlights the excellent propagation delay characteristics of the LTC1520 line receiver. Receivers A and B are driven differentially by the MC10116 PECL device. Because the inputs to these two receivers are the same, probing the two receiver outputs simultaneously will show channel-to-channel skew. Receiver C is driven by a CMOS inverter. Note that the negative input of Receiver C is not driven externally; it is internally self-biased to 3.3V. The 0.01µF C6 bypass capacitor is recommended for maximum frequency operation. Receiver D has both inputs brought out for the user to test some of the other features of the LTC1520, such as rail-to-rail input common mode, Hot Swap™ capable inputs which may be overdriven to ±10V and high input resistance (>18k, even when unpowered).

Equipment

In order to accurately measure the subnanosecond skews of the LTC1520, it is necessary to use high bandwidth equipment:

- 500MHz scope with high frequency FET probes
- ~3ns input rise/fall times input square wave (J1)

Receiver Skew

Connect DRVP to RCVP. Connect DRVN to RCVN. Make sure you use two small wires of equal length to make the connection. When a signal (square wave) is input to J1, OUT1 and OUT2 receiver outputs will show a 0.4ns typical skew. The FET probes must be inserted into the probe sockets; do not use the probe ground clips. This allows good grounding of the FET probes.

Twisted-Pair Connection

The LTC1520 can be used to receive high speed data over twisted-pair lines. One end of the twisted pair should be connected between DRVP and DRVN. The other end of the twisted pair should be terminated by a 120Ω resistor and connected between RCVP and RCVN. DC126 allows up to 50Mbps operation with a 100ft section of Category 5 twisted-pair wire. Longer wire will result in a lower maximum frequency.

Propagation Delay Measurement

Measure propagation delay by inserting one probe at RCVP and another at OUT1. Measure from the 50% point of the AC portion of the input to the 50% point of the AC portion of the output. Note that if the FET probes are not used, the probe capacitance may exceed 15pF, which will slightly increase the propagation delay (see the LTC1520 data sheet).

Single-Ended Operation

Receiver C is set up for single-ended operation. Its positive input is driven by a high speed CMOS hex inverter output. The negative input is connected only to a bypass capacitor, which is needed only during maximum frequency operation. The receiver inputs of the LTC1520 have an open-circuit voltage of 3.3V with a 5V supply, and a minimum input resistance of 18k. This configuration is useful for minimizing the number of routed lines on your PC board.

Uncommitted Receiver

The inputs to Receiver D have been left unconnected. This allows the user to test some of the other features of the LTC1520.

Temperature Stability

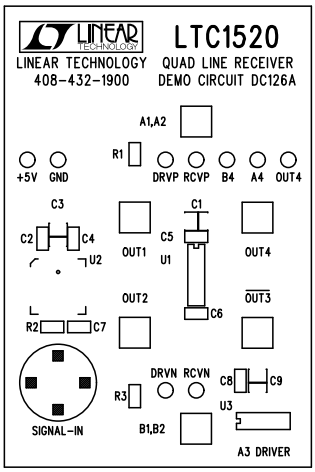
The LTC1520 is designed for superior temperature performance (see the data sheet). Make connections as described in the “Receiver Skew” section. Measure the propagation delay. Heat up/cool down the device. Remeasure the propagation delay. The propagation delay should change by less than ±1ns over the commercial temperature range.

Hot Swap is a trademark of Linear Technology Corporation.

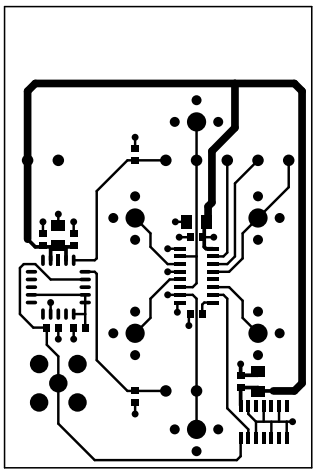
LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

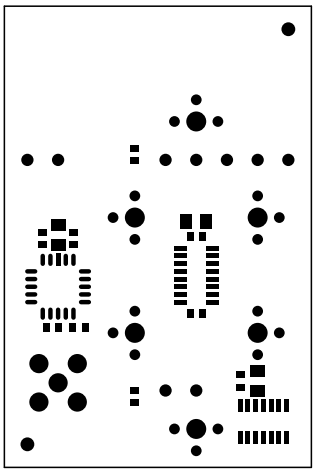
PCB LAYOUT AND FILM



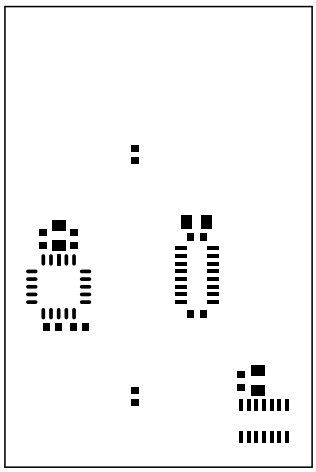
Component Side Silkscreen



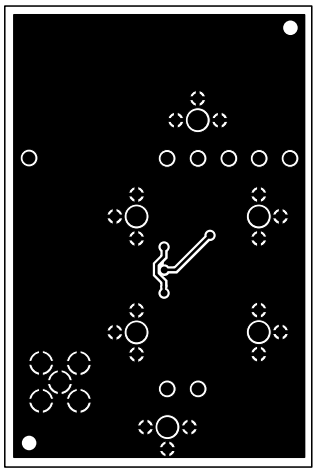
Component Side



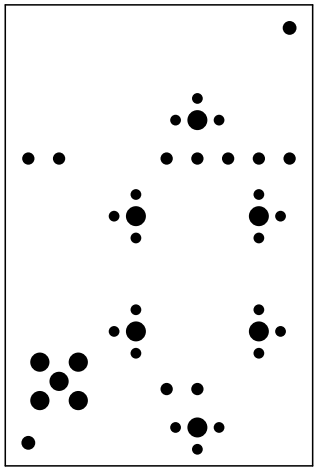
Component Side Solder Mask



Paste Mask Top

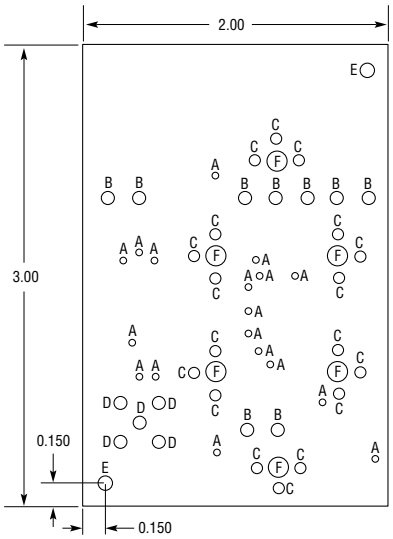


Solder Side



Solder Side Solder Mask

PC FAB DRAWING



SIZE	QTY	SYM	PLTD
0.015	18	A	Yes
0.026	9	B	Yes
0.035	18	C	Yes
0.052	5	D	Yes
0.070	2	E	No
0.090	6	F	Yes

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES ±0.003
2. FINISHED MATERIAL IS FR4, 0.062 THICK, 2 OZ COPPER, 2 LAYERS
3. FINISHED HOLE SIZES ARE +0.003/–0
4. PLATED HOLE WALL THICKNESS IS 0.001 MINIMUM
5. SOLDER MASK BOTH SIDES USING GREEN SR1020 OR EQUIVALENT
6. SILKSCREEN WHITE NONCONDUCTIVE INK COMPONENT SIDE

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