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NTE4066B & NTE4066BT
Integrated Circuit
CMOS, Quad Bilateral Switch

Description:

The NTE4066B (14–Lead DIP) and NTE4066BT (SOIC–14) are integrated circuits consisting of four independent switches capable of controlling either digital or analog signals. These quad bilateral switches are useful in signal gating, chopper, modulator, demodulator, and CMOS logic implementation.

The NTE4066B/BT is designed to be pin–for–pin compatible with the NTE4016B/BT, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

Features:

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range: 3V to 18V
- Linearized Transfer Characteristics
- Low Noise: $12nV/\sqrt{Cycle}$, $f \geq 1kHz$ typical

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1, Note 2)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Switch Through Current, I_{SW} . . . . . ±25mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Ambient Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Stresses exceeding maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Note 2. These devices contain protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. eiher V_{SS}, V_{EE} or V_{DD}), Unused outputs must be left open.

Electrical Characteristics: (Note 3)

Parameter	Symbol	V_{DD} Vdc	Test Conditions	−55°C		+25°C			+125°C		Unit
				Min	Max	Min	Typ	Max	Min	Max	
Supply Requirements (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	–		3	18	3	–	18	3	18	V
Quiescent Current Per Package	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}, Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$, and $\Delta V_{switch} \le 500mV$, Note 4	–	0.25	–	0.005	0.25	–	7.5	μA
		10		–	0.5	–	0.010	0.5	–	15	μA
		15		–	1.0	–	0.015	1.0	–	30	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5	T_A = +25°C only (The channel component, $(V_{in} - V_{out}) / R_{on}$, is not included)	Typical			(0.07μA/kHz) f + I_{DD}				μA
		10		Typical			(0.20μA/kHz) f + I_{DD}				μA
		15		Typical			(0.36μA/kHz) f + I_{DD}				μA
Control Inputs (Voltages Referenced to V_{SS})											
Low−Level Input Voltage	V_{IL}	5	R_{on} = per spec, I_{off} = per spec	–	1.5	–	2.25	1.5	–	1.5	V
		10		–	3.0	–	4.50	3.0	–	3.0	V
		15		–	4.0	–	6.75	4.0	–	4.0	V
High−Level Input Voltage	V_{IH}	5	R_{on} = per spec, I_{off} = per spec	3.5	–	3.5	2.75	–	3.5	–	V
		10		7.0	–	7.0	5.50	–	7.0	–	V
		15		11.0	–	11.0	8.25	–	11.0	–	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Capacitance	C_{in}	–		–	–	–	5.0	7.5	–	–	pF
Switches In/Out (Voltages Referenced to V_{SS})											
Recommended Peak−to−Peak Voltage Into or Out of the Switch	$V_{I/O}$	–	Channel On or Off	0	V_{DD}	0	–	V_{DD}	0	V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch (Note 4)	ΔV_{switch}	–	Channel On	0	600	0	–	600	0	300	mV
Output Offset Voltage	V_{OO}	–	V_{in} = 0V, No Load	–	–	–	10	–	–	–	μV
On Resistance	R_{on}	5	$\Delta V_{switch} \le 500mV$ (Note 4) $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	–	800	–	250	1050	–	1200	Ω
		10		–	400	–	120	500	–	520	Ω
		15		–	220	–	80	280	–	300	Ω
ΔOn Resistance between any Two Channels in the Same Package	ΔR_{on}	5		–	70	–	25	70	–	135	Ω
		10		–	50	–	10	50	–	95	Ω
		15		–	45	–	10	45	–	65	Ω
Off−Channel Leakage Current	$_{I}$off	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	–	±100	–	±0.05	±100	–	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	–	Switch Off	–	–	–	10	15	–	–	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	–		–	–	–	0.47	–	–	–	pF

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 4. For voltage drops across the switch (ΔV_{switch}) > 600mV (> 300mV at high temperatures), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded (See the first page of this data sheet).

Electrical Characteristics: (V_{SS} = –5V, C_L = 50pF, T_A = +25°C, Note 3, 5 unless otherwise specified)

Parameter	Symbol	V_{DD}	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Times Input to Output (V_{SS} = 0V, R_L = 10kΩ)	t_{PLH}, t_{PHL}	5	t_{PLH}, t_{PHL} = (0.17ns/pF) C_L + 15.5ns	–	20	40	ns
		10	t_{PLH}, t_{PHL} = (0.08ns/pF) C_L + 6.0ns	–	10	20	ns
		15	t_{PLH}, t_{PHL} = (0.06ns/pF) C_L + 4.0ns	–	7.0	15	ns
Control to Output Output "1" to High Impedance	t_{PHZ}	5	V_{SS} = 0V, R_L = 1kΩ	–	40	80	ns
		10		–	35	70	ns
		15		–	30	60	ns
Output "0" to High Impedance	t_{PLZ}	5		–	40	80	ns
		10		–	35	70	ns
		15		–	30	60	ns
High Impedance to Output "1"	t_{PZH}	5		–	60	120	ns
		10		–	20	40	ns
		15		–	15	30	ns
High Impedance to Output "0"	t_{PZL}	5		–	60	120	ns
		10		–	20	40	ns
		15		–	15	30	ns
Second Harmonic Distortion		5	V_{in} = 1.77V, RMS Centered @ 0V, R_L = 10kΩ, f = 1kHz, V_{SS} = –5V	–	0.1	–	%
Bandwidth (Switch ON)		5	R_L = 1kΩ, 20 Log V_{out}/V_{in} = –3dB, C_L = 50pF, V_{in} = $5V_{P-P}$, V_{SS} = –5V	–	65	–	MHz
Feedthrough Attenuation (Switch OFF)		5	V_{in} = $5V_{P-P}$, R_L = 1kΩ, f_{in} = 1Mhz, V_{SS} = –5V	–	–50	–	dB
Channel Separation		5	V_{in} = $5V_{P-P}$, R_L = 1kΩ, f_{in} = 8MHz, Switch A ON, Switch B OFF, V_{SS} = –5V	–	–50	–	dB
Crosstalk, Control Input to Signal Output		5	V_{SS} = –5V, R_1 = 1kΩ, R_L = 10kΩ, Control t_{TLH} = t_{THL} = 20ns	–	300	–	mV_{P-P}

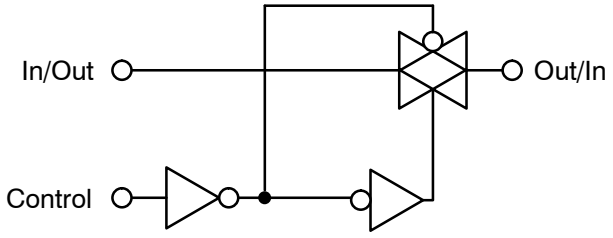
Note 3. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

Note 5. The formulas given are for the typical characteristics only at +25°C.

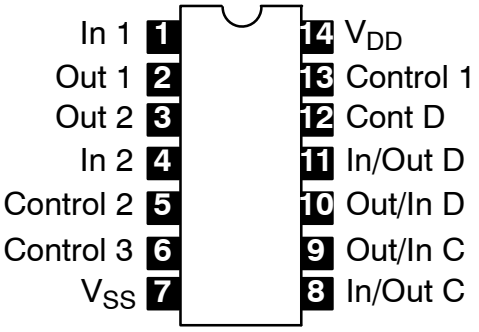
Logic Diagram and Truth Table: (1/4 of Device Shown)

Control	Switch
0 = V_{SS}	OFF
1 = V_{DD}	ON

Logic Diagram Restrictions
$V_{SS} \le V_{in} \le V_{DD}$
$V_{SS} \le V_{out} \le V_{DD}$



Pin Connection Diagram



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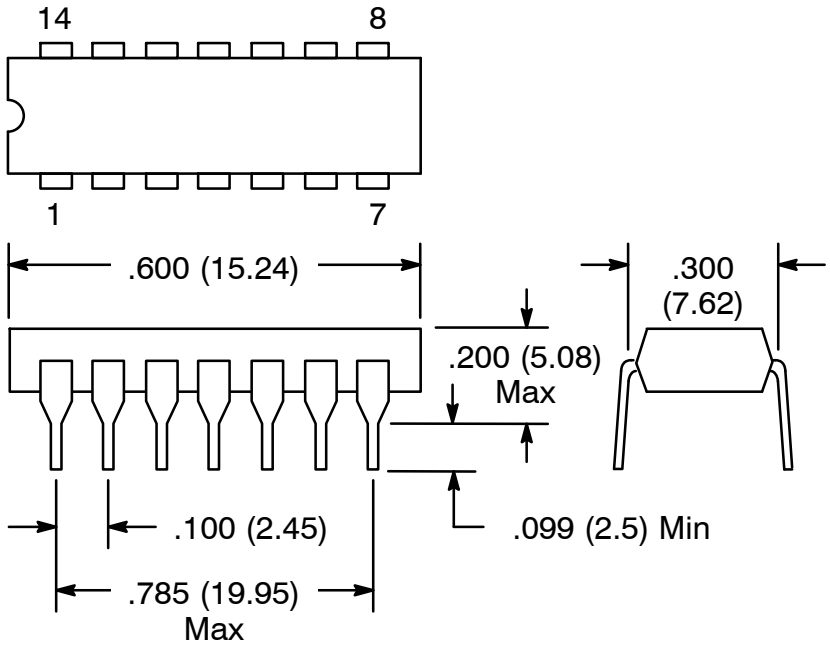
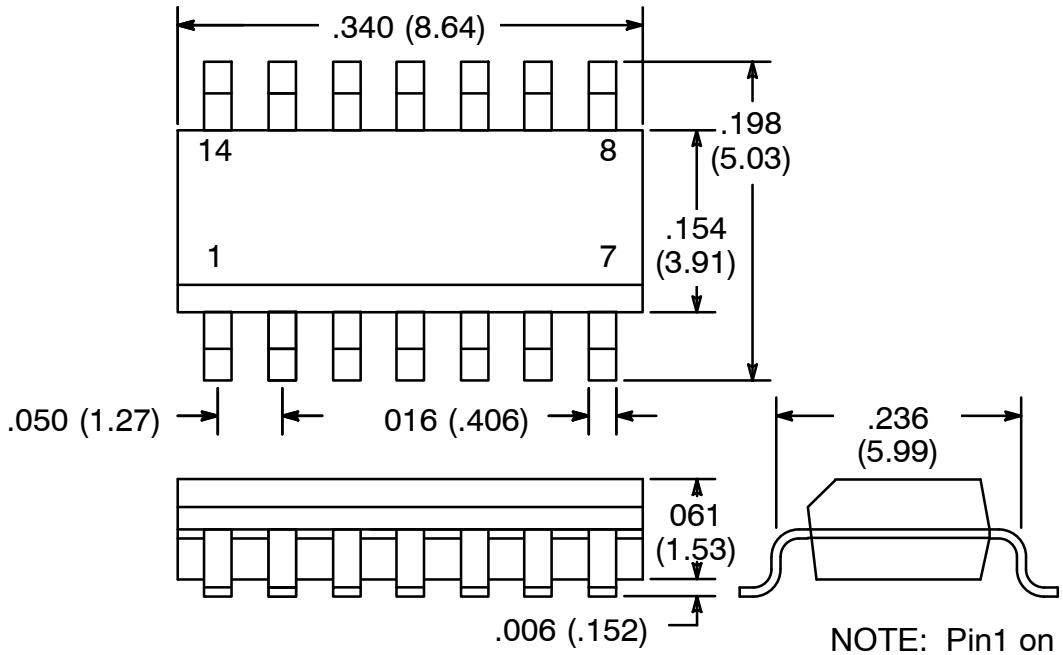


NTE4066BT



NOTE: Pin1 on Beveled Edge