NCP102

Low Dropout Linear Regulator Controller

The NCP102 is a low dropout linear regulator controller for applications requiring high−current and ultra low dropout voltages. The use of an external N−Channel MOSFET allows the user to adapt the device to a multitude of applications depending on system requirements for current and dropout voltage.

An extremely accurate 0.8 V (±2%) reference allows the implementation of sub 1 V voltage supplies. The reference is guaranteed over the complete supply and temperature ranges.

Other features of the NCP102 are a dedicated enable input, internally compensated error amplifier and an adjustable soft−start. A minimum drive capability of ±5 mA provides fast transient response. The drive current is internally limited to protect the controller in case of an external MOSFET failure. The NCP102 is packaged in a space saving TSOP−6.

Features

- 4.5 V to 13.5 V Supply Voltage Range
- 0.8 V (±2%) Voltage Reference (Temperature and Process)
- Programmable Regulator Output Voltage Down to 0.8 V
- Drive Current Capability of > ±5 mA
- MLCC and POSCAP Compatible
- Programmable Soft−Start
- Enable Active High
- Space Saving TSOP−6 Package
- RoHS Compliant Pb−Free Package

Applications

- Desktop and Laptops
- Computer Peripherals such as Graphics Cards
- Sub 1 V Power Supplies

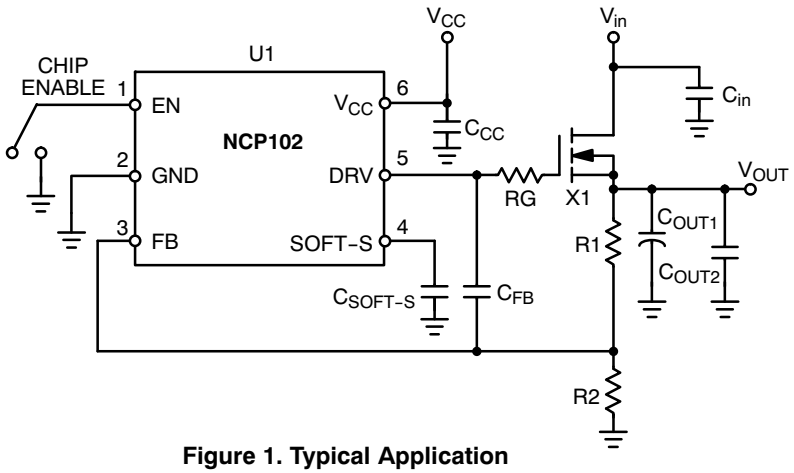

Figure 1. Typical Application

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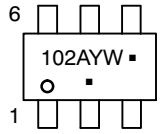
http://onsemi.com

MARKING DIAGRAM

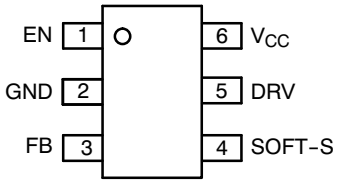
TSOP−6
(SOT23−6)
SN SUFFIX
CASE 318G



102	= Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP102SNT1G	TSOP−6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

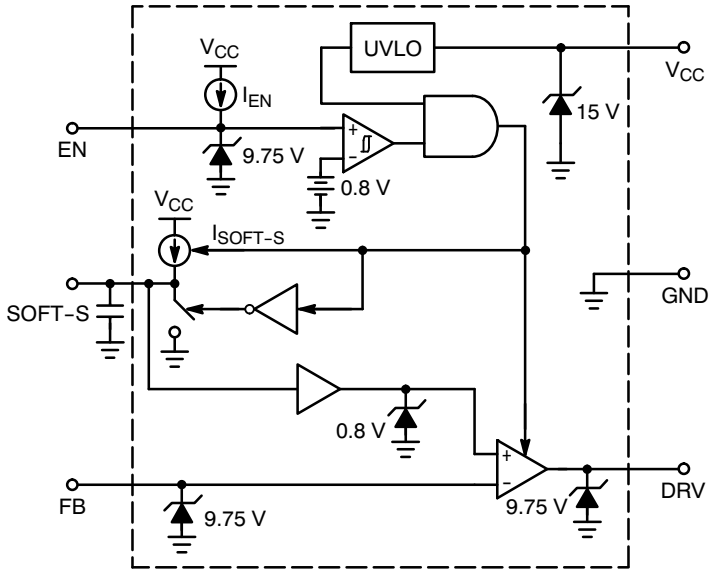


Figure 2. Representative Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol Name	Description
1	EN	Enable Input (Active High). Pull the EN pin below 0.8 V to disable the regulator and enter the standby mode operation.
2	GND	Ground
3	FB	Inverting input of the error amplifier. The output voltage is sampled by means of a resistor divider and applied to this pin for regulation.
4	SOFT−S	Programmable soft−start. An internal current source charges the capacitor connected to this pin. The soft−start period ends once the voltage of the soft−start capacitor reaches 0.8 V.
5	DRV	Gate drive for external N−Channel MOSFET. It is also the buffered output of the error amplifier.
6	V_{CC}	Power supply voltage input. Operating voltage range is from 4.5 to 13.5 V. A decoupling capacitor to GND should be used. A minimum of 0.1 μF is recommended.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Main Supply Input Voltage Main Supply Input Current	V_{CC} I_{CC}	−0.3 to 15 100	V mA
Enable Voltage Enable Current	V_{EN} I_{EN}	−0.3 to 9.75 100	V mA
Soft−Start Voltage Soft−Start Current	V_{SOFT-S} I_{SOFT-S}	−0.3 to 9.75 100	V mA
Drive Voltage Drive Current	V_{DRV} I_{DRV}	−0.3 to 9.75 100	V mA
Feedback Voltage Feedback Current	V_{FB} I_{FB}	−0.3 to 9.75 100	V mA
Thermal Resistance, Junction−to−Ambient (0.36 sq in Printed Circuit Copper Clad) (1.0 sq in Printed Circuit Copper Clad)	$R_{\theta JA}$	 230 200	°C/W
Power Dissipation (T_A = 25°C, 2 oz Cu, 0.36 sq in Printed Circuit Copper Clad)	P_D	0.4	W
Storage Temperature Range	T_{stg}	−65 to 150	°C
Operating Junction Temperature Range	T_J	−40 to 125	°C
Reflow Temperature 10 seconds	T_{reflow}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115
2. Latch−up current maximum rating: ±100 mA per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{EN} = 1 V, V_{DRV} = V_{FB}, V_{SS} = open, C_{CC} = 0.1 μF. For typical values T_J = 25°C. For min/max values, T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Condition		Min	Typ	Max	Unit
POWER SUPPLY						
Supply Voltage		V_{CC}	4.5	–	13.5	V
Supply Current	V_{CC} = 5 V V_{CC} = 12 V	I_{CC1} I_{CC2}	– –	1.4 1.8	3.2 3.2	mA
V_{CC} Startup Voltage	V_{CC} increasing	$V_{CC(on)}$	4.0	4.2	4.5	V
V_{CC} Turn Off Voltage	V_{CC} decreasing	$V_{CC(off)}$	3.8	4.0	4.4	V
V_{CC} Hysteresis	$V_{CC(on)}$ − $V_{CC(off)}$	$V_{CC(hys)}$	0.10	0.24	0.30	V
Standby Current	V_{EN} = 0 V, V_{CC} = 5 V V_{EN} = 0 V, V_{CC} = 12 V	$I_{CC(off1)}$ $I_{CC(off2)}$	– –	0.3 0.48	0.8 1.5	mA
ERROR AMPLIFIER						
Input Bias Current	V_{FB} = 1.0 V	I_{FB}	−1.0	–	1.0	μA
Open Loop DC Gain (Note 3)		A_v	55	70	–	dB
Unity Gain Bandwidth	V_{FB} = V_{DRV}	BW	–	0.7	–	MHz
Power Supply Rejection Ratio (Note 3)	V_{CC} = 12 V, 100 Hz	PSRR	50	–	–	dB
DRIVE						
Sink Current	V_{DRV} = 6 V, V_{FB} = 1 V V_{DRV} = 2.5 V, V_{CC} = 5 V V_{FB} = 1 V	$I_{DRV(SNK1)}$ $I_{DRV(SNK2)}$	5.0 5.0	– –	– –	mA
Source Current	V_{DRV} = 6 V, V_{FB} = 0.6 V V_{DRV} = 2.5 V, V_{CC} = 5 V, V_{FB} = 0.6 V	$I_{DRV(SRC1)}$ $I_{DRV(SRC2)}$	5.0 5.0	– –	– –	mA
Output Voltage Low State High State	I_{DRV} = 5 mA, V_{FB} = 1 V I_{DRV} = 5 mA, V_{FB} = 0.6 V, V_{CC} = 9.5 V	$V_{DRV(low)}$ $V_{DRV(high)}$	– 9.0	– –	0.5 –	V
Drive Current Under Fault Conditions T_J = 25°C	V_{DRV} = 0 V, V_{FB} = 0.6 V V_{DRV} = open, V_{FB} = 0.6 V	$I_{DRV(MAX1)}$ $I_{DRV(MAX2)}$	– –	– –	45 40	mA
SOFT−START						
Source Current	V_{SOFT-S} = 1 V	I_{SOFT-S}	3.5	4.5	6.2	μA
ENABLE						
Source Current		I_{EN}	5.0	10	15	μA
Input Threshold Voltage On State Off State	 V_{EN} Increasing V_{EN} Decreasing	 $V_{EN(on)}$ $V_{EN(off)}$	 0.7 0.66	 0.8 0.77	 0.9 0.88	V
Threshold Voltage Hysteresis	$V_{EN(on)}$ − $V_{EN(off)}$	$V_{EN(hys)}$	–	35	–	mV
REFERENCE						
Reference Voltage	V_{CC} = 5 V, V_{CC} = 12 V	V_{REF}	0.784	0.8	0.816	V

3. Guaranteed by design.

TYPICAL CHARACTERISTICS

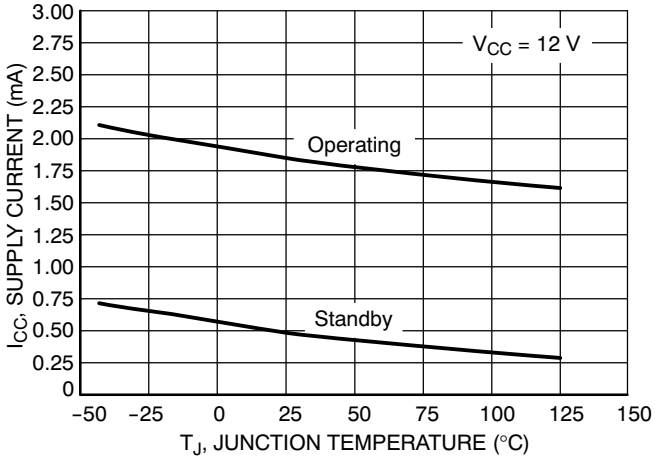


Figure 3. Supply Current vs. Junction Temperature

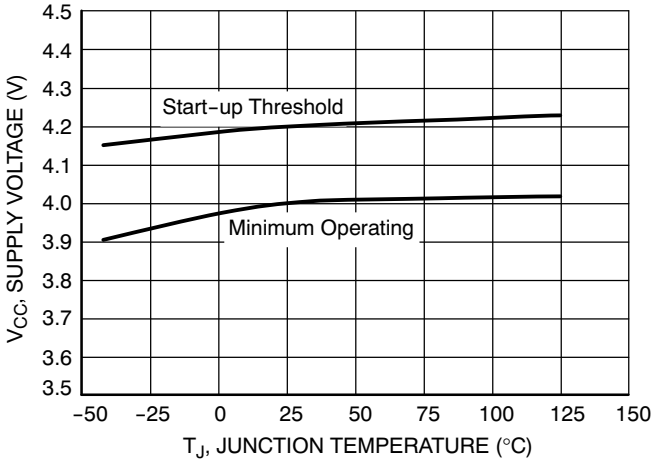


Figure 4. Supply Voltage Thresholds vs. Junction Temperature

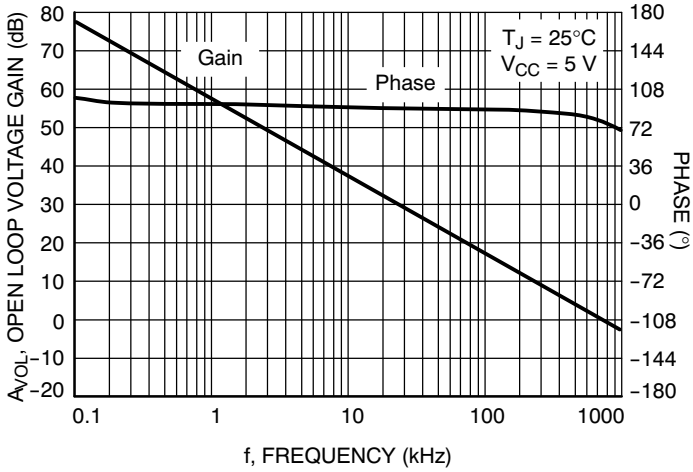


Figure 5. Error Amplifier Open Loop Voltage Gain/Phase vs. Frequency

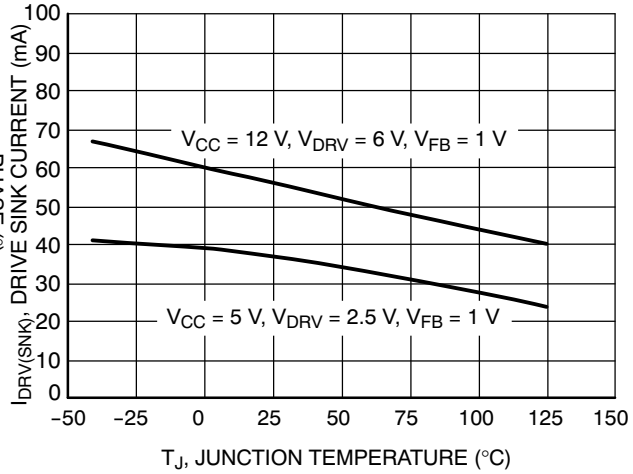


Figure 6. Drive Sink Current vs. Junction Temperature

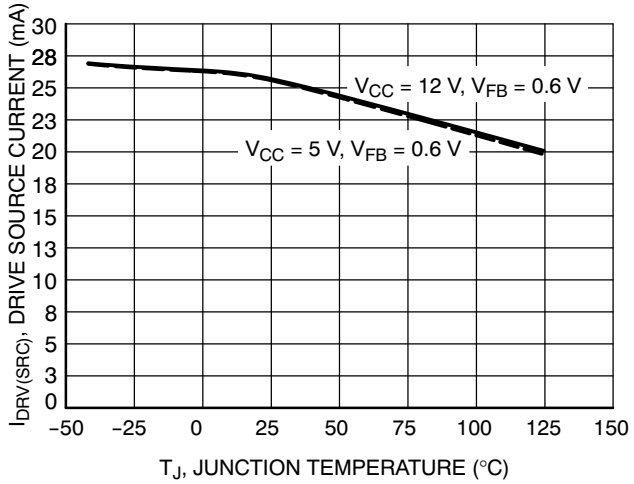


Figure 7. Drive Source Current vs. Junction Temperature

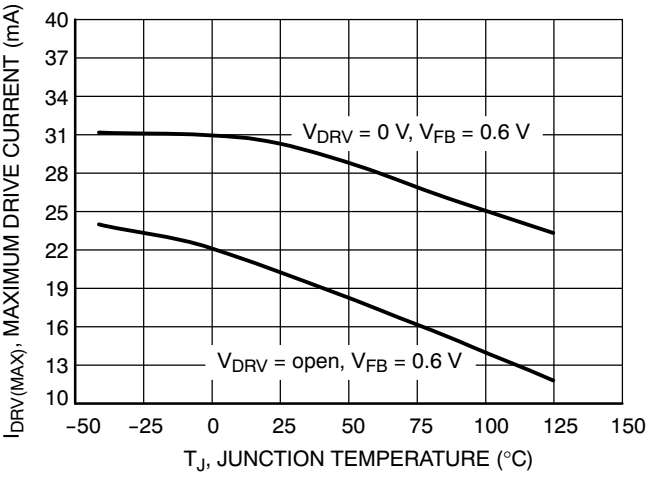


Figure 8. Drive Current Under Fault Conditions vs. Junction Temperature

TYPICAL CHARACTERISTICS

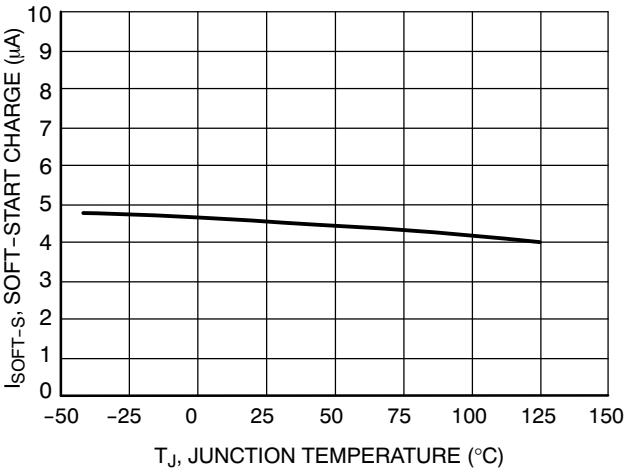


Figure 9. Soft−Start Charge Current vs. Junction Temperature

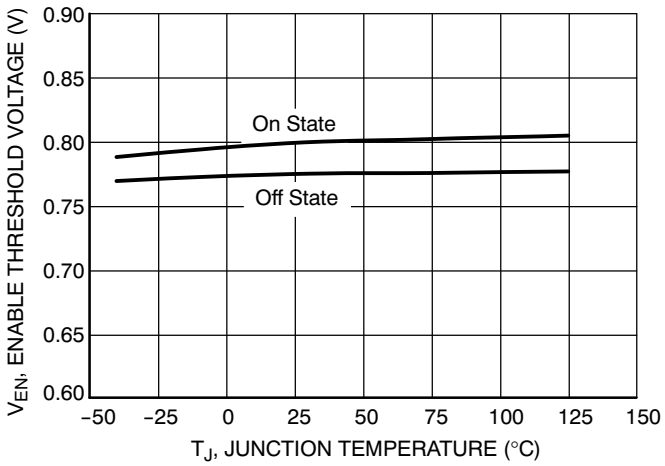


Figure 10. Enable Threshold Voltages vs. Junction Temperature

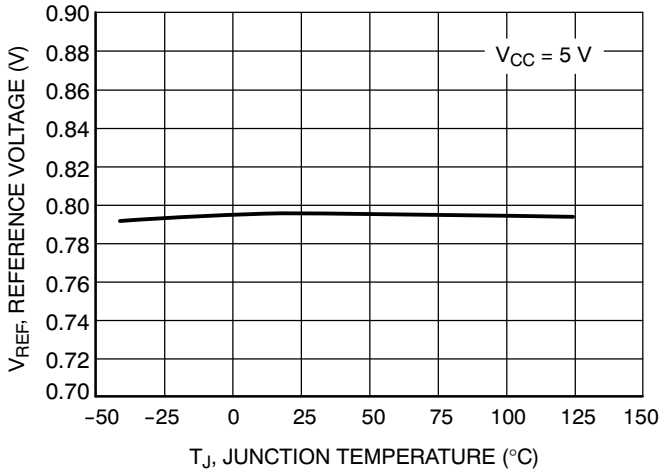


Figure 11. Reference Voltage vs. Junction Temperature

DETAILED OPERATING DESCRIPTION

The NCP102 is a low dropout linear regulator controller for applications requiring high−current and ultra low dropout voltages. The use of an external N−Channel MOSFET allows the user to adapt the device to a multitude of applications depending on system requirements for current and dropout voltage.

An extremely accurate 0.8 V (±2%) reference allows the implementation of sub 1 V voltage supplies. The reference is guaranteed over the complete supply and temperature ranges.

Other features of the NCP102 are a dedicated enable input, internally compensated error amplifier and an adjustable soft−start. A minimum drive capability of ±5 mA provides fast transient response. The drive current is internally limited to protect the controller in case of an external MOSFET failure. The NCP102 is packaged in a space saving TSOP−6.

SUPPLY VOLTAGE

The NCP102 supply voltage range is between 4.5 V and 13.5 V. The controller is enabled once the supply voltage exceeds its minimum supply threshold, typically 4.5 V. The minimum operating voltage is reduced to 4.2 V (typical) once the controller is enabled to provide noise immunity.

A bypass capacitor is required on the V_{CC} pin to provide charge storage during power up and transient events. A minimum of 0.1 μF is recommended.

DRIVE OUTPUT

A powerful error amplifier (EA) capable of driving an external MOSFET is built into the NCP102. The output of the error amplifier is connected to the DRV pin. It has a minimum drive current capability of ±5 mA providing a fast transient response.

The EA is biased directly from V_{CC}. The DRV voltage follows V_{CC} up and it is internally clamped to 9.75 V (typ.). This allows the use of external MOSFETs with a maximum gate voltage of 12 V.

The DRV current is provided directly from V_{CC}. Therefore, the V_{CC} capacitor should be large enough to maintain a constant V_{CC} during power up and transients. Otherwise, the supply voltage may collapse reaching the controller undervoltage lockout threshold.

INTERNAL REFERENCE

The internal 0.8 V reference facilitates the implementation of sub 1 V supplies required in modern computing equipment. The internal reference is trimmed during manufacturing to obtain better than ±2% accuracy over the complete operating range.

The output voltage, V_{out}, is programmed using a resistor divider (R1 and R2) as shown in Figure 1.

The resistor divider senses the output voltage and compares it to the internal 0.8 V reference.

Equation 1 relates the output voltage to the internal reference voltage and external resistors R1 and R2.

$$V_{out} = V_{REF} \cdot \left(\frac{R1 + R2}{R2}\right) \qquad \text{(eq. 1)}$$

ERROR AMPLIFIER

The NCP102 has a wide bandwidth error amplifier. It allows the user to implement a wide bandwidth feedback loop resulting in better transient response and lower system cost. It requires the user to compensate the system. A narrow bandwidth error amplifier usually does not require external compensation but it requires more output capacitance to meet typical transient requirements.

The output of the error amplifier is available for frequency compensation. A capacitor (C_{COMP}) can be placed between the DRV and FB pins. In most cases the resistor is not needed. The uncompensated error amplifier dominant pole is approximately 1.65 Hz. Any external capacitance between the DRV and FB pins reduces the dominant pole frequency due to the Miller multiplication effect. Equation 2 relates the dominant pole frequency to C_{COMP}.

$$f_{pole} = 6.7016 \cdot C_{COMP}^{-0.846} \qquad \text{(eq. 2)}$$

EXTERNAL ENABLE

The EN input allows the NCP102 to be remotely enabled. An internal 10 μA (typ.) current source pulls up the EN voltage. The EN pin is internally pulled to V_{CC} or 9.5 V, whichever is lower.

The controller is enabled once the EN pin voltage exceeds 0.8 V (typ.). The controller is disabled by pulling down on the EN pin. Figure 12 shows the relationship between enable and soft−start.

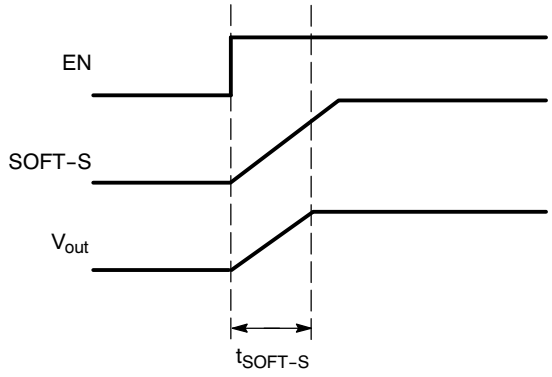


Figure 12. Relationship Between Enable and Soft−Start

The EN pin can be connected to V_{CC} if the enable feature is not used. If connected to V_{CC} and V_{CC} is higher than 9.5 V a resistor in series should be used to limit the current into the EN pin as the pin is internally clamped to 9.5 V. A minimum of 40 kΩ is recommended.

SOFT−START

Soft−start reduces inrush current and overshoot of the output voltage. The adjustable soft−start built into the NCP102 allows the user to select the optimum soft−start time for the application. The soft−start time is set with a capacitor from the SOFT−S pin to ground.

Soft−start is achieved by controlling the slope of the DRV voltage based on the slope of the soft−start capacitor voltage, C_{SOFT-S}. The capacitor is charged to V_{CC} with a constant 4.5 μA (typ.) current source, I_{SOFT-S}. This results in a linear charge of the soft−start capacitor and thus the output voltage. The soft−start period, t_{SOFT-S}, ends once the capacitor voltage reaches 0.8 V (typ). The soft−start capacitor is calculated using Equation 3.

$$t_{SOFT-S} = \left(\frac{C_{SOFT-S} \cdot 0.8}{I_{SOFT-S}}\right) \quad \text{(eq. 3)}$$

The soft−start capacitor is internally pulled to GND when V_{CC} is not within its operating range or the controller is disabled using the EN pin.

POWER SEQUENCING

Power sequencing can be easily implemented using the SOFT−S and EN pins. This is achieved by directly connecting the SOFT−S pin of the master controller to the EN pin of the slave controller. If V_{CC} is above 9.5 V a resistor divider is required to limit the voltage on the EN pin because the pin is internally clamped to 9.5 V. Figure 13 shows the timing waveforms of the master and slave controllers.

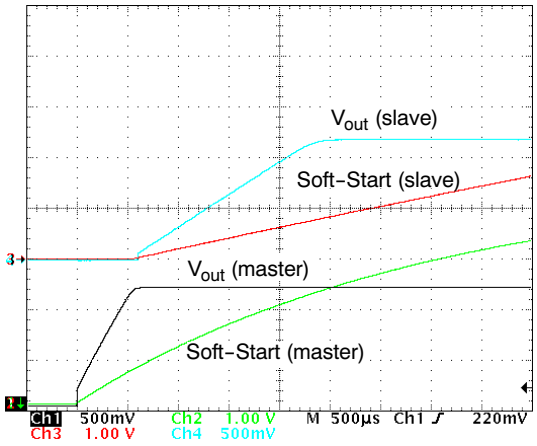


Figure 13. Power−up Sequencing Waveforms

Power sequencing will affect the soft−start time calculated using Equation 3 because the soft−start capacitor charge current is now increased by the enable charge current. The soft−start time is calculated using Equation 3 by replacing I_{SOFT-S} with the sum of I_{EN} and I_{SOFT-S}.

APPLICATION INFORMATION

ON Semiconductor provides an electronic design tool, a demonstration board and an application note to facilitate design using the NCP102 and to reduce development cycle time. All the tools can be downloaded at www.onsemi.com.

The electronic design tool allows the user to easily determine most of the system parameters of a linear regulator. The tool also evaluates the frequency response of the system. The demonstration board is designed to generate a 1.2 V/3 A voltage supply from a 1.8 V supply. The circuit schematic is shown in Figure 14 and the regulator design is described in Application Note AND8303.

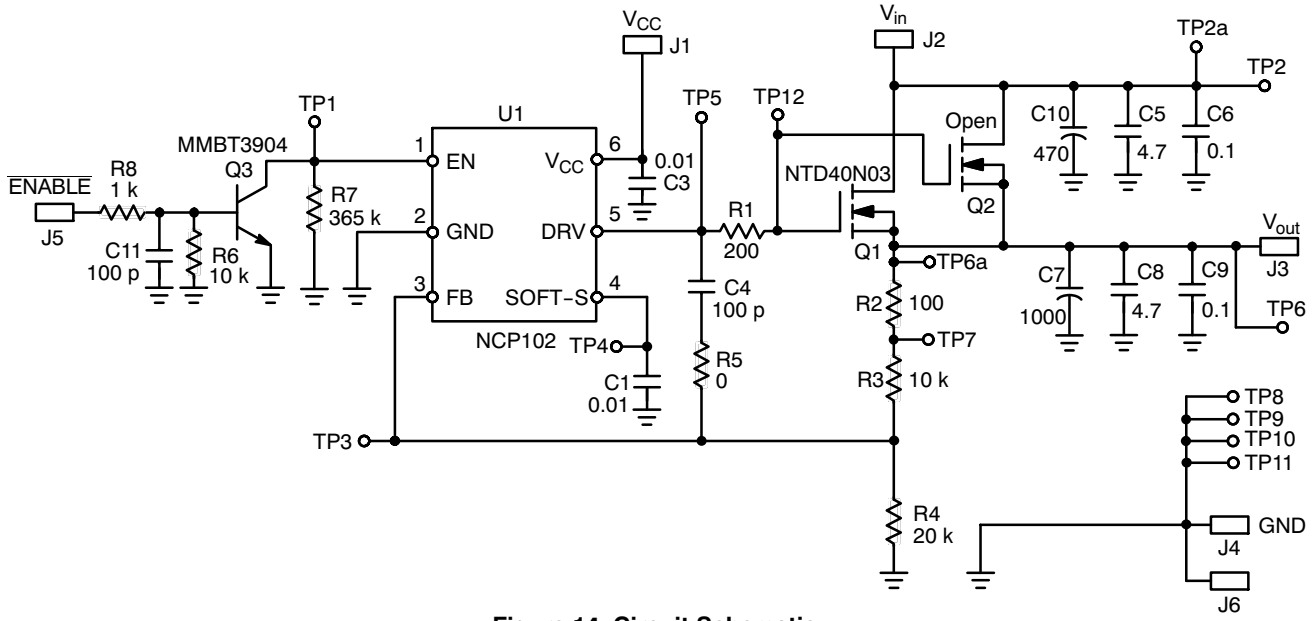


Figure 14. Circuit Schematic

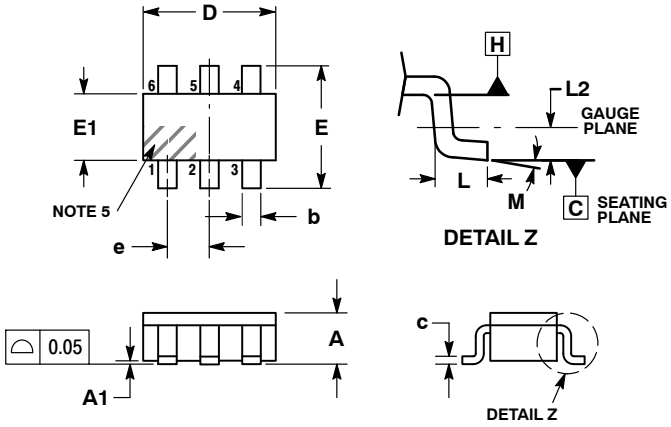
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

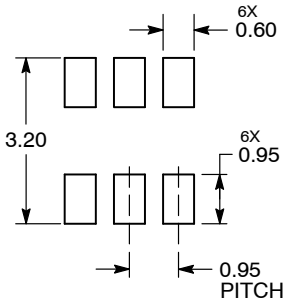
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

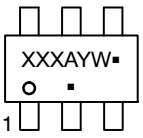
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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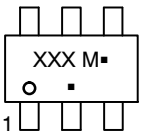

STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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