

**DUAL MICROPOWER PRECISION RAIL-TO-RAIL CMOS OPERATIONAL AMPLIFIER**

**GENERAL DESCRIPTION**

The ALD2711A/ALD2711B/ALD2711 is a dual monolithic CMOS micropower precision high slew rate operational amplifier intended for a broad range of analog applications using  $\pm 1V$  to  $\pm 5V$  dual power supply systems, as well as +2V to +10V battery operated systems. All device characteristics are specified for +5V single supply or  $\pm 2.5V$  dual supply systems. Typical supply current is 200 $\mu A$  at 5V supply voltage. It is manufactured with Advanced Linear Devices' enhanced AC MOS silicon gate CMOS process.

The ALD2711A/ALD2711B/ALD2711 has been developed specifically for the +5V single supply or  $\pm 1V$  to  $\pm 5V$  dual supply user and has an input stage that operates to +300mV above and -300mV below the supply voltages with no adverse effects and/or phase reversals.

Several important characteristics of the device make application easier to implement at those voltages. First, each operational amplifier can operate with rail to rail input and output voltages. This means the signal input voltage and output voltage can be at the positive and negative supply voltages. This feature allows numerous analog serial stages and flexibility in input signal bias levels. Second, each device was designed to accommodate mixed applications where digital and analog circuits may operate off the same power supply or battery. Third, the output stage can typically drive up to 50pF capacitive and 10K $\Omega$  resistive loads.

These features, combined with extremely low input currents, high open loop voltage gain, high useful bandwidth, and slew rate make the ALD2711A/ALD2711B/ALD2711 a versatile, micropower operational amplifier.

The ALD2711A/ALD2711B/ALD2711 with on-chip offset voltage trimming allows the device to be used without nulling in most applications. Additionally, robust design and rigorous screening make this device especially suitable for operation in temperature-extreme environments and rugged conditions.

The unique characteristics of the ALD2711A/ALD2711B/ALD2711 are modeled in an available macromodel.

**ORDERING INFORMATION** ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to 125°C
8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD2711ASAL	ALD2711APAL	ALD2711ADA
ALD2711BSAL	ALD2711BPAL	ALD2711BDA
ALD2711SAL	ALD2711PAL	ALD2711DA

\* Contact factory for leaded (non-RoHS) or high temperature versions.

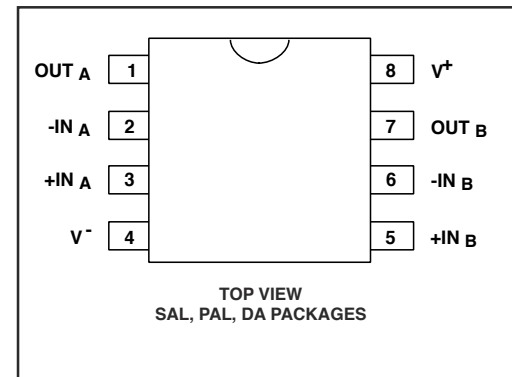
**FEATURES**

- Designed and characterized for 5V operation
- Linear mode operation with input voltages 300mV beyond supply rails
- Output voltages to within 2mV of power supply rails when driving a high impedance load
- Unity gain stable
- Extremely low input bias currents -- 0.01pA
- Dual power supply  $\pm 1.0V$  to  $\pm 5.0V$
- Single power supply +2V to +10V
- High voltage gain
- Output short circuit protected
- Unity gain bandwidth of 0.7MHz
- Slew rate of 0.7V/ $\mu s$
- Low power dissipation
- Symmetrical complementary output drive
- Suitable for rugged, temperature-extreme environments

**APPLICATIONS**

- Voltage follower/buffer/amplifier
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter

**PIN CONFIGURATION**



## ABSOLUTE MAXIMUM RATINGS

Supply voltage,  $V_+$  \_\_\_\_\_ 10.6V  
 Differential input voltage range \_\_\_\_\_ -0.3V to  $V_+ + 0.3V$   
 Power dissipation \_\_\_\_\_ 600 mW  
 Operating temperature range SAL, PAL packages \_\_\_\_\_  $0^\circ\text{C}$  to  $+70^\circ\text{C}$   
 DA package \_\_\_\_\_  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Storage temperature range \_\_\_\_\_  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Lead temperature, 10 seconds \_\_\_\_\_  $+260^\circ\text{C}$

**CAUTION:** ESD Sensitive Device. Use static control procedures in ESD controlled environment.

## OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$   $V_S = \pm 2.5V$  unless otherwise specified

Parameter	Symbol	2711A			2711B			2711			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Supply Voltage	$V_S$	$\pm 1.0$		$\pm 5.0$	$\pm 1.0$		$\pm 5.0$	$\pm 1.0$		$\pm 5.0$	V	Dual Supply Single Supply
	$V_+$	2.0		10.0	2.0		10.0	2.0		10.0	V	
Input Offset Voltage	$V_{OS}$		0.25	1.0 1.4		0.5	1.4 1.9		0.8	1.9 2.4	mV mV	$R_S \leq 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
Input Offset Current	$I_{OS}$		0.01	10 280		0.01	10 280		0.01	10 280	pA pA	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
Input Bias Current	$I_B$		0.01	10 280		0.01	10 280		0.01	10 280	pA pA	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
Input Voltage Range	$V_{IR}$	-0.3 -2.8		5.3 2.8	-0.3 -2.8		5.3 2.8	-0.3 -2.8		5.3 2.8	V V	$V_+ = +5V$ $V_S = \pm 2.5V$
Input Resistance	$R_{IN}$		$10^{13}$			$10^{13}$			$10^{13}$		$\Omega$	
Input Offset Voltage Drift	$TCV_{OS}$		5			5			7		$\mu\text{V}/^\circ\text{C}$	$R_S \leq 100K\Omega$
Power Supply Rejection Ratio	PSRR	63	90		63	90		60	90		dB	$R_S \leq 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
		63	90		63	90		60	90		dB	
Common Mode Rejection Ratio	CMRR	63	90		63	90		60	90		dB	$R_S \leq 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
		63	90		63	90		60	90		dB	
Large Signal Voltage Gain	$A_V$	15	100 300		15	100 300		10	100 300		V/mV V/mV V/mV	$R_L = 100K\Omega$ $R_L \geq 1M\Omega$ $R_L = 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
		10			10			7				
Output Voltage Range	$V_O$ low		0.001	0.01		0.001	0.01		0.001	0.01	V	$R_L = 1M\Omega$ $V_+ = +5V$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
	$V_O$ high	4.99	4.999		4.99	4.999		4.99	4.999		V	
	$V_O$ low		-2.48	-2.40		-2.48	-2.40		-2.48	-2.40	V	$R_L = 100K\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
	$V_O$ high	2.40	2.48		2.40	2.48		2.40	2.48		V	
Output Short Circuit Current	$I_{SC}$		1			1			1		mA	
Supply Current	$I_S$		200	450		200	450		200	450	$\mu\text{A}$	$V_{IN} = 0V$ No Load
Power Dissipation	$P_D$		1.0 0.25	2.25 0.6		1.0 0.25	2.25 0.6		1.0 0.25	2.25 0.6	mW	$V_S = \pm 2.5V$ Both $V_S = \pm 1.0V$ amplifiers

## OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

**T<sub>A</sub> = 25°C V<sub>S</sub> = ±2.5V unless otherwise specified**

Parameter	Symbol	2711A			2711B			2711			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Capacitance	C <sub>IN</sub>		1			1			1		pF	
Bandwidth	B <sub>W</sub>		700			700			700		KHz	
Slew Rate	S <sub>R</sub>		0.7			0.7			0.7		V/μs	A <sub>V</sub> = +1 R <sub>L</sub> = 100KΩ
Rise time	t <sub>r</sub>		0.2			0.2			0.2		μs	R <sub>L</sub> = 100KΩ
Overshoot Factor			20			20			20		%	R <sub>L</sub> = 100KΩ C <sub>L</sub> = 50pF
Settling Time	t <sub>s</sub>		10.0			10.0			10.0		μs	0.1% A <sub>V</sub> = 100 R <sub>L</sub> = 100KΩ C <sub>L</sub> = 50pF
Channel Separation	C <sub>S</sub>		140			140			140		dB	A <sub>V</sub> = 100

**T<sub>A</sub> = 25°C V<sub>S</sub> = ±5.0V unless otherwise specified**

Parameter	Symbol	2711A			2711B			2711			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Power Supply Rejection Ratio	PSRR		100			100			100		dB	R <sub>S</sub> ≤ 100KΩ
Common Mode Rejection Ratio	CMRR		100			100			100		dB	R <sub>S</sub> ≤ 100KΩ
Large Signal Voltage Gain	A <sub>V</sub>		300			300			300		V/mV	R <sub>L</sub> = 100KΩ
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high	4.90	-4.98 4.98	-4.90	4.90	-4.98 4.98	-4.90	4.90	-4.98 4.98	-4.90	V V	R <sub>L</sub> = 100KΩ
Bandwidth	B <sub>W</sub>		1.0			1.0			1.0		MHz	
Slew Rate	S <sub>R</sub>		1.0			1.0			1.0		V/μs	A <sub>V</sub> = +1 C <sub>L</sub> = 50pF

**V<sub>S</sub> = ±2.5V -55°C ≤ T<sub>A</sub> ≤ +125°C unless otherwise specified**

Parameter	Symbol	2711ADA			2711BDA			2711DA			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V <sub>OS</sub>			2.2			2.7			3.2	mV	R <sub>S</sub> ≤ 100KΩ
Input Offset Current	I <sub>OS</sub>			4			4			4	nA	
Input Bias Current	I <sub>B</sub>			4			4			4	nA	
Power Supply Rejection Ratio	PSRR	60	85		60	85		60	85		dB	R <sub>S</sub> ≤ 100KΩ
Common Mode Rejection Ratio	CMRR	60	83		60	83		60	83		dB	R <sub>S</sub> ≤ 100KΩ
Large Signal Voltage Gain	A <sub>V</sub>	10	50		10	50		10	50		V/mV	R <sub>L</sub> ≤ 100KΩ
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high	2.35	-2.47 2.45	-2.40	2.35	-2.47 2.45	-2.40	2.35	-2.47 2.45	-2.40	V V	R <sub>L</sub> ≤ 100KΩ

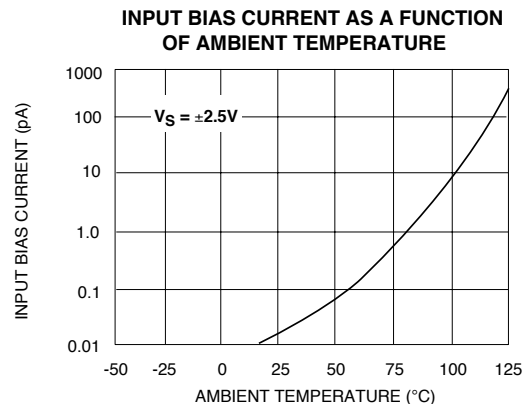
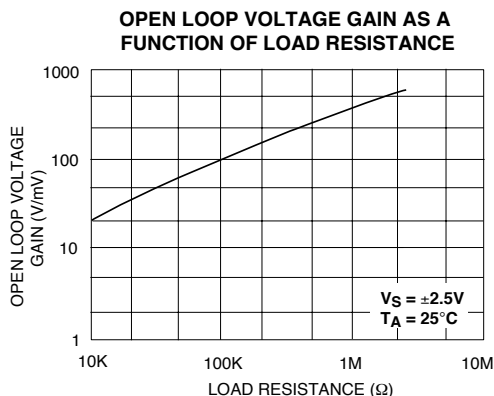
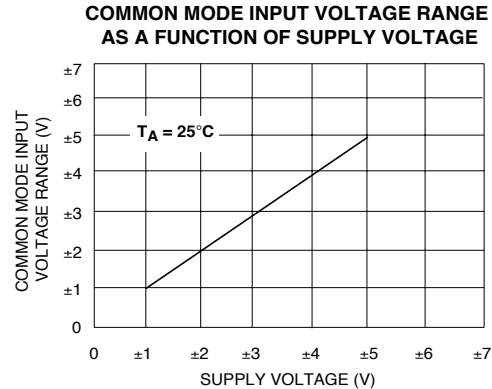
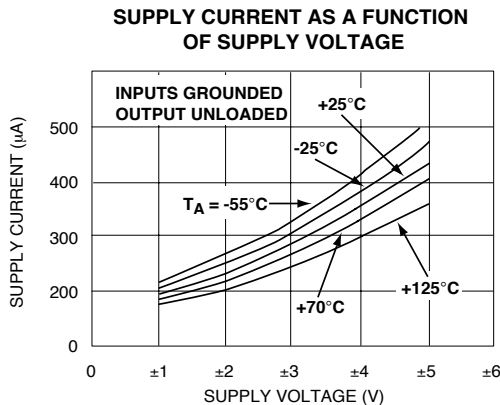
## Design & Operating Notes:

1. The ALD2711A/ALD2711B/ALD2711 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accommodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD2711A/ALD2711B/ALD2711 is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency.
2. The ALD2711A/ALD2711B/ALD2711 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V below the positive supply voltage. Since offset voltage trimming on the ALD2711A/ALD2711B/ALD2711 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions above this switching point. The user should however, be aware that this switching does take place if the operational amplifier is connected as a unity gain buffer and should make provision in his design to allow for input offset voltage variations.
3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA

at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than  $10^{12}\Omega$  would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

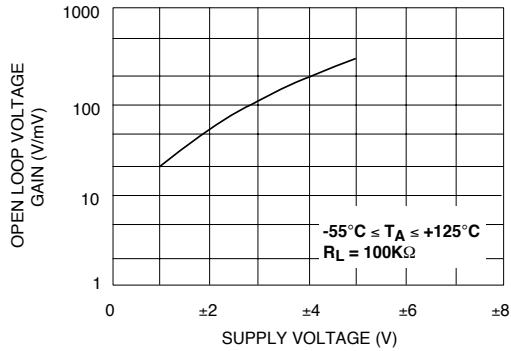
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.
5. The ALD2711A/ALD2711B/ALD2711 operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.
6. The ALD2711A/ALD2711B/ALD2711, with its micropower operation, offers numerous benefits in reduced power supply requirements, less noise coupling and current spikes, less thermally induced drift, better overall reliability due to lower self heating, and lower input bias current. It requires practically no warm up time as the chip junction heats up to only 0.2°C above ambient temperature under most operating conditions.

## TYPICAL PERFORMANCE CHARACTERISTICS

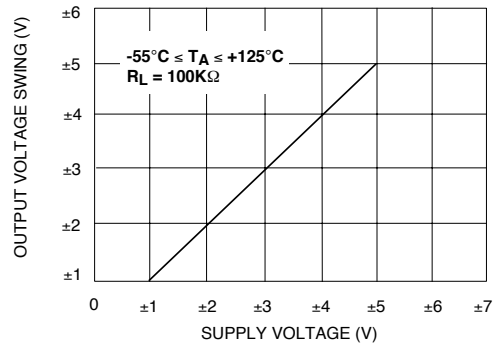


## TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

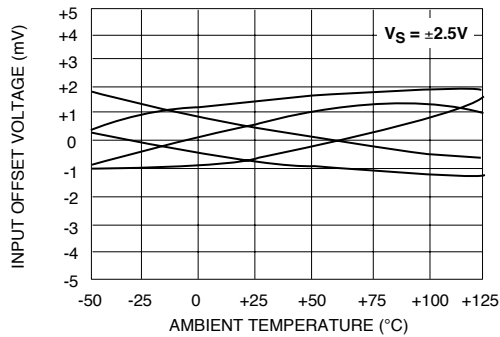
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE**



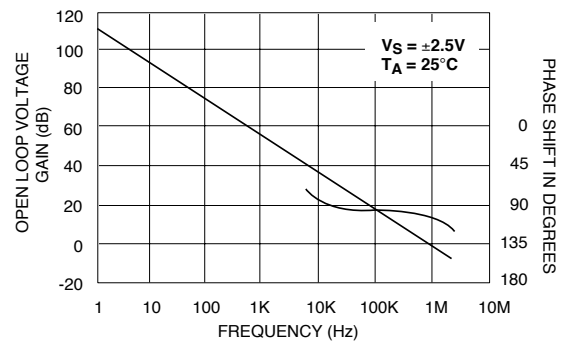
**OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE**



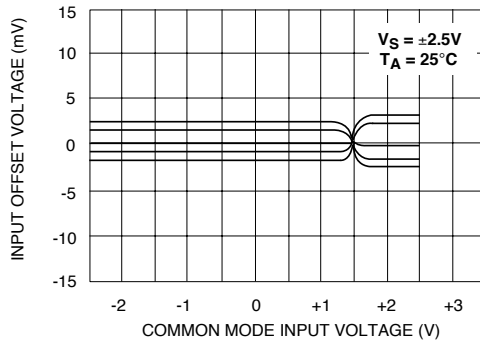
**INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE REPRESENTATIVE UNITS**



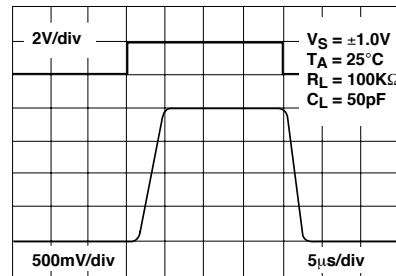
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY**



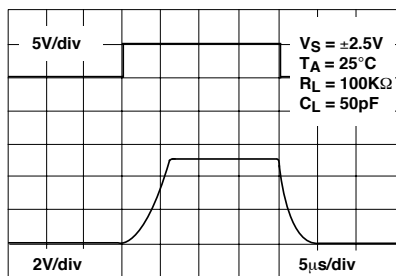
**INPUT OFFSET VOLTAGE AS A FUNCTION OF COMMON MODE INPUT VOLTAGE**



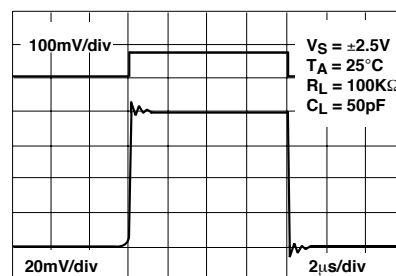
**LARGE - SIGNAL TRANSIENT RESPONSE**



**LARGE - SIGNAL TRANSIENT RESPONSE**

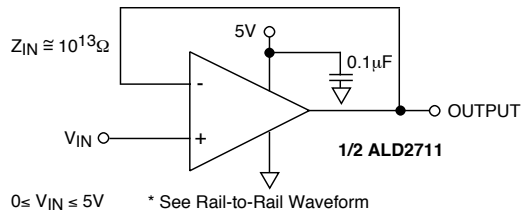


**SMALL - SIGNAL TRANSIENT RESPONSE**

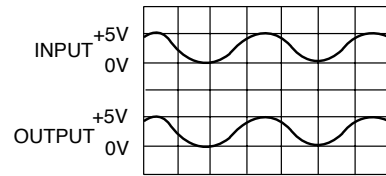


# TYPICAL APPLICATIONS

## RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER

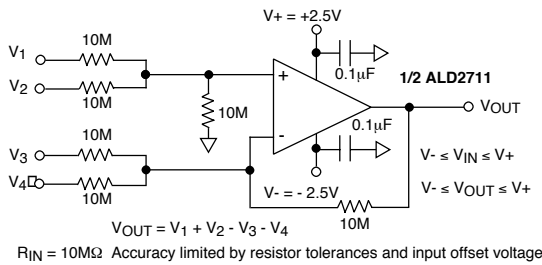


## RAIL-TO-RAIL WAVEFORM

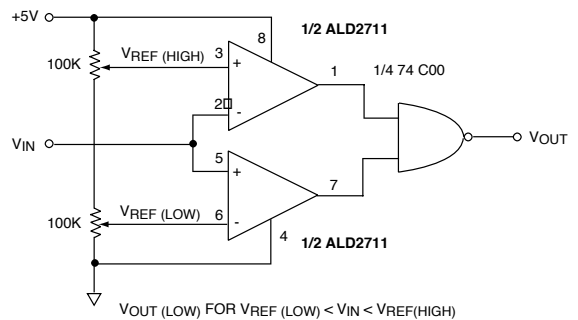


**Performance waveforms.**  
Upper trace is the output of a Wien Bridge Oscillator. Lower trace is the output of Rail-to-Rail voltage follower.

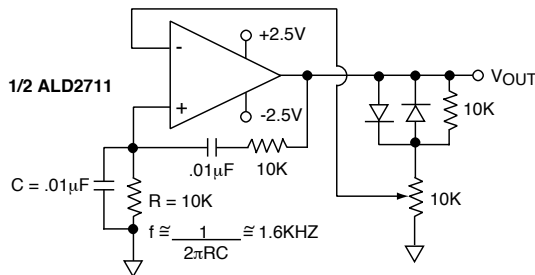
## HIGH INPUT IMPEDANCE RAIL-TO-RAIL PRECISION DC SUMMING AMPLIFIER



## RAIL-TO-RAIL WINDOW COMPARATOR

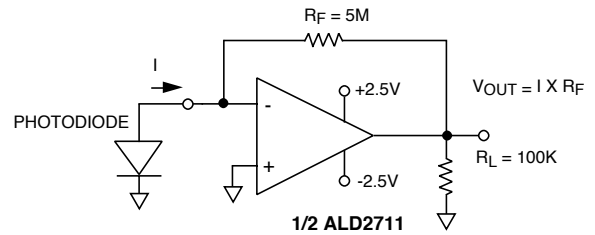


## WIEN BRIDGE OSCILLATOR (RAIL-TO-RAIL) SINE WAVE GENERATOR

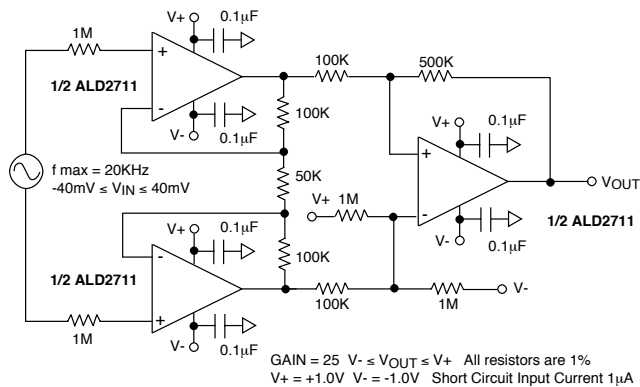


\* See Rail-to-Rail Waveform

## PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER

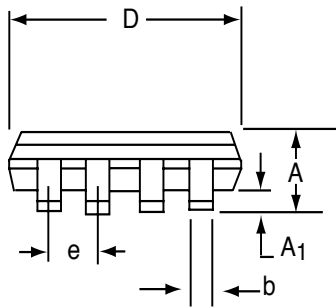
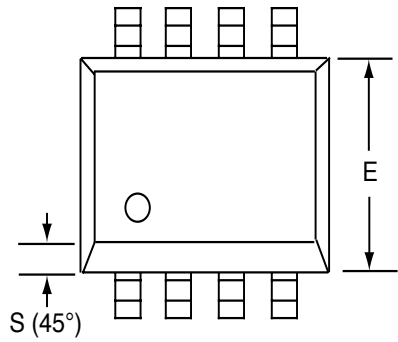


## LOW VOLTAGE INSTRUMENTATION AMPLIFIER



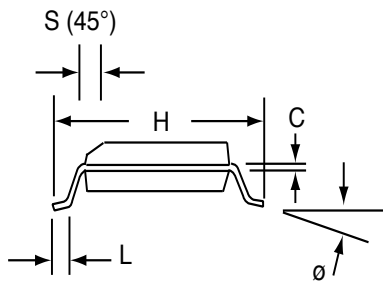
# SOIC-8 PACKAGE DRAWING

## 8 Pin Plastic SOIC Package



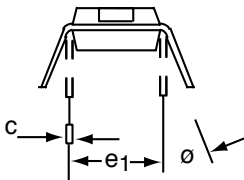
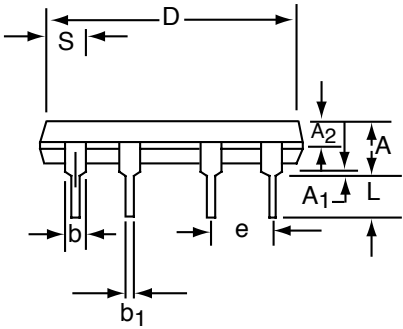
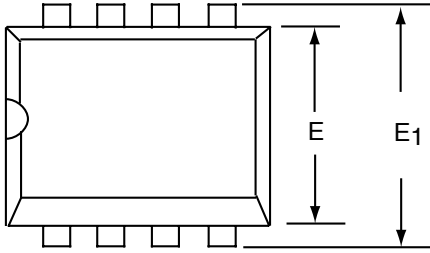
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
∅	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

□



# PDIP-8 PACKAGE DRAWING

## 8 Pin Plastic DIP Package

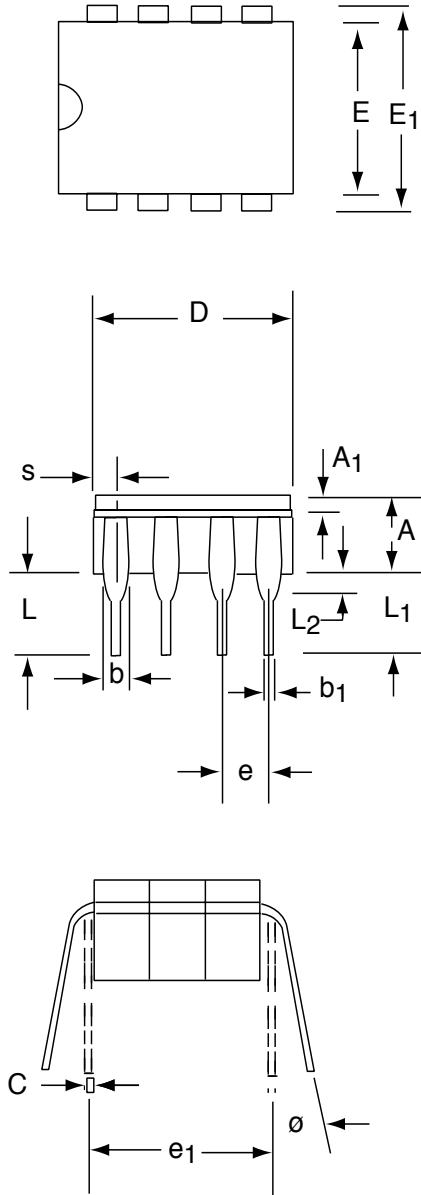


Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A <sub>1</sub>	0.38	1.27	0.015	0.050
A <sub>2</sub>	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b <sub>1</sub>	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E <sub>1</sub>	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e <sub>1</sub>	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
$\theta$	0°	15°	0°	15°



# CERDIP-8 PACKAGE DRAWING

## 8 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	3.55	5.08	0.140	0.200
<b>A<sub>1</sub></b>	1.27	2.16	0.050	0.085
<b>b</b>	0.97	1.65	0.038	0.065
<b>b<sub>1</sub></b>	0.36	0.58	0.014	0.023
<b>C</b>	0.20	0.38	0.008	0.015
<b>D-8</b>	--	10.29	--	0.405
<b>E</b>	5.59	7.87	0.220	0.310
<b>E<sub>1</sub></b>	7.73	8.26	0.290	0.325
<b>e</b>	□2.54 BSC		0.100 BSC	
<b>e<sub>1</sub></b>	□7.62 BSC		0.300 BSC	
<b>L</b>	3.81	5.08	0.150	0.200
<b>L<sub>1</sub></b>	3.18	--	0.125	--
<b>L<sub>2</sub></b>	0.38	1.78	0.015	0.070
<b>S</b>	--	2.49	--	0.098
<b>∅</b>	0°	15°	0°	15°