

# 74HC1GU04

## Single unbuffered inverter

Rev. 7 — 4 February 2022

Product data sheet

## 1. General description

The 74HC1GU04 is a single unbuffered inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- High noise immunity
- Symmetrical output impedance
- CMOS low power dissipation
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JEDEC Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000V
  - MM EIA/JESD22-A115-A exceeds 200V
- Specified from -40 °C to 85 °C and -40 °C to 125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC1GU04GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74HC1GU04GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753

## 4. Marking

Table 2. Marking codes

Type number	Marking <sup>[1]</sup>
74HC1GU04GW	HD
74HC1GU04GV	HU4

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram

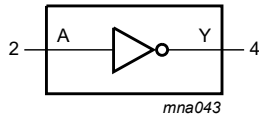


Fig. 1. Logic symbol

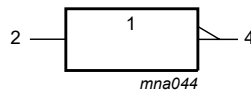


Fig. 2. IEC logic symbol

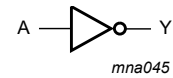


Fig. 3. Logic diagram

## 6. Pinning information

### 6.1. Pinning

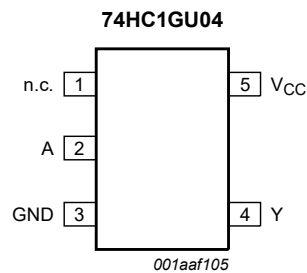


Fig. 4. Pin configuration SOT353-1 (TSSOP5) and SOT753 (SC-74A)

### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V <sub>CC</sub>	5	supply voltage

## 7. Functional description

Table 4. Function table

*H = HIGH voltage level; L = LOW voltage level*

Input	Output
A	Y
L	H
H	L

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 12.5$	mA
$I_{CC}$	supply current		-	25	mA
$I_{GND}$	ground current		-25	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.  
For SOT753 (SC-74A) package:  $P_{tot}$  derates linearly with 3.8 mW/K above 85 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}$	-	-	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V). All typical values are measured at  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.7	1.4	-	1.7	-	V
		$V_{CC} = 4.5\text{ V}$	3.6	2.6	-	3.6	-	V
		$V_{CC} = 6.0\text{ V}$	4.8	3.4	-	4.8	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.6	0.3	-	0.3	V
		$V_{CC} = 4.5\text{ V}$	-	1.9	0.9	-	0.9	V
		$V_{CC} = 6.0\text{ V}$	-	2.6	1.2	-	1.2	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.0	4.5	-	4.0	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.5	6.0	-	5.5	-	V
		I <sub>O</sub> = -2.0 mA; V <sub>CC</sub> = 4.5 V	4.13	4.32	-	3.7	-	V
		I <sub>O</sub> = -2.6 mA; V <sub>CC</sub> = 6.0 V	5.63	5.81	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.5	-	0.5	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.5	-	0.5	V
		I <sub>O</sub> = 2.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.33	-	0.4	V
		I <sub>O</sub> = 2.6 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	1.0	-	1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	10	-	20	μA
C <sub>I</sub>	input capacitance		-	5	-	-	-	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6.0 ns; For test circuit see Fig. 6. All typical values are measured at T<sub>amb</sub> = 25 °C.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
t <sub>pd</sub>	propagation delay	A to Y; see Fig. 5 [1]						
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF	-	10	90	-	105	ns
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF	-	7	18	-	21	ns
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF	-	6	15	-	18	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	5	-	-	-	ns
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> [2]	-	14	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[2] C<sub>PD</sub> is used to determine the dynamic power dissipation P<sub>D</sub> (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in Volts.

11.1. Waveform and test circuit

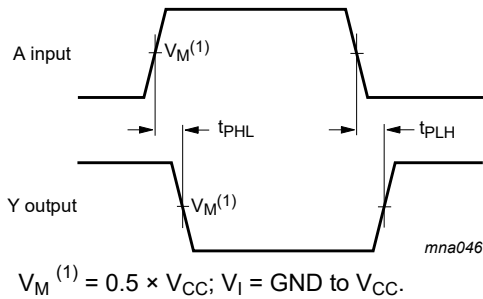


Fig. 5. Input to output propagation delays

$V_M^{(1)} = 0.5 \times V_{CC}$ ;  $V_I = \text{GND to } V_{CC}$ .

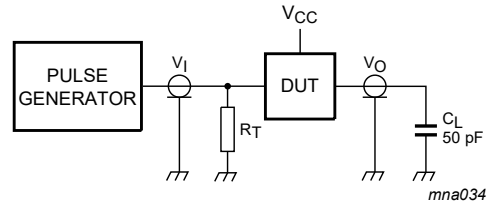


Fig. 6. Test circuit for measuring switching times

Test data is given in [Table 8](#).

DUT = Device Under Test

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

11.2. Additional characteristics

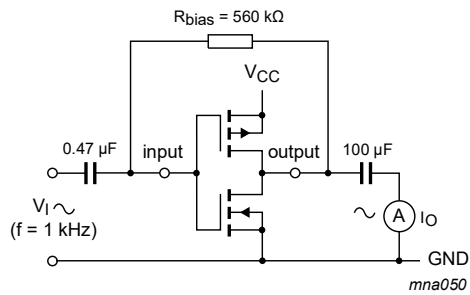


Fig. 7. Test set-up for measuring forward transconductance

$g_{fs} = \Delta I_O / \Delta V_I$  at  $V_O$  is constant.

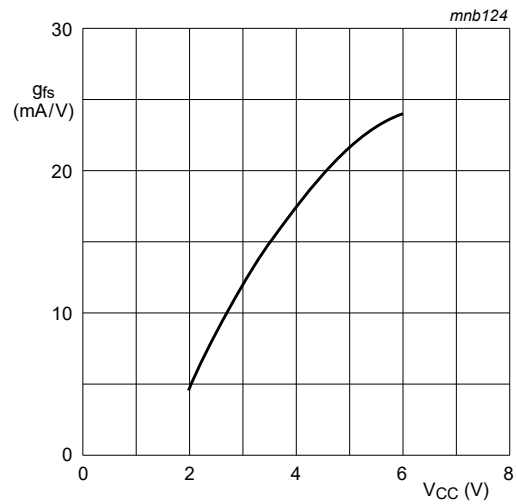
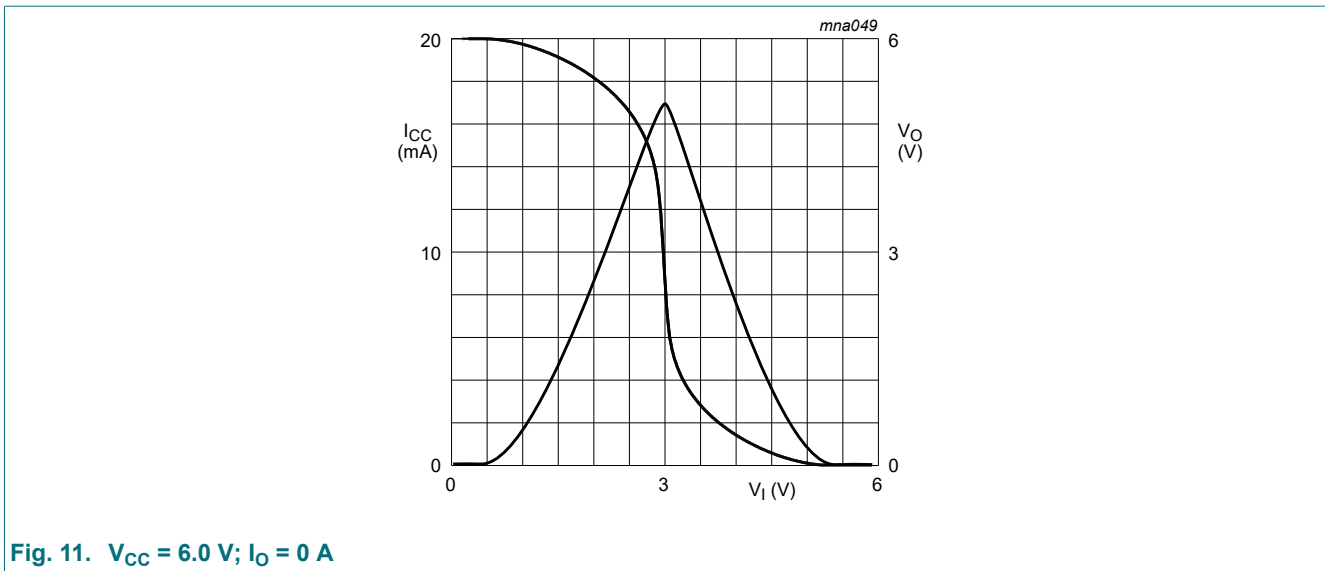
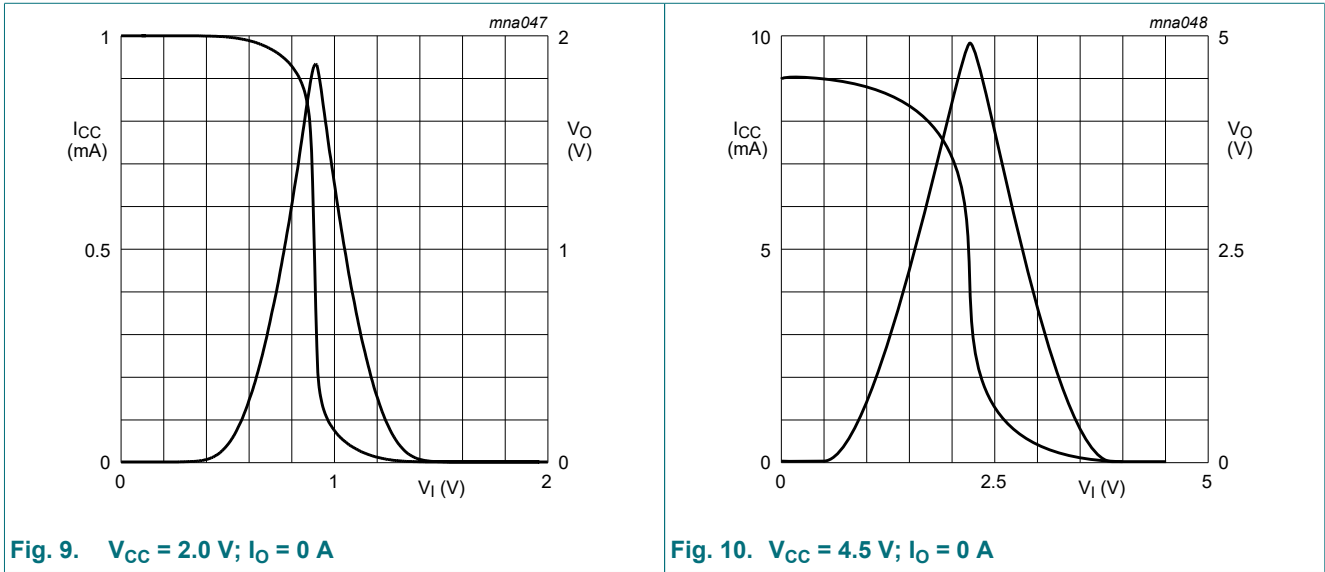


Fig. 8. Typical forward transconductance as a function of supply voltage

$T_{amb} = 25 \text{ }^\circ\text{C}$

11.3. Typical transfer characteristics

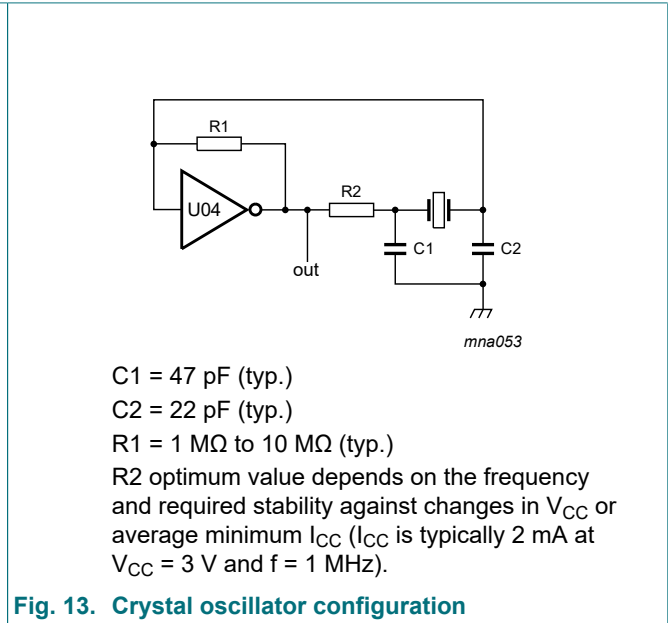
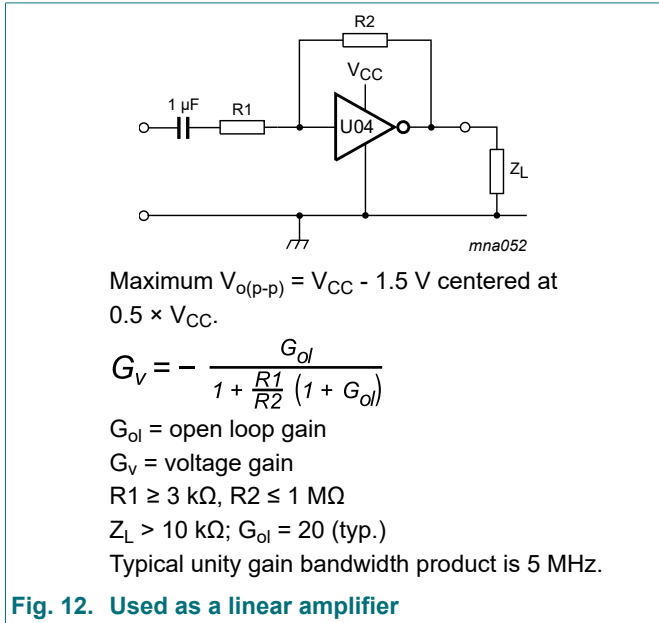


## 12. Application information

Some applications are:

- Linear amplifier (see Fig. 12)
- In crystal oscillator design (see Fig. 13)

**Remark:** All values given are typical unless otherwise specified.



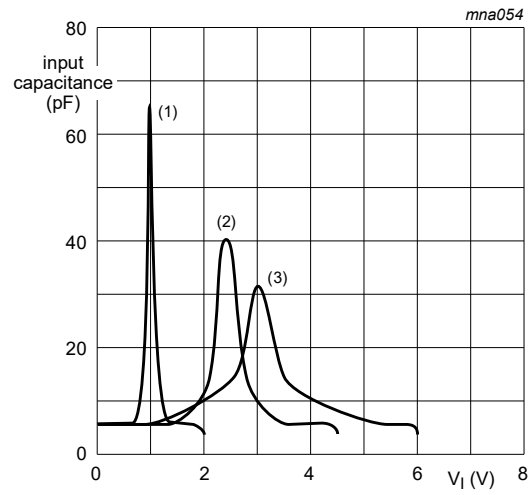
**Table 9. External components for resonator (f < 1 MHz)**

All values given are typical and must be used as an initial set-up

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	2.2 MΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	2.2 MΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	2.2 MΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	2.2 MΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	2.2 MΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	2.2 MΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	2.2 MΩ	47 kΩ	47 pF	5 pF

**Table 10. Optimum value for R2**

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required $I_{CC}$
	8.0 kΩ	minimum influence due to change in $V_{CC}$
6 kHz	1.0 kΩ	minimum required $I_{CC}$
	4.7 kΩ	minimum influence by $V_{CC}$
10 kHz	0.5 kΩ	minimum required $I_{CC}$
	2.0 kΩ	minimum influence by $V_{CC}$
14 kHz	0.5 kΩ	minimum required $I_{CC}$
	1.0 kΩ	minimum influence by $V_{CC}$
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF



(1)  $V_{CC} = 2.0$  V

(2)  $V_{CC} = 4.5$  V

(3)  $V_{CC} = 6.0$  V

**Fig. 14. Typical input capacitance as a function of the input voltage**



### 13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig. 15. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

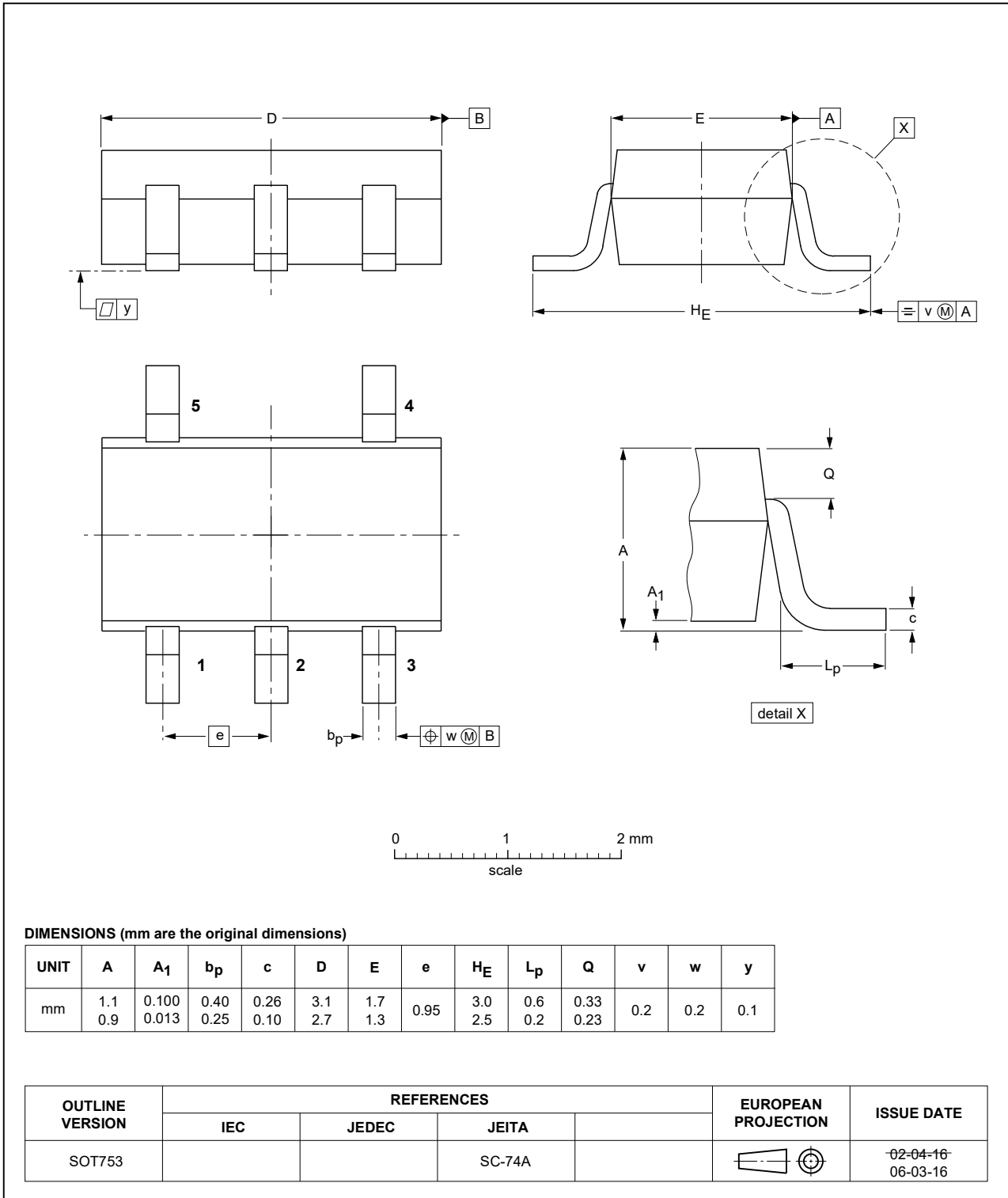


Fig. 16. Package outline SOT753 (SC-74A)

## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
MM	Machine Model

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC1GU04 v.7	20220204	Product data sheet	-	74HC1GU04 v.6
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li>• <a href="#">Fig. 15</a>: Package outline drawing SOT353-1 (TSSOP5) has changed.</li> </ul>			
74HC1GU04 v.6	20180725	Product data sheet	-	74HC1GU04 v.5
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Fig. 8</a>: forward transconductance graph added.</li> </ul>			
74HC1GU04 v.5	20070710	Product data sheet	-	74HC1GU04 v.4
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Package SOT353 changed to SOT353-1 in <a href="#">Table 1</a> and <a href="#">Fig. 15</a>.</li> <li>• Quick Reference Data and Soldering sections removed.</li> <li>• <a href="#">Section 2</a> updated.</li> </ul>			
74HC1GU04 v.4	20020527	Product specification	-	74HC1GU04 v.3
74HC1GU04 v.3	20020513	Product specification	-	74HC1GU04 v.2
74HC1GU04 v.2	20010427	Product specification	-	74HC1GU04 v.1
74HC1GU04 v.1	19981118	Product specification	-	-

## 16. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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