

Low-Power, High-Speed CMOS Analog Switches

DESCRIPTION

The DG401, DG403, DG405 monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (0.35 μ W, typ.) with high speed (t_{ON} : 75 ns, typ.), the DG401 series is ideally suited for portable and battery powered industrial and military applications.

Built on the Vishay Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full ± 15 V analog range, rivaling JFET performance without the inherent dynamic range limitations.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams.

FEATURES

- 44 V supply max. rating
- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 30 Ω
- Low leakage - $I_{D(on)}$: 40 pA
- Fast switching - t_{ON} : 75 ns
- Ultra low power requirements - P_D : 0.35 μ W
- TTL, CMOS compatible
- Single supply capability
- **Compliant to RoHS directive 2002/95/EC**



RoHS*
COMPLIANT

BENEFITS

- Wide dynamic range
- Break-before-make switching action
- Simple interfacing

APPLICATIONS

- Audio and video switching
- Sample-and-hold circuits
- Battery operation
- Test equipment
- Communications systems
- PBX, PABX

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



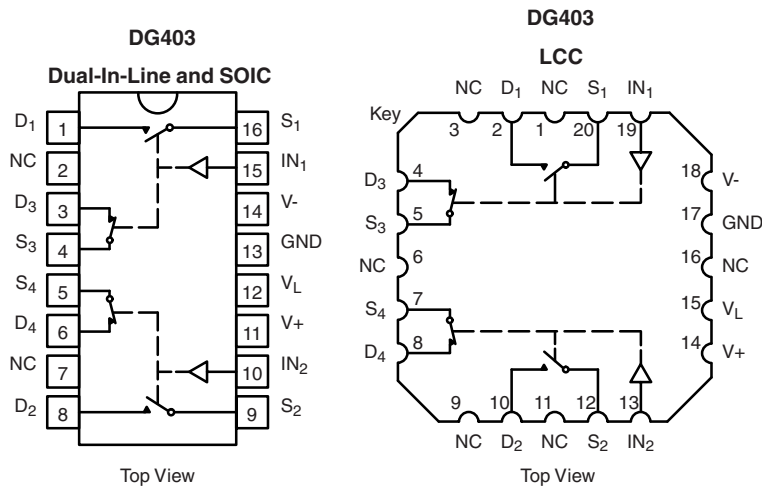
Two SPST Switches per Package

| TRUTH TABLE | |
|-------------|--------|
| Logic | Switch |
| 0 | OFF |
| 1 | ON |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply

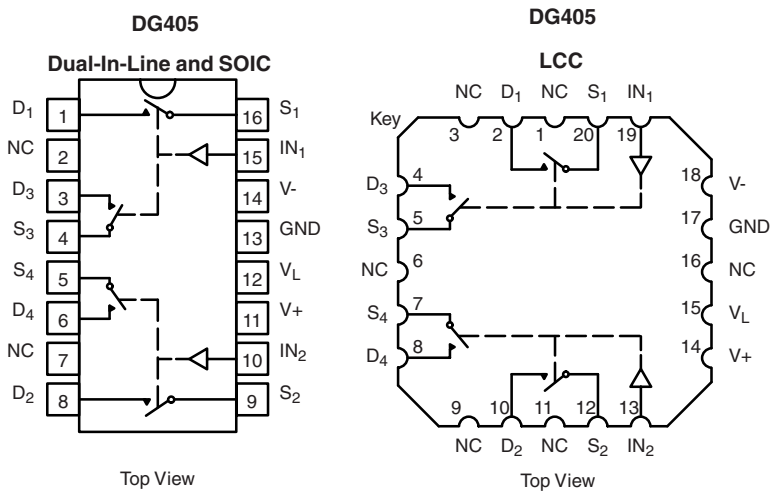
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Two SPDT Switches per Package

| TRUTH TABLE | | |
|-------------|-----------------------------------|-----------------------------------|
| Logic | SW ₁ , SW ₂ | SW ₃ , SW ₄ |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V



Two DPST Switches per Package

| TRUTH TABLE | |
|-------------|--------|
| Logic | Switch |
| 0 | OFF |
| 1 | ON |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V



| ORDERING INFORMATION | | |
|-----------------------------|--------------------|--|
| Temp. Range | Package | Part Number |
| DG401 | | |
| - 40 °C to 85 °C | 16-Pin Plastic DIP | DG401DJ DG401DJ-E3 |
| | 16-Pin Narrow SOIC | DG401DY DG401DY-T1 DG401DY-E3 DG401DY-T1-E3 |
| DG403 | | |
| - 40 °C to 85 °C | 16-Pin Plastic DIP | DG403DJ DG403DJ-E3 |
| | 16-Pin Narrow SOIC | DG403DY DG403DY-E3 DG403DY-T1 DG403DY-T1-E3 |
| DG405 | | |
| - 40 °C to 85 °C | 16-Pin Plastic DIP | DG405DJ DG405DJ-E3 |
| | 16-Pin Narrow SOIC | DG405DY DG405DY-E3 DG405DY-T1 DG405DY-T1-E3 |

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|--|------|----|
| Parameter | Limit | Unit | |
| V+ to V- | 44 | V | |
| GND to V- | 25 | | |
| V _L | (GND - 0.3) to (V+) + 0.3 | | |
| Digital Inputs ^a , V _S , V _D | (V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first | | |
| Current (Any Terminal) Continuous | 30 | mA | |
| Current, S or D (Pulsed 1 ms, 10 % Duty) | 100 | | |
| Storage Temperature | (DJ, DY Suffix) - 65 to 125 | °C | |
| Power Dissipation (Package) ^b | 16-Pin Plastic DIP ^c | 450 | mW |
| | 16-Pin SOIC ^d | 600 | |

Notes:

- Signals on S_x, D_x, or IN_x exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC board.
- Derate 6 mW/°C above 75 °C.
- Derate 7.6 mW/°C above 75 °C.

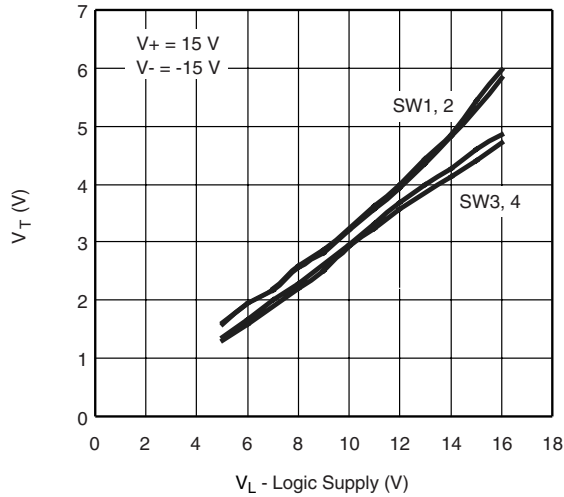
| SPECIFICATIONS ^a | | | | | | | |
|--------------------------------------|-------------------------------------|--|--------------------|-------------------|------------------------------|-------------------|------|
| Parameter | Symbol | Test Conditions Unless Specified V ₊ = 15 V, V ₋ = - 15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f | Temp. ^b | Typ. ^c | D Suffix - 40 °C to 85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | |
| Analog Signal Range ^e | V _{ANALOG} | | Full | | - 15 | 15 | V |
| Drain-Source On-Resistance | R _{DS(on)} | I _S = - 10 mA, V _D = ± 10 V V ₊ = 13.5 V, V ₋ = - 13.5 V | Room Full | 30 | | 45 55 | Ω |
| Δ Drain-Source On-Resistance | ΔR _{DS(on)} | I _S = - 10 mA, V _D = ± 5 V, 0 V V ₊ = 16.5 V, V ₋ = - 16.5 V | Room Full | 3 | | 3 5 | |
| Switch Off Leakage Current | I _{S(off)} | V ₊ = 16.5 V, V ₋ = - 16.5 V V _D = ± 15.5 V, V _S = ± 15.5 V | Room Hot | - 0.01 | - 0.5 - 5 | 0.5 5 | nA |
| | I _{D(off)} | | Room Hot | - 0.01 | - 0.5 - 5 | 0.5 5 | |
| Channel On Leakage Current | I _{D(on)} | V ₊ = 16.5 V, V ₋ = - 16.5 V V _S = V _D = ± 15.5 V | Room Hot | - 0.04 | - 1 - 10 | 1 10 | |
| Digital Control | | | | | | | |
| Input Current V _{IN} Low | I _{IL} | V _{IN} under test = 0.8 V All Other = 2.4 V | Full | 0.005 | - 1 | 1 | μA |
| Input Current V _{IN} High | I _{IH} | V _{IN} under test = 2.4 V All Other = 0.8 V | Full | 0.005 | - 1 | 1 | |
| Dynamic Characteristics | | | | | | | |
| Turn-On Time | t _{ON} | R _L = 300 Ω, C _L = 35 pF See Figure 2 | Room | 75 | | 150 | ns |
| Turn-Off Time | t _{OFF} | | Room | 30 | | 100 | |
| Break-Before-Make Time Delay (DG403) | t _D | R _L = 300 Ω, C _L = 35 pF | Room | 35 | 5 | | |
| Charge Injection | Q | C _L = 10 nF V _{gen} = 0 V, R _{gen} = 0 Ω | Room | 60 | | | pC |
| Off Isolation Reject Ratio | OIRR | R _L = 100 Ω, C _L = 5 pF f = 1 MHz | Room | 72 | | | dB |
| Channel-to-Channel Crosstalk | X _{TALK} | | Room | 90 | | | |
| Source Off Capacitance | C _{S(off)} | f = 1 MHz, V _S = 0 V | Room | 12 | | | pF |
| Drain Off Capacitance | C _{D(off)} | | Room | 12 | | | |
| Channel On Capacitance | C _D , C _{S(on)} | | Room | 39 | | | |
| Power Supplies | | | | | | | |
| Positive Supply Current | I ₊ | V ₊ = 16.5 V, V ₋ = - 16.5 V V _{IN} = 0 or 5 V | Room Full | 0.01 | | 1 5 | μA |
| Negative Supply Current | I ₋ | | Room Full | - 0.01 | - 1 - 5 | | |
| Logic Supply Current | I _L | | Room Full | 0.01 | | 1 5 | |
| Ground Current | I _{GND} | | Room Full | - 0.01 | - 1 - 5 | | |

Notes:

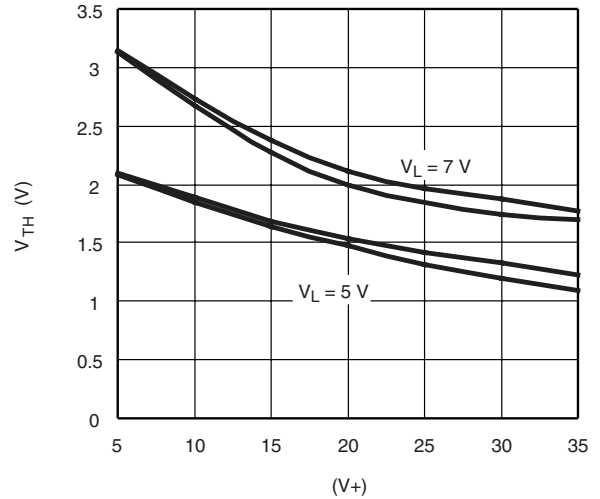
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

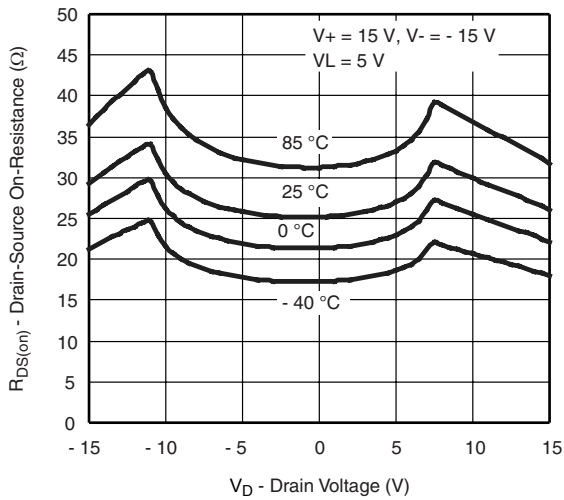
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



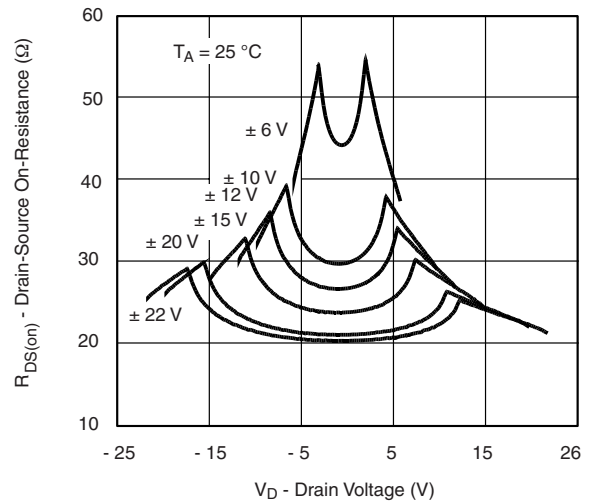
Input Switching Threshold vs. Logic Supply Voltage



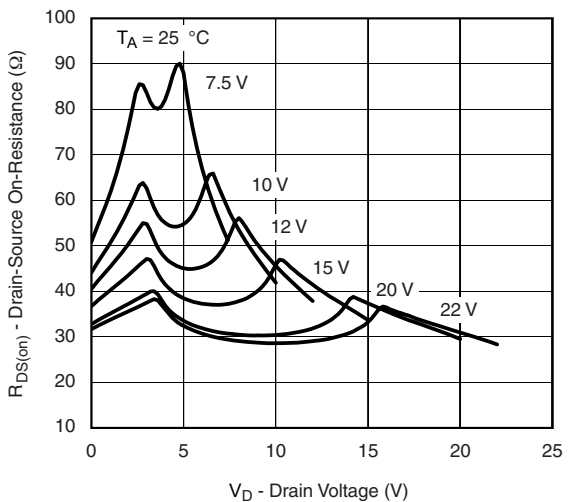
Input Switching Threshold vs. Supply Voltages



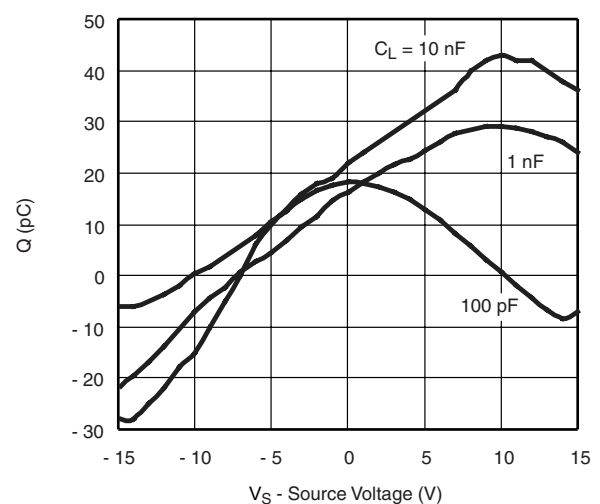
$R_{DS(on)}$ vs. V_D and Temperature



$R_{DS(on)}$ vs. V_D and Power Supply Voltage

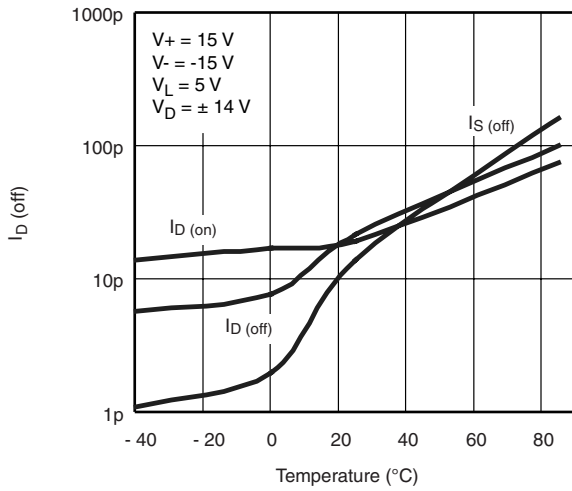


$R_{DS(on)}$ vs. V_D and Power Supply Voltage ($V_- = 0$ V)

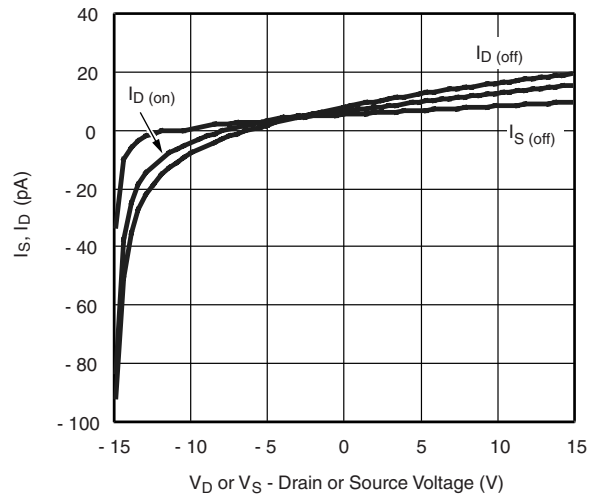


Charge Injection vs. Analog Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Leakage Current vs. Temperature



Leakage Current vs. Analog Voltage



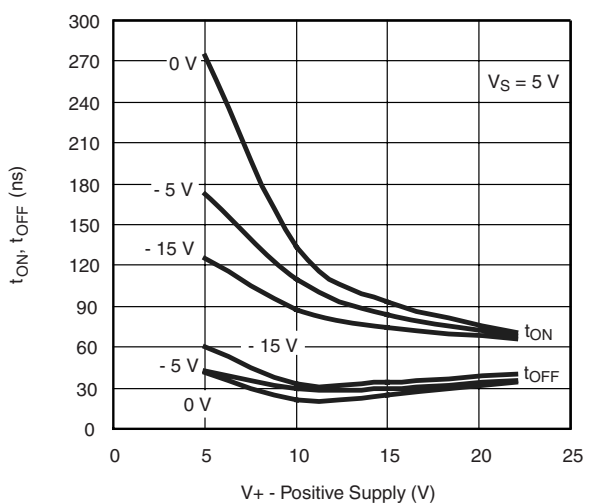
Supply Current vs. Temperature



Switching Time vs. Temperature*



Switching Time vs. Power Supply Voltage*



Switching Time vs. Positive Supply Voltage*

* Refer to Figure 2 for test conditions.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Supply Current vs. Switching Frequency

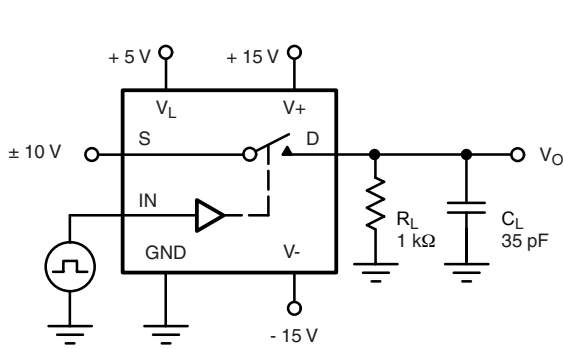
SCHEMATIC DIAGRAM Typical Channel



Figure 1.

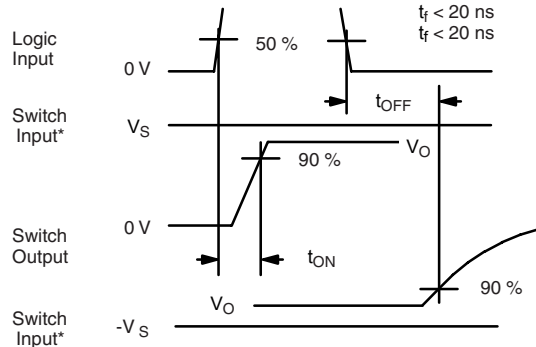
TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



* $V_S = 10\text{ V}$ for t_{ON} , $V_S = -10\text{ V}$ for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time



C_L (includes fixture and stray capacitance)

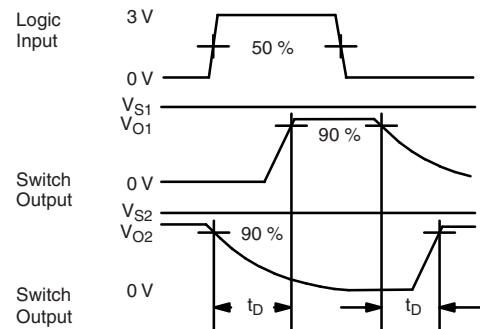


Figure 3. Break-Before-Make

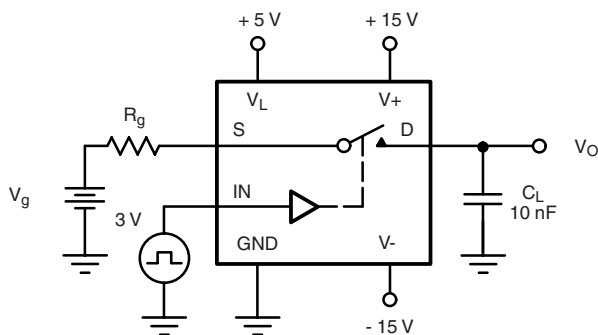


Figure 4. Charge Injection

TEST CIRCUITS



Figure 5. Off Isolation



Figure 7. Crosstalk



Figure 6. Insertion Loss

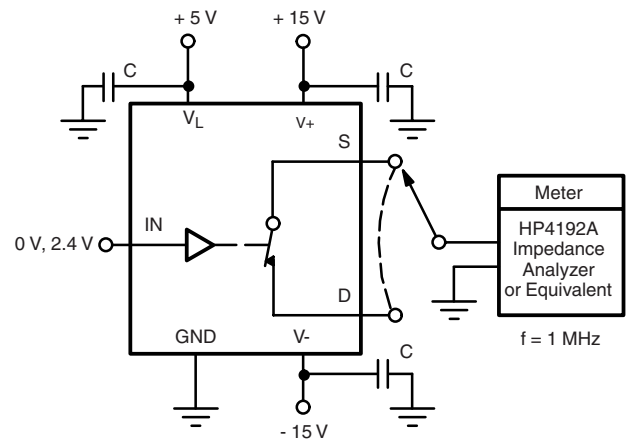


Figure 8. Capacitances

APPLICATIONS

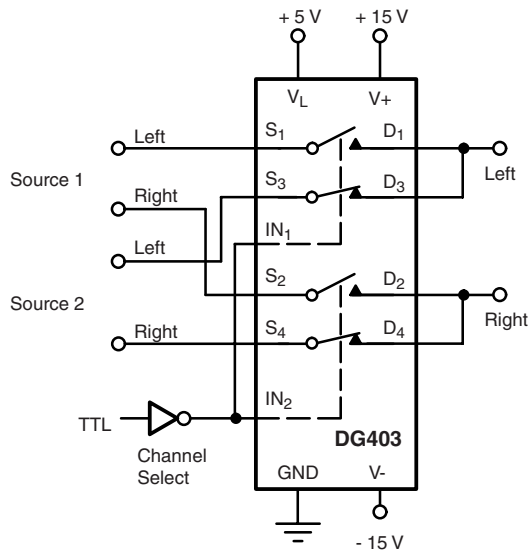


Figure 9. Stereo Source Selector

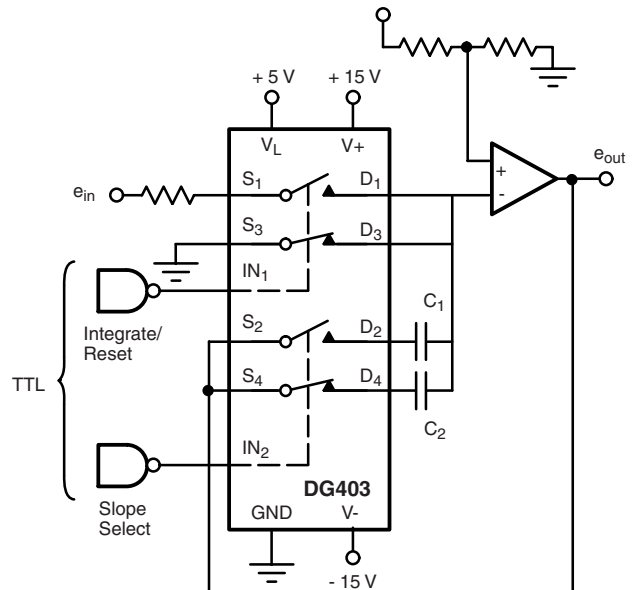


Figure 10. Dual Slope Integrator

Dual Slope Integrators:

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2 . Another one selects e_{in} or discharges the capacitor in preparation for the next integration cycle.

Band-Pass Switched Capacitor Filter:

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.



Figure 11. Band-Pass Switched Capacitor Filter

APPLICATIONS
Peak Detector:

A_3 acting as a comparator provides the logic drive for operating SW_1 . The output of A_2 is fed back to A_3 and compared to the analog input e_{in} . If $e_{in} > e_{out}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to

the analog input voltage. When e_{in} goes below e_{out} A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.



Figure 12. Positive Peak Detector

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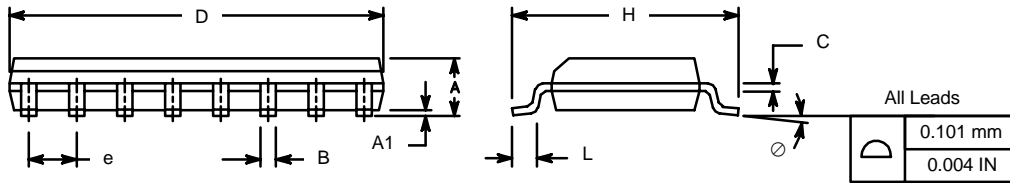


SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012



| Dim | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A ₁ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| C | 0.18 | 0.23 | 0.007 | 0.009 |
| D | 9.80 | 10.00 | 0.385 | 0.393 |
| E | 3.80 | 4.00 | 0.149 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| ∅ | 0° | 8° | 0° | 8° |

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



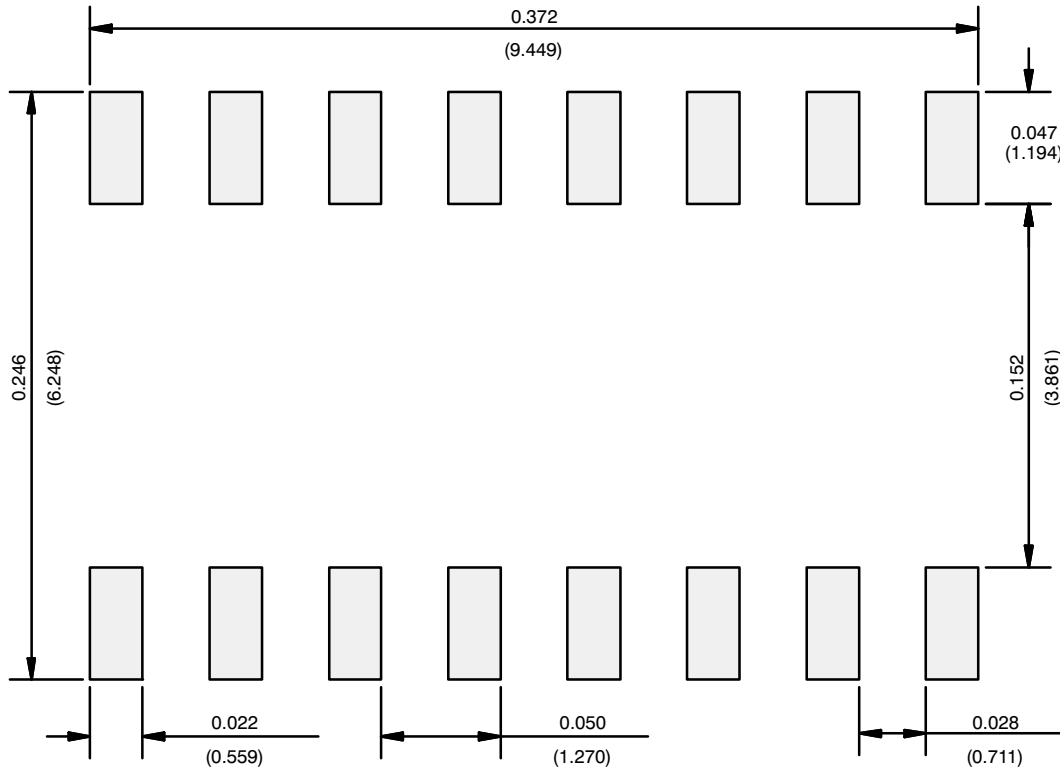
PDIP: 16-LEAD



| Dim | MILLIMETERS | | INCHES | |
|----------------------|-------------|-------|--------|-------|
| | Min | Max | Min | Max |
| A | 3.81 | 5.08 | 0.150 | 0.200 |
| A₁ | 0.38 | 1.27 | 0.015 | 0.050 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| B₁ | 0.89 | 1.65 | 0.035 | 0.065 |
| C | 0.20 | 0.30 | 0.008 | 0.012 |
| D | 18.93 | 21.33 | 0.745 | 0.840 |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E₁ | 5.59 | 7.11 | 0.220 | 0.280 |
| e₁ | 2.29 | 2.79 | 0.090 | 0.110 |
| e_A | 7.37 | 7.87 | 0.290 | 0.310 |
| L | 2.79 | 3.81 | 0.110 | 0.150 |
| Q₁ | 1.27 | 2.03 | 0.050 | 0.080 |
| S | 0.38 | 1.52 | .015 | 0.060 |

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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