Motor Control, Current Measurement 1-Bit, 10MHz, 2nd-Order, Delta-Sigma Modulator

FEATURES

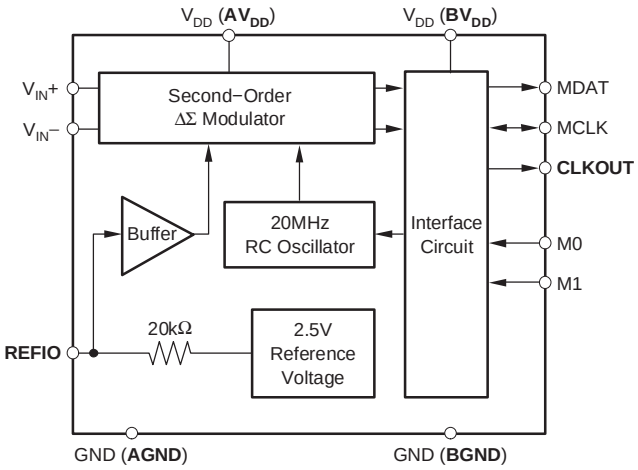
- **16-Bit Resolution**
- **14-Bit Linearity**
- **±250mV Input Range with Single +5V Supply**
- **1% Internal Reference Voltage**
- **1% Gain Error**
- **Flexible Serial Interface with Four Different Modes**
- **Implemented Twinned Binary Coding as Split-Phase or Manchester Coding for One-Line Interfacing**
- **Operating Temperature Range: −40°C to +125°C**

APPLICATIONS

- **Motor Control**
- **Current Measurement**
- **Industrial Process Control**
- **Instrumentation**
- **Smart Transmitters**

DESCRIPTION

The ADS1203 is a delta-sigma (ΔΣ) modulator with a 95dB dynamic range, operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low-level signals. With the appropriate digital filter and modulator rate, the device can be used to achieve 16-bit analog-to-digital (A/D) conversion with no missing codes. An effective resolution of 14 bits or SNR of 85dB (typical) can be maintained with a digital filter bandwidth of 40kHz at a modulator rate of 10MHz. The ADS1203 is designed for use in medium- to high-resolution measurement applications including current measurements, smart transmitters, and industrial process control. The ADS1203 is available in TSSOP-8 and QFN-16 (3x3) packages.



NOTE: **BOLD** pins are available only in QFN package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted

	ADS1203	UNIT
Supply Voltage, AV_{DD} to AGND or V_{DD} to GND	−0.3 to 6	V
Supply Voltage, BV_{DD} to BGND	−0.3 to 6	V
Analog Input Voltage with Respect to AGND or GND	AGND − 0.3 to AV_{DD} + 0.3	V
Reference Input Voltage with Respect to AGND	AGND − 0.3 to AV_{DD} + 0.3	V
Digital Input Voltage with Respect to BGND or GND	BGND − 0.3 to BV_{DD} + 0.3	V
Ground Voltage Difference, AGND to BGND	±0.3	V
Voltage Differences, BV_{DD} to AGND	−0.3 to 6	V
Input Current to Any Pin Except Supply	±10	mA
Power Dissipation	See Dissipation Rating Table	
Operating Virtual Junction Temperature Range, T_J	−40 to +150	°C
Operating Free-Air Temperature Range, T_A	−40 to +125	°C
Storage Temperature Range, T_{STG}	−65 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply Voltage, AV_{DD} to AGND or V_{DD} to GND		4.5	5	5.5	V
Supply Voltage, BV_{DD} to BGND	Low-Voltage Levels	2.7		3.6	V
	5V Logic Levels	4.5	5	5.5	V
Reference Input Voltage		0.5	2.5	2.6	V
Operating Common-Mode Signal		0		5	V
Analog Inputs	$V_{IN}+ - V_{IN}-$ (TSSOP package)	−250		+250	mV
	$V_{IN}+ - V_{IN}-$ (QFN package)	−0.1 × REFIO		+0.1 × REFIO	V
External Clock(1)		16	20	24	MHz
Operating Junction Temperature Range, T_J		−40		+150	°C

(1) With reduced accuracy, clock can go from 1MHz up to 32MHz; see Typical Characteristic curves.

DISSIPATION RATINGS

PACKAGE	$T_A \le +25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = +25°C$(1)	$T_A = +70°C$ POWER RATING	$T_A = +85°C$ POWER RATING	$T_A = +125°C$ POWER RATING
TSSOP-8	532mW	4.3mW/°C	338mW	274mW	102mW
QFN-16	2540mW	20.4mW/°C	1622mW	1316mW	500mW

(1) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$). Thermal resistances are not production tested and are for informational purposes only.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at −40°C to +125°C, AV_{DD} = BV_{DD} = +5V or V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, Mode 3, MCLK input = 20MHz, and 16-bit $Sinc^3$ filter, with OSR = 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1203I			UNITS
			MIN	TYP(1)	MAX	
Resolution			16			Bits
DC Accuracy						
INL	Integral linearity error(2)			±1	±4	LSB
		T_A = −40°C to +85°C			±3	LSB
DNL	Differential nonlinearity(3)				±1	LSB
V_{OS}	Input offset(4)			±220	±1000	µV
TCV_{OS}	Input offset drift			±3.5	±8	µV/°C
G_{ERR}	Gain error(4)	REFIO = internal 2.5V		±0.2	±1.4	%
		REFIO = internal 2.5V, T_A = −40°C to +85°C	−1		1	%
TCG_{ERR}	Gain error drift			±30		ppm/°C
		T_A = −40°C to +85°C		±20		ppm/°C
PSRR	Power-supply rejection ratio	4.5V < AV_{DD} or V_{DD} < 5.5V		80		dB
Analog Input						
FSR	Full-scale differential range	(V_{IN}+) − (V_{IN}−)			±320	mV
	Operating common-mode signal(3)		−0.1		5	V
	Input capacitance	Common-mode		3		pF
	Input leakage current				±16	nA
		T_A = −40°C to +85°C			±1	nA
	Differential input resistance	Equivalent		28		kΩ
	Differential input capacitance			5		pF
CMRR	Common-mode rejection ratio	At DC		92		dB
		V_{IN} = 0V to 5V at 50kHz		105		dB
Internal Clock for Modes 0, 1, and 2						
	Clock frequency		8.7	10	11	MHz
		T_A = −40°C to +85°C	9		11	MHz
External Clock for Mode 3						
	Clock frequency(5)		16	20	24	MHz

(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for V_{IN}+ = −250mV to +250mV, expressed either as the number of LSBs or as a percent of measured input range (500mV).
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(5) With reduced accuracy, the supported external clock frequency range is 1MHz up to 32MHz.
(6) Available only for QFN package.
(7) Applicable for 5.0V nominal supply: BV_{DD} = 4.5V to 5.5V.
(8) Applicable for 3.0V nominal supply: BV_{DD} = 2.7V to 3.6V.
(9) Measured with CLKOUT pin not loaded.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating free-air temperature range at −40°C to +125°C, AV_{DD} = BV_{DD} = +5V or V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, Mode 3, MCLK input = 20MHz, and 16-bit $Sinc^3$ filter, with OSR = 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1203I MIN	ADS1203I TYP(1)	ADS1203I MAX	UNITS
AC Accuracy						
SINAD	Signal-to-noise + distortion	V_{IN} = ±250mV$_{PP}$ at 5kHz	81	85		dB
		V_{IN} = ±250mV$_{PP}$ at 5kHz, T_A = −40°C to +85°C	82.5			dB
SNR	Signal-to-noise ratio	V_{IN} = ±250mV$_{PP}$ at 5kHz	81.5	85		dB
		V_{IN} = ±250mV$_{PP}$ at 5kHz, T_A = −40°C to +85°C	83			dB
THD	Total harmonic distortion	V_{IN} = ±250mV$_{PP}$ at 5kHz		−95	−87	dB
		V_{IN} = ±250mV$_{PP}$ at 5kHz, T_A = −40°C to +85°C			−88	dB
SFDR	Spurious-free dynamic range	V_{IN} = ±250mV$_{PP}$ at 5kHz	88	95		dB
		V_{IN} = ±250mV$_{PP}$ at 5kHz, T_A = −40°C to +85°C	90			dB
Voltage Reference Output(6)						
V_{OUT}	Reference voltage output		2.440	2.5	2.560	V
dV_{OUT}/dT	Reference voltage temperature drift			±30		ppm/°C
		T_A = −40°C to +85°C		±20		ppm/°C
	Output voltage noise	f = 0.1Hz to 10Hz, C_L = 10µF		10		µVrms
		f =10Hz to 10kHz, C_L = 10µF		12		µVrms
PSRR	Power-supply rejection ratio			60		dB
I_{OUT}	Output current			10		µA
I_{SC}	Short-circuit current			0.5		mA
	Turn-on settling time	To 0.1% at C_L = 0		100		µs
Voltage Reference Input(6)						
V_{IN}	Reference voltage input		0.5	2.5	2.6	V
	Reference input resistance			20		kΩ
	Reference input capacitance			5		pF
	Reference input current				1	µA
Digital Inputs(7)						
	Logic family		CMOS with Schmitt Trigger			
V_{IH}	High-level input voltage		0.7×BV_{DD}		BV_{DD}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.3×BV_{DD}	V
I_{IN}	Input current	V_{IN} = BV_{DD} or GND			±50	nA
C_I	Input capacitance			5		pF
Digital Outputs(7)						
	Logic family			CMOS		
V_{OH}	High-level output voltage	BV_{DD} = 4.5V, I_{OH} = −100µA	4.44			V
V_{OL}	Low-level output voltage	BV_{DD} = 4.5V, I_{OL} = +100µA			0.5	V
C_L	Load capacitance				30	pF
	Data format			Bit Stream		

(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for V_{IN}+ = −250mV to +250mV, expressed either as the number of LSBs or as a percent of measured input range (500mV).
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(5) With reduced accuracy, the supported external clock frequency range is 1MHz up to 32MHz.
(6) Available only for QFN package.
(7) Applicable for 5.0V nominal supply: BV_{DD} = 4.5V to 5.5V.
(8) Applicable for 3.0V nominal supply: BV_{DD} = 2.7V to 3.6V.
(9) Measured with CLKOUT pin not loaded.

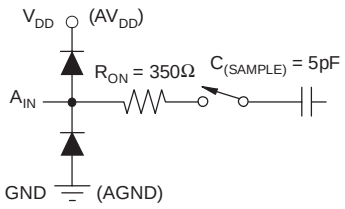
ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating free-air temperature range at −40°C to +125°C, AV_{DD} = BV_{DD} = +5V or V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, Mode 3, MCLK input = 20MHz, and 16-bit $Sinc^3$ filter, with OSR = 256, unless otherwise noted.

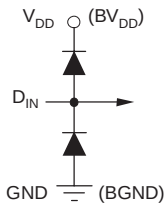
PARAMETER		TEST CONDITIONS	ADS1203I MIN	ADS1203I TYP(1)	ADS1203I MAX	UNITS
Digital Inputs(6)(8)						
	Logic family			LVCMOS		
V_{IH}	High-level input Voltage	BV_{DD} = 3.6V	2		BV_{DD}+0.3	V
V_{IL}	Low-level input voltage	BV_{DD} = 2.7V	−0.3		0.8	V
I_{IN}	Input current	V_I = BV_{DD} or GND			±50	nA
C_I	Input capacitance			5		pF
Digital Outputs(6)(8)						
	Logic family			LVCMOS		
V_{OH}	High-level output voltage	BV_{DD} = 2.7V, I_{OH} = −100µA	BV_{DD}−0.2			V
V_{OL}	Low-level output voltage	BV_{DD} = 2.7V, I_{OL} = +100µA			0.2	V
C_L	Load capacitance				30	pF
	Data format			Bit Stream		
Power Supply						
V_{DD}	Supply voltage		4.5		5.5	V
AV_{DD}(6)	Analog supply voltage		4.5		5.5	V
BV_{DD}(6)	Buffer I/O supply voltage	Low-voltage levels	2.7		3.6	V
		5V logic levels	4.5		5.5	V
I_{DD}	Supply current	Mode 0		8.4	10.5	mA
		Mode 3		6.7	8.5	mA
AI_{DD}(6)	Analog operating supply current	Mode 0		6.2	7.5	mA
		Mode 3		5.9	6.9	mA
BI_{DD}(6)	Buffer I/O operating supply current	BV_{DD} = 3V, Mode 0		2.2	2.3	mA
		BV_{DD} = 3V, Mode 3(9)		0.8	0.9	mA
	Power dissipation	Mode 0		42	49	mW
		Mode 3(9)		33.5	39	mW

(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for V_{IN}+ = −250mV to +250mV, expressed either as the number of LSBs or as a percent of measured input range (500mV).
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(5) With reduced accuracy, the supported external clock frequency range is 1MHz up to 32MHz.
(6) Available only for QFN package.
(7) Applicable for 5.0V nominal supply: BV_{DD} = 4.5V to 5.5V.
(8) Applicable for 3.0V nominal supply: BV_{DD} = 2.7V to 3.6V.
(9) Measured with CLKOUT pin not loaded.

EQUIVALENT INPUT CIRCUIT



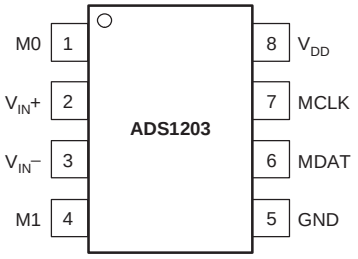
Diode Turn on Voltage: 0.4V
Equivalent Analog Input Circuit



Equivalent Digital Input Circuit

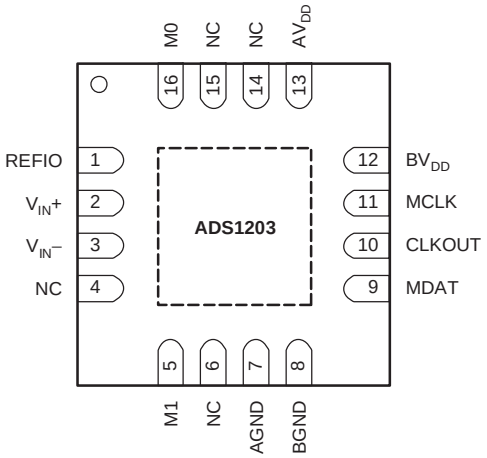
PIN ASSIGNMENTS: PW (TSSOP) PACKAGE

PW PACKAGE
TSSOP-8
(TOP VIEW)



PIN ASSIGNMENTS: RGT (QFN) PACKAGE

RGT PACKAGE(1)
QFN-16
(TOP VIEW)



(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

Terminal Functions: PW (TSSOP) Package

TERMINAL NAME	NO.	I/O	DESCRIPTION
M0	1	I	Mode input
V_{IN}+	2	I	Noninverting analog input
V_{IN}−	3	I	Inverting analog input
M1	4	I	Mode input
GND	5		Power supply ground
MDAT	6	O	Modulator data output
MCLK	7	I/O	Modulator clock input or output
V_{DD}	8		Power supply: +5V nominal

NOTE: For the TSSOP package, BGND and AGND are internally connected to the GND pin. Additionally, the AV_{DD} and BV_{DD} pins are connected to V_{DD}.

Terminal Functions: RGT (QFN) Package

TERMINAL NAME	NO.	I/O	DESCRIPTION
REFIO	1	I/O	Reference voltage input/output
V_{IN}+	2	I	Noninverting analog input
V_{IN}−	3	I	Inverting analog input
NC	4, 6, 14, 15	I	Not connected
M1	5	I	Mode input
AGND	7		Analog power-supply ground
BGND	8		Interface power-supply ground
MDAT	9	O	Modulator data output
CLKOUT	10	O	Modulator clock output (Mode 3 only)
MCLK	11	I/O	Modulator clock input or output
BV_{DD}	12		Interface power supply
AV_{DD}	13		Analog power supply
M0	16		Mode input

PARAMETER MEASUREMENT INFORMATION

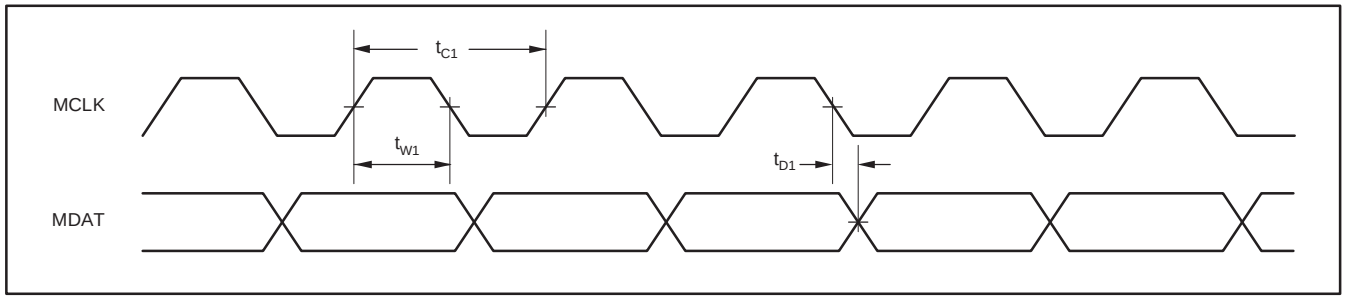


Figure 1. Mode 0 Operation

TIMING CHARACTERISTICS: MODE 0

Over recommended operating free-air temperature range at −40°C to +125°C, AV_{DD} = BV_{DD} = +5V(1) or AV_{DD} = +5V, BV_{DD} = +3V(2) or V_{DD} = +5V(1), unless otherwise noted.

PARAMETER		MODE	MIN	MAX	UNIT
t_{C1}	Clock period	0	91	111	ns
t_{W1}	Clock high time	0	(t_{C1}/2) − 5	(t_{C1}/2) + 5	ns
t_{D1}	Data delay after falling edge of clock	0	−2	2	ns

(1) Applicable for 5.0V nominal supply: BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V.
(2) Only for QFN package. Applicable for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V.

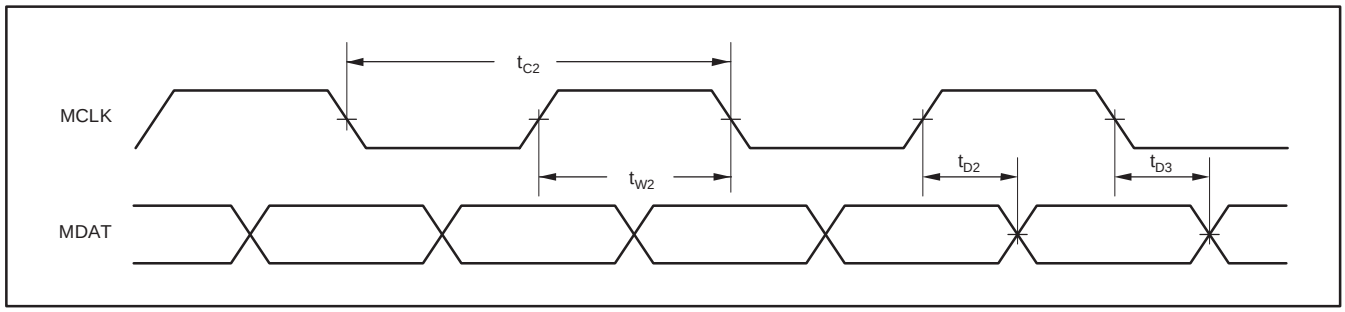


Figure 2. Mode 1 Operation

TIMING CHARACTERISTICS: MODE 1

Over recommended operating free-air temperature range at −40°C to +125°C, AV_{DD} = BV_{DD} = +5V(1) or AV_{DD} = +5V, BV_{DD} = +3V(2) or V_{DD} = +5V(1), unless otherwise noted.

PARAMETER		MODE	MIN	MAX	UNIT
t_{C2}	Clock period	1	182	222	ns
t_{W2}	Clock high time	1	(t_{C2}/2) − 5	(t_{C2}/2) + 5	ns
t_{D2}	Data delay after rising edge of clock	1	(t_{W2}/2) − 2	(t_{W2}/2) + 2	ns
t_{D3}	Data delay after falling edge of clock	1	(t_{W2}/2) − 2	(t_{W2}/2) + 2	ns

(1) Applicable for 5.0V nominal supply: BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V.
(2) Only for QFN package. Applicable for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V.

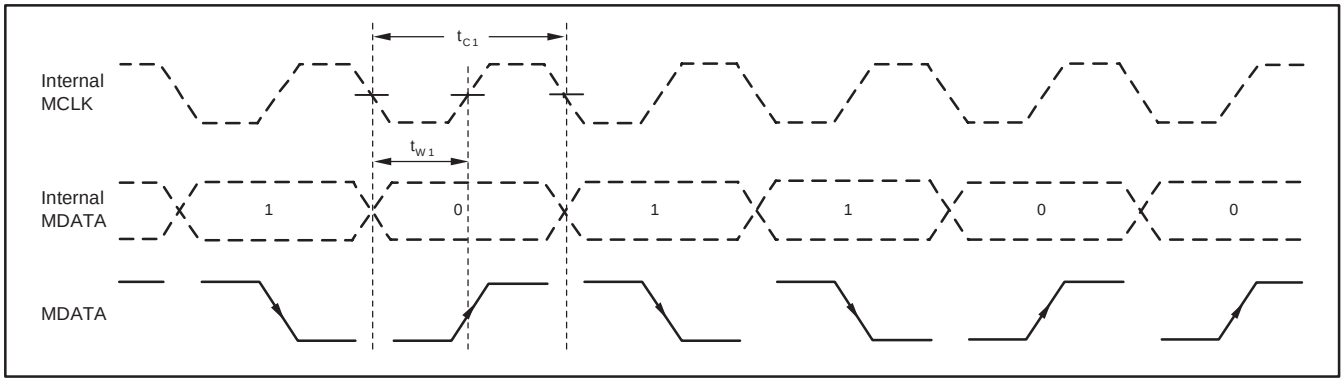


Figure 3. Mode 2 Operation

TIMING CHARACTERISTICS: MODE 2

Over recommended operating free-air temperature range at −40°C to +125°C, AV_{DD} = BV_{DD} = +5V(1) or AV_{DD} = +5V, BV_{DD} = +3V(2) or V_{DD} = +5V(1), unless otherwise noted.

PARAMETER		MODE	MIN	MAX	UNIT
t_{C1}	Clock period	2	91	111	ns
t_{W1}	Clock high time	2	(t_{C1}/2) − 5	(t_{C1}/2) + 5	ns

(1) Applicable for 5.0V nominal supply: BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V.
(2) Only for QFN package. Applicable for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V.

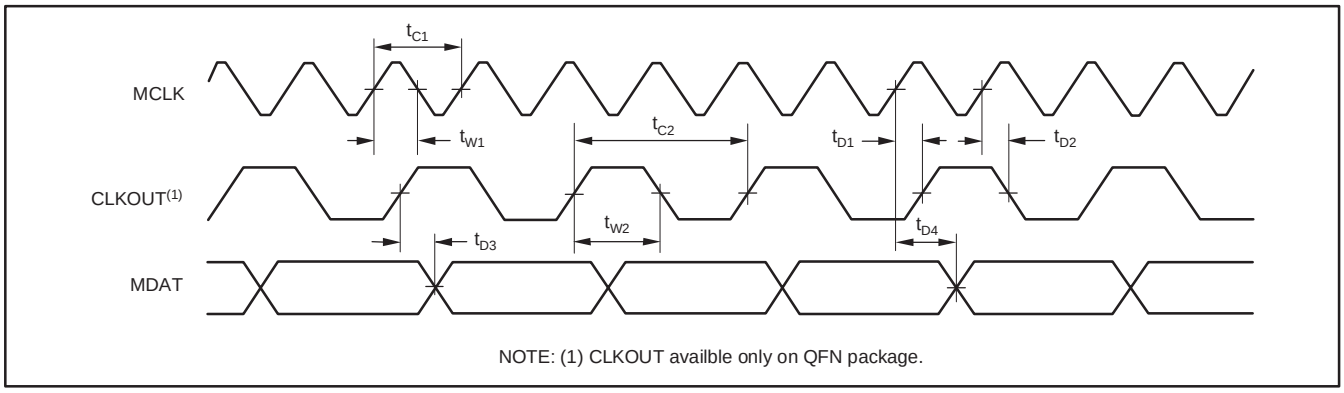


Figure 4. Mode 3 Operation

TIMING CHARACTERISTICS: MODE 3

Over recommended operating free-air temperature range at −40°C to +125°C, AV_{DD} = BV_{DD} = +5V(1) or AV_{DD} = +5V, BV_{DD} = +3V(2) or V_{DD} = +5V(1), unless otherwise noted.

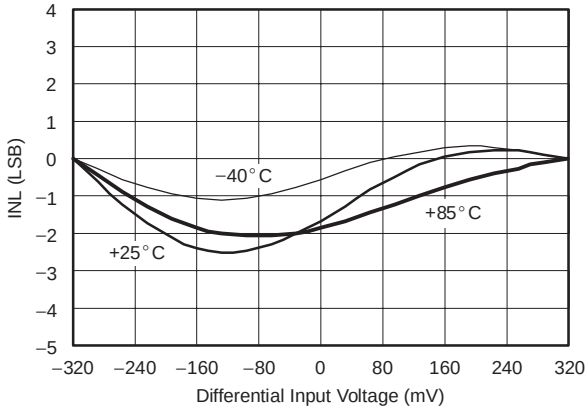
PARAMETER		MIN	MAX	UNIT
t_{C1}	MCLK period	41.6	1000	ns
t_{W1}	MCLK high time	10	t_{C1} − 10	ns
t_{C2}	CLKOUT period	2 × t_{C1}	2 × t_{C1}	ns
t_{W2}	CLKOUT high time	(t_{C2}/2) − 5	(t_{C2}/2) + 5	ns
t_{D1}	CLKOUT rising edge delay after MCLK rising edge	0	10	ns
t_{D2}	CLKOUT falling edge delay after MCLK rising edge	0	10	ns
t_{D3}	Data valid delay after rising edge of CLKOUT	−2	+2	ns
t_{D4}	Data valid delay after rising edge of MCLK	0	10	ns

NOTE: Input signal is specified with t_R = t_F = 5ns (10% to 90% of BV_{DD} or V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See timing diagram.
(1) Applicable for 5.0V nominal supply: BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V.
(2) Only for QFN package. Applicable for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V.

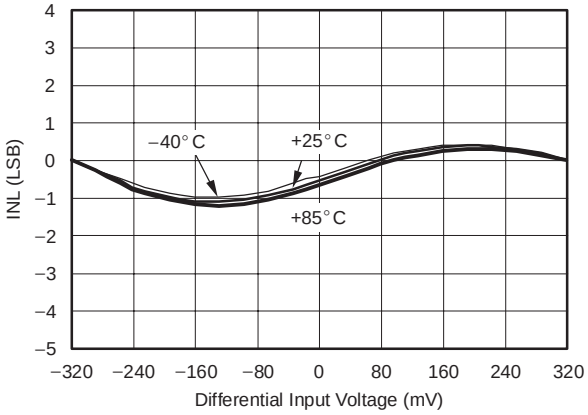
TYPICAL CHARACTERISTICS

AV_{DD} = BV_{DD} = +5V or V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit $Sinc^3$ filter, with OSR = 256, unless otherwise noted.

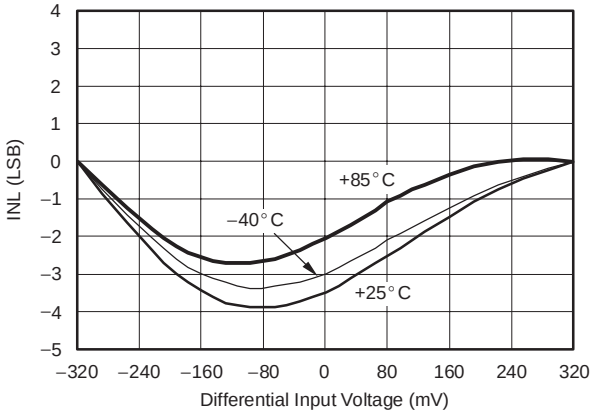
INTEGRAL NONLINEARITY vs INPUT SIGNAL
(Mode 0)



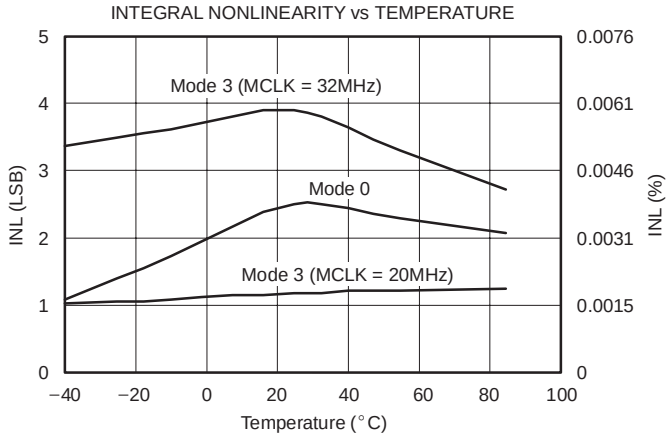
INTEGRAL NONLINEARITY vs INPUT SIGNAL
(Mode 3, MCLK = 20MHz)



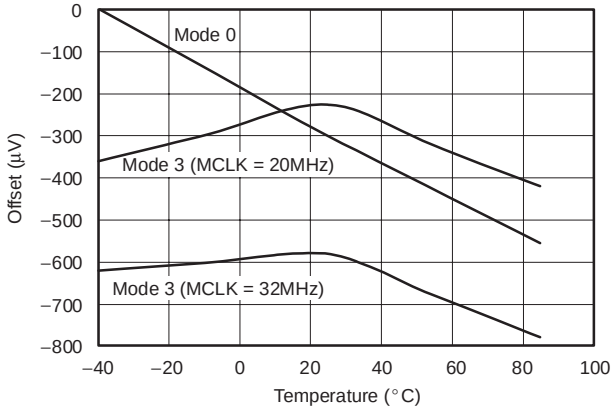
INTEGRAL NONLINEARITY vs INPUT SIGNAL
(Mode 3, MCLK = 32MHz)



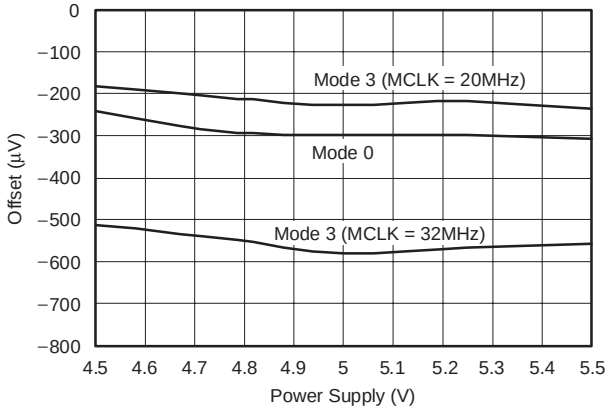
INTEGRAL NONLINEARITY vs TEMPERATURE



OFFSET vs TEMPERATURE



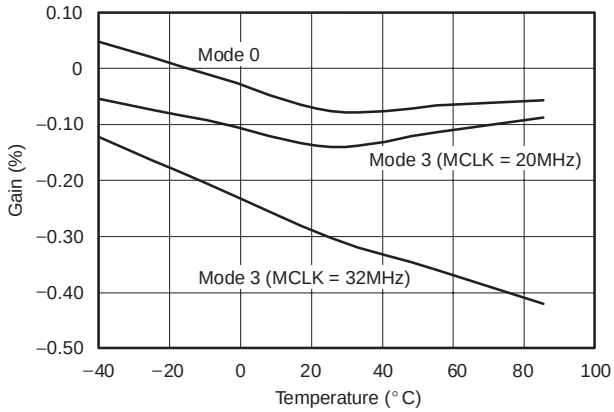
OFFSET vs POWER SUPPLY



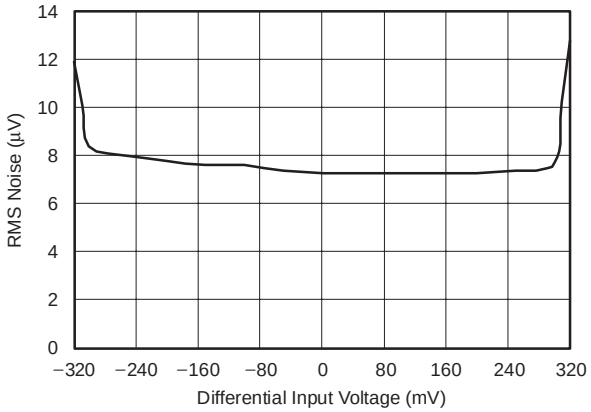
TYPICAL CHARACTERISTICS (continued)

AV_{DD} = BV_{DD} = +5V or V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit $Sinc^3$ filter, with OSR = 256, unless otherwise noted.

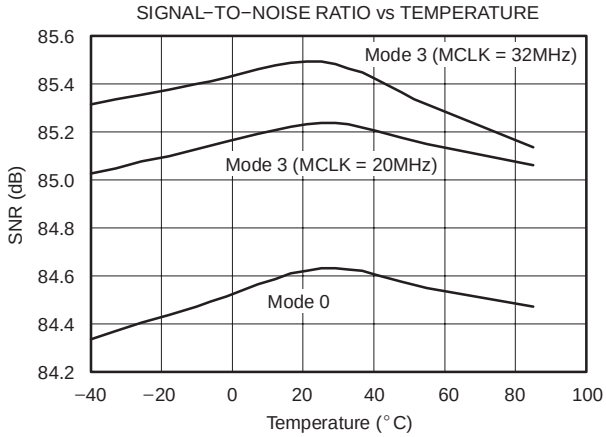
GAIN vs TEMPERATURE



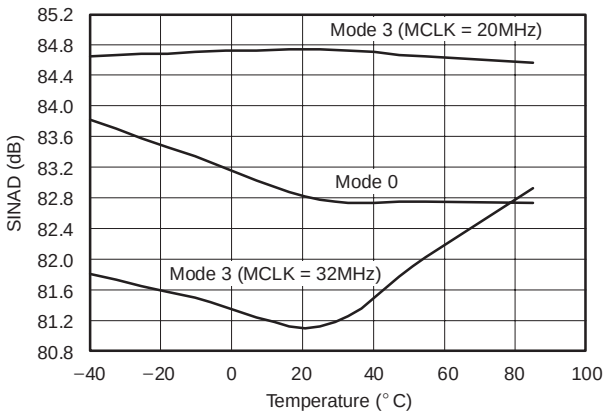
RMS NOISE vs INPUT VOLTAGE LEVEL



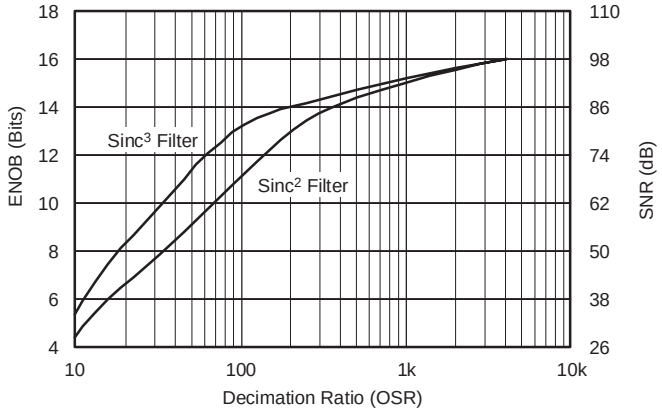
SIGNAL−TO−NOISE RATIO vs TEMPERATURE



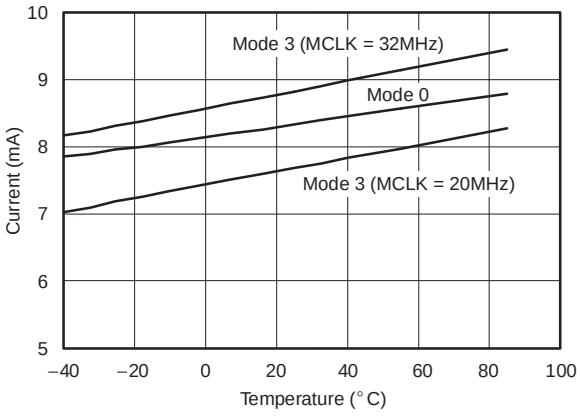
SIGNAL−TO−NOISE + DISTORTION vs TEMPERATURE



EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



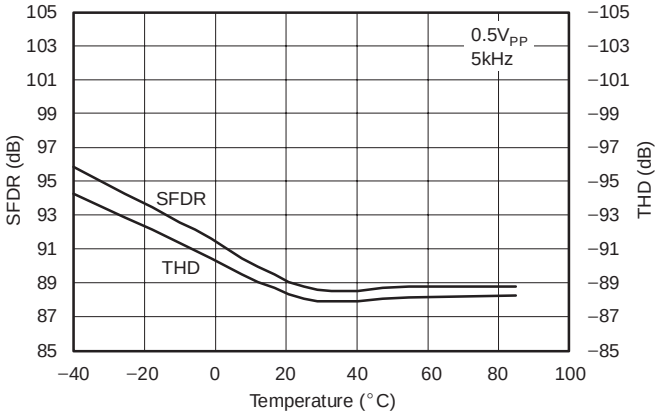
POWER−SUPPLY CURRENT vs TEMPERATURE



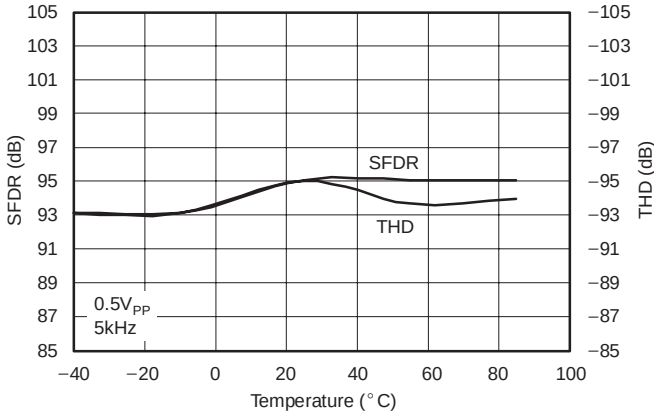
TYPICAL CHARACTERISTICS (continued)

AV_{DD} = BV_{DD} = +5V or V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit $Sinc^3$ filter, with OSR = 256, unless otherwise noted.

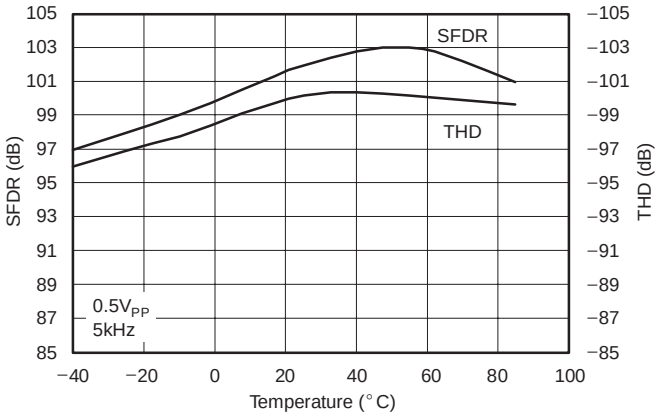
SPURIOUS−FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs TEMPERATURE
(Mode 0)



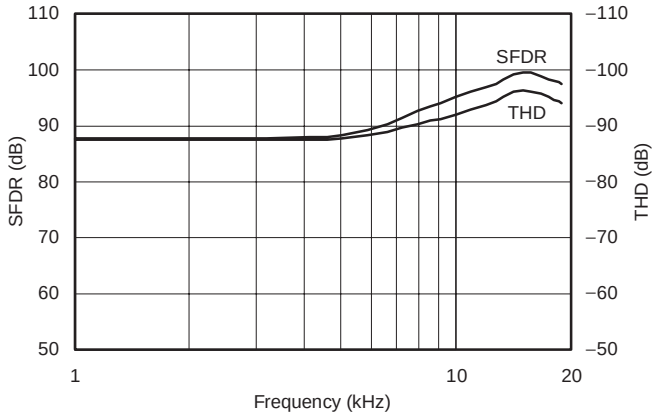
SPURIOUS−FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs TEMPERATURE
(Mode 3, MCLK = 20MHz)



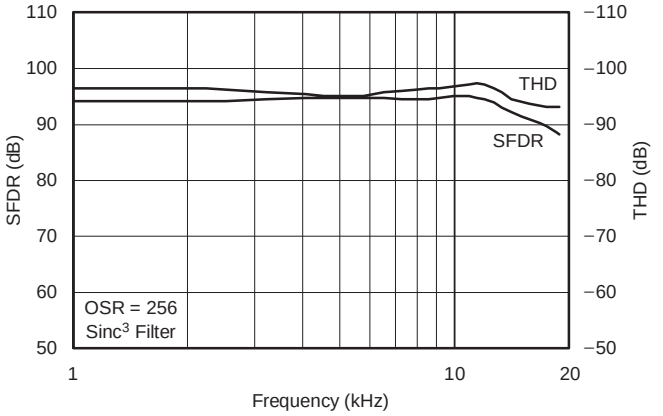
SPURIOUS−FREE DYNAMIC RANGE
AND TOTAL HARMONIC DISTORTION
vs TEMPERATURE (Mode 3, MCLK = 32MHz)



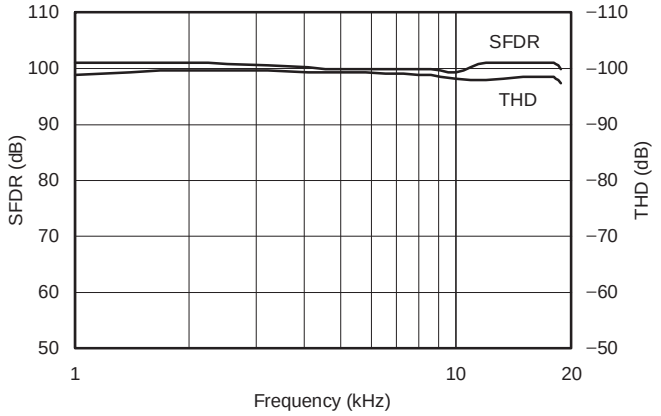
SPURIOUS−FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY
(Mode 0)



SPURIOUS−FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY
(Mode 3, MCLK = 20MHz)



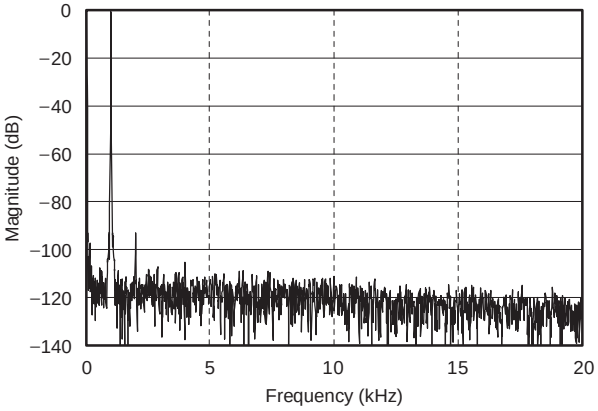
SPURIOUS−FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY
(Mode 3, MCLK = 32MHz)



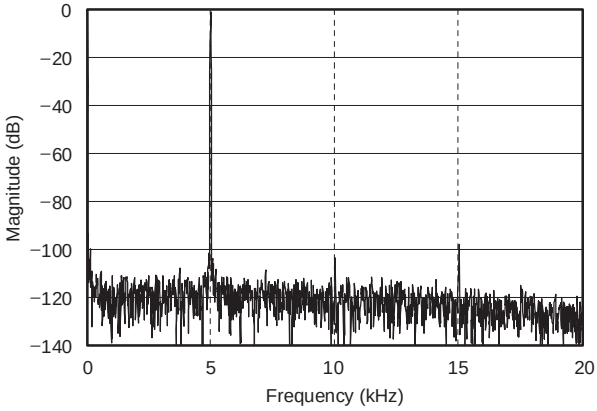
TYPICAL CHARACTERISTICS (continued)

AV_{DD} = BV_{DD} = +5V or V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit $Sinc^3$ filter, with OSR = 256, unless otherwise noted.

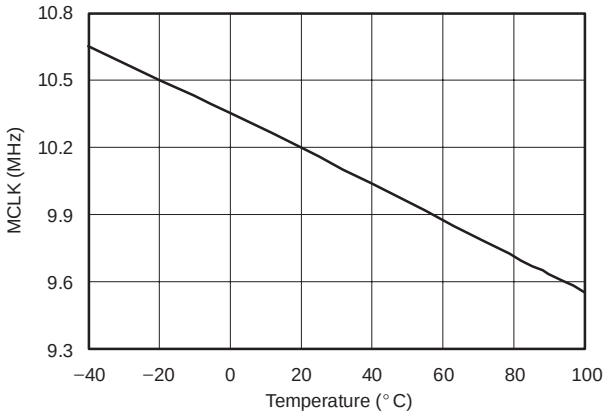
FREQUENCY SPECTRUM
(4096 Point FFT, f_{IN} = 1kHz, 0.5V_{PP})



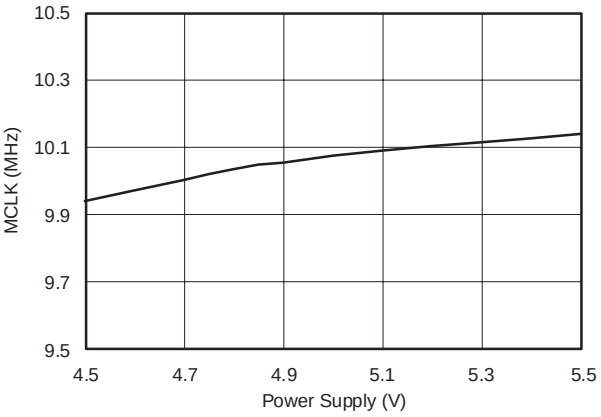
FREQUENCY SPECTRUM
(4096 Point FFT, f_{IN} = 5kHz, 0.5V_{PP})



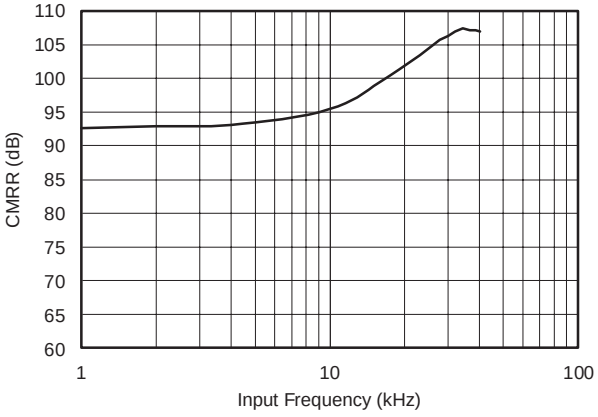
CLOCK FREQUENCY vs TEMPERATURE



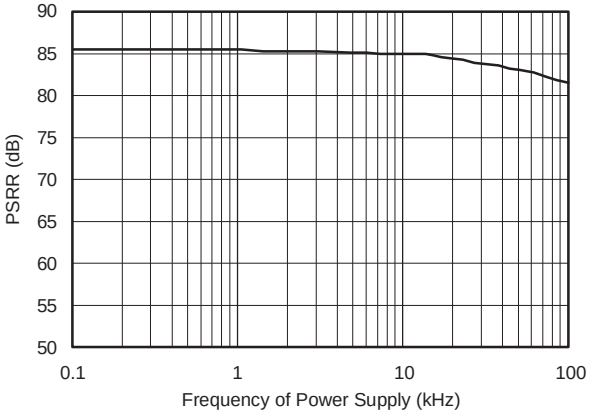
CLOCK FREQUENCY vs POWER SUPPLY



COMMON−MODE REJECTION RATIO
vs FREQUENCY



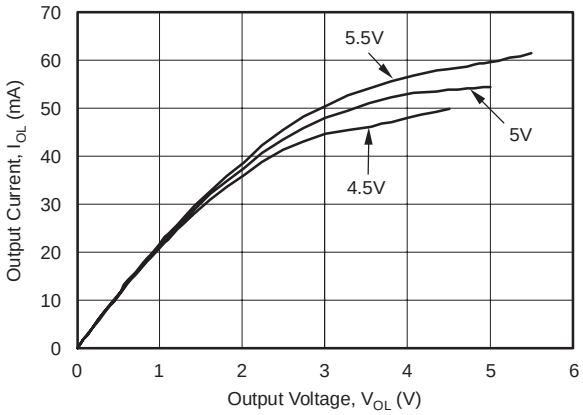
POWER−SUPPLY REJECTION RATIO
vs FREQUENCY



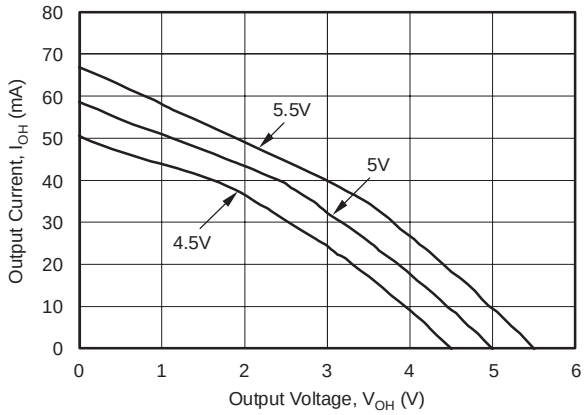
TYPICAL CHARACTERISTICS (continued)

AV_{DD} = BV_{DD} = +5V or V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit $Sinc^3$ filter, with OSR = 256, unless otherwise noted.

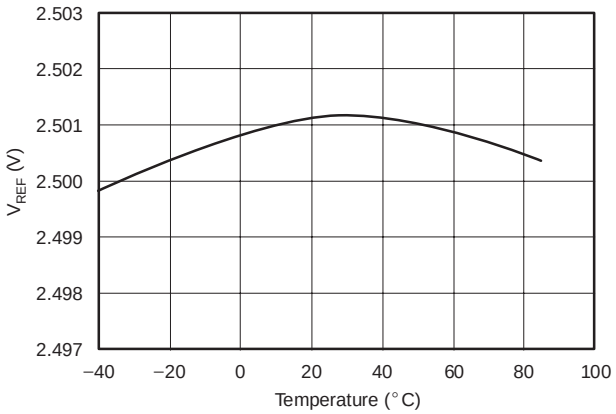
MCLK AND MDAT
TYPICAL SINK CURRENT



MCLK AND MDAT
TYPICAL SOURCE CURRENT



REFERENCE VOLTAGE vs TEMPERATURE



GENERAL DESCRIPTION

The ADS1203 is a single-channel, 2nd-order, CMOS delta-sigma modulator, designed for medium- to high-resolution A/D conversions from DC to 39kHz with an oversampling ratio (OSR) of 256. The output of the converter (MDAT) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies. A low-pass digital filter should be used at the output of the delta-sigma modulator. The primary purpose of the digital filter is to filter out high-frequency noise. The secondary purpose is to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). A digital signal processor (DSP), microcontroller (μC), or field programmable gate array (FPGA) could be used to implement the digital filter. Figure 6 shows the ADS1203 connected to a DSP.

The overall performance (speed and accuracy) depends on the selection of an appropriate OSR and filter type. A higher OSR produces greater output accuracy while operating at a lower refresh rate. Alternatively, a lower OSR produces lower output accuracy, but operates at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range exceeding 95dB with an OSR = 256.

THEORY OF OPERATION

The differential analog input of the ADS1203 is implemented with a switched-capacitor circuit. This circuit implements a 2nd-order modulator stage, which digitizes the analog input signal into a 1-bit output stream. The clock source can be internal as well as external. Different frequencies for this clock allow for a variety of solutions and signal bandwidths (however, this can only be used in mode 3). The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream, which accurately represents the analog input voltage over time, appears at the output of the converter.

REFERENCE

Under normal operation, REFIO (pin 1) provides an internal +2.5V reference to the ADS1203. However, the ADS1203 can operate with an external reference in the range of 0.5V to 2.6V, for a corresponding full-scale range of 0.256 × REFIO, as long as the input does not exceed the AV_{DD} + 0.3V value. The recommended input range is ±0.1 × REFIO.

The ADS1203 reference is double-buffered. If the internal reference is used to drive an external load, it can only drive a high-impedance load because R_I = 20kΩ. If an external reference voltage is used, the external source must be capable of driving the 20kΩ resistor. To minimize noise, a 0.1μF capacitor should be connected to REFIO.

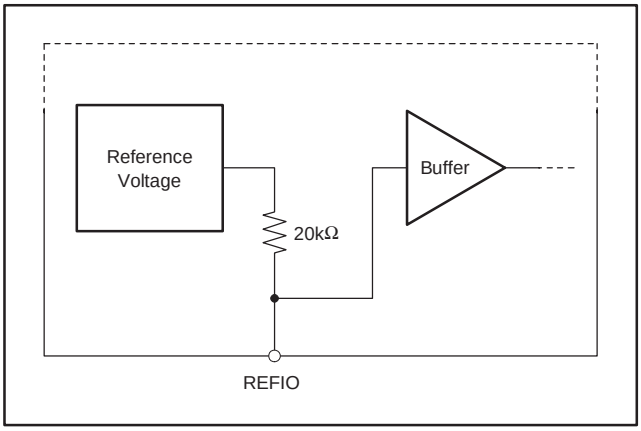


Figure 5. REFIO Voltage Reference Connection

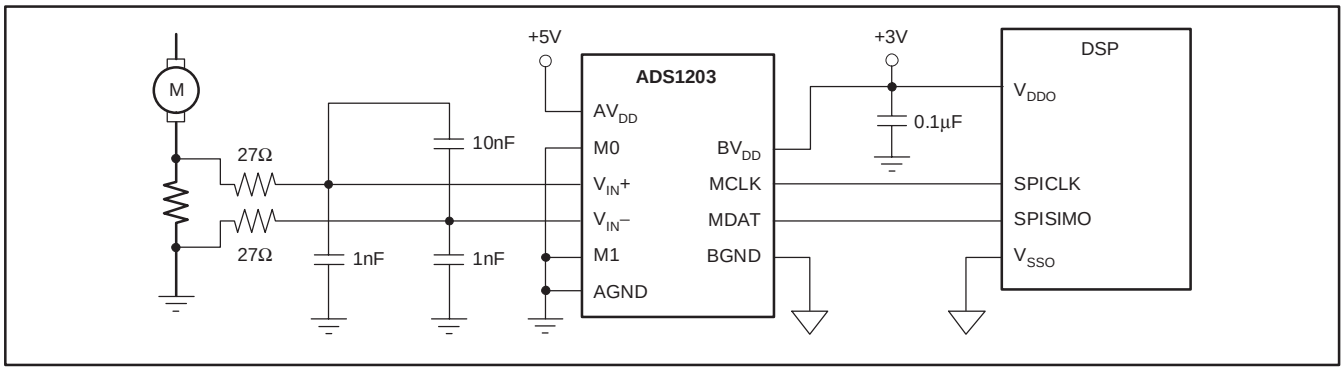


Figure 6. Connection Diagram for the ADS1203 Delta-Sigma Modulator Including DSP

ANALOG INPUT STAGE

Analog Input

The input design topology of the ADS1203 is based on a fully differential switched-capacitor architecture. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (92dB), and excellent power-supply rejection.

The input impedance of the analog input depends on the modulator clock frequency (f_{CLK}), which is also the sampling frequency of the modulator. Figure 7 shows the basic input structure of the ADS1203. The relationship between the input impedance of the ADS1203 and the modulator clock frequency is:

$$Z_{IN} = \frac{28k\Omega}{f_{CLK}/10MHz} \quad (1)$$

The input impedance becomes a consideration in designs where the source impedance of the input signal is high. This may cause a degradation in gain, linearity and THD. The importance of this effect depends on the desired system performance. There are two restrictions on the analog input signals, V_{IN}+ and V_{IN}−. If the input voltage exceeds the range GND – 0.4V to V_{DD} + 0.3V, the input current must be limited to 10mA because the input protection diodes on the front end of the converter will begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog voltage resides within ±250mV; however, the FSR input voltage is ±320mV.

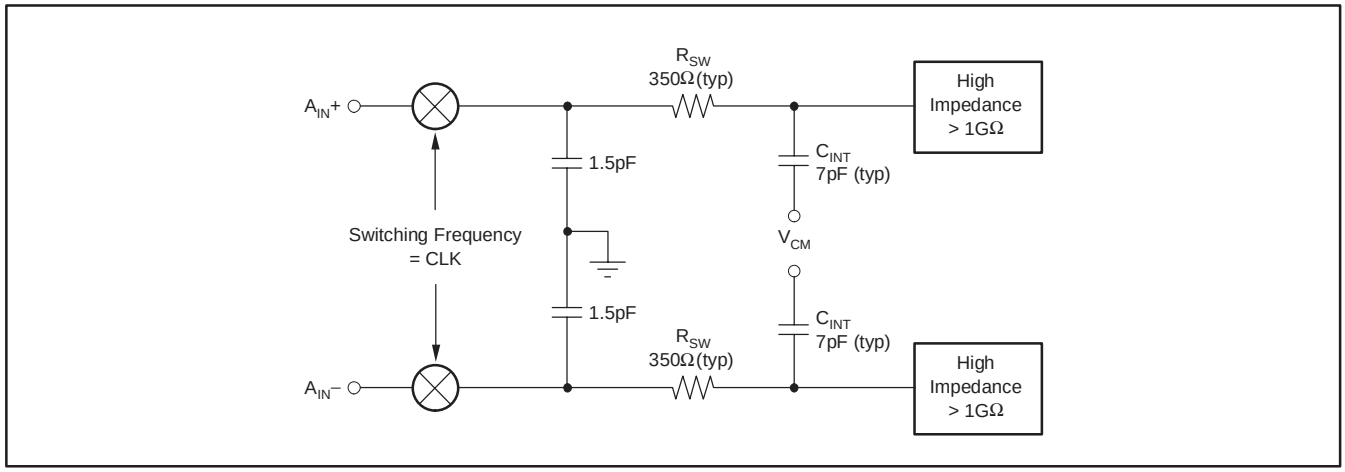


Figure 7. Input Impedance of the ADS1203

Modulator

The ADS1203 can be operated in four modes. Modes 0, 1, and 2 use the internal clock, which is fixed at 20MHz. The modulator can also be operated with an external clock in mode 3. In all modes, the clock is divided by 2 internally and is used as the modulator clock. The frequency of the external clock can vary from 1MHz to 32MHz to adjust for the clock requirements of the application.

The modulator topology is fundamentally a 2nd-order, switched-capacitor, delta-sigma modulator, such as the one conceptualized in Figure 8. The analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing analog voltages at X_2 and X_3. The voltages at X_2 and X_3 are presented to the respective individual integrators. The output of these integrators progresses in a negative or positive direction. When the value of the signal at X_4 equals the comparator reference voltage, the output of the comparator switches from negative to positive, or positive to negative, depending on its original state. When the output value of the comparator switches from high to low or vice versa, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage at X_6, causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators forces the value of the integrator output to track the average of the input.

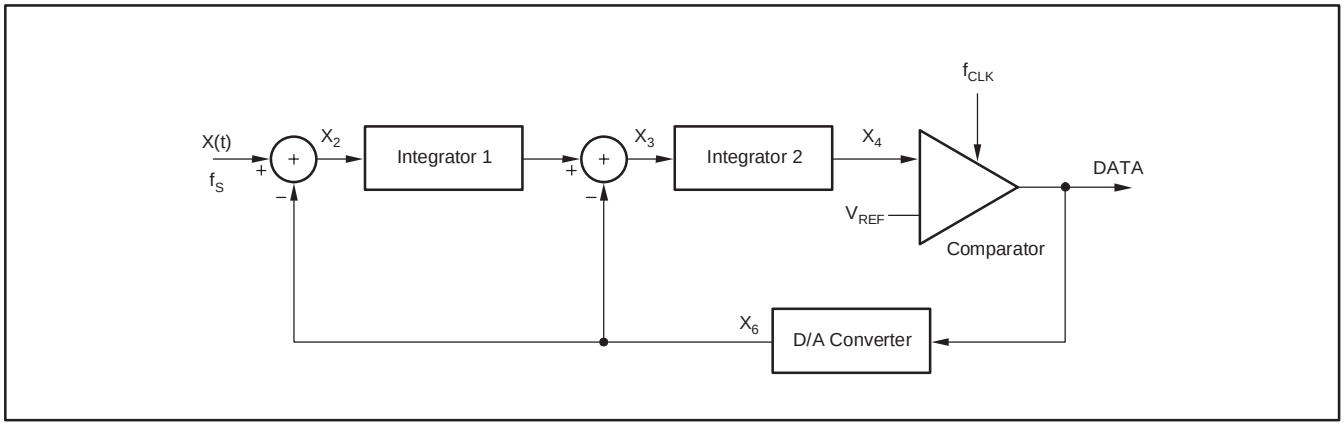


Figure 8. Block Diagram of the 2nd-Order Modulator

DIGITAL OUTPUT

A differential input signal of 0V ideally produces a stream of ones and zeros that is high 50% of the time and low 50% of the time. A differential input of +256mV produces a stream of ones and zeros that is high 80% of the time. A differential input of –256mV produces a stream of ones and zeros that is high 20% of the time. The input voltage versus the output modulator signal is shown in Figure 9.

DIGITAL INTERFACE

INTRODUCTION

The analog signal that is connected to the input of the delta-sigma modulator is converted using the clock signal applied to the modulator. The result of the conversion, or modulation, is the output signal DATA from the delta-sigma modulator. In most applications where a direct connection is realized between the delta-sigma modulator and an ASIC, FPGA, DSP, or µC (each with an implemented filter), the two standard signals (MCLK and MDAT) are provided from the modulator. To reduce the wiring (for example, for galvanic isolation), a single line is preferred. Therefore, in mode 2, the data stream is Manchester-encoded.

MODES OF OPERATION

The system clock of the ADS1203 is 20MHz by default. The system clock can be provided either from the internal 20MHz RC oscillator or from an external clock source. For this purpose, the MCLK pin is bidirectional and controlled by the mode setting.

The system clock is divided by 2 for the modulator clock. Therefore, the default clock frequency of the modulator is 10MHz. With a possible external clock range of 1MHz to 32MHz, the modulator operates between 500kHz and 16MHz.

The four modes of operation for the digital data interface are shown in Table 1.

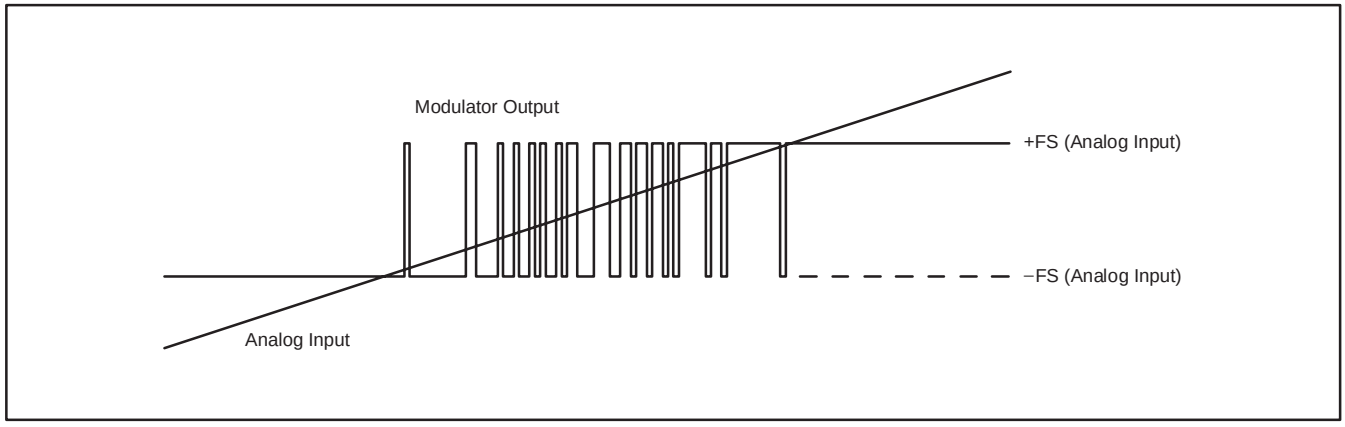


Figure 9. Analog Input vs Modulator Output of the ADS1203

Table 1. Digital Data Interface Modes of Operation

MODE	DEFINITION	M1	M0
0	Internal clock, synchronous data output	Low	Low
1	Internal clock, synchronous data output, half output clock frequency	Low	High
2	Internal clock, Manchester-encoded data output	High	Low
3	External clock, synchronous data output	High	High

Mode 0

In mode 0, the internal RC oscillator is running. The data are provided at the MDAT output pin, and the modulator clock at the MCLK pin. The data change at the falling edge of MCLK; therefore, the data can safely be strobed with the rising edge. See Figure 1 on page 7.

Mode 1

In mode 1, the internal RC oscillator is running. The data are provided at the MDAT output pin. The MCLK pin provides the half modulator clock. The data must be strobed at both the rising and falling edges of MCLK. The data at MDAT change in the middle, between the rising and falling edge. In this mode the frequency of both MCLK and MDAT is only 5MHz. See Figure 2 on page 7.

Mode 2

In mode 2, the internal RC oscillator is running. The data are Manchester-encoded and are provided at the MDAT pin. The MCLK output is set to low. There is no clock output provided in this mode. The Manchester coding allows the data transfer with only a single line. See Figure 3 on page 8.

Mode 3

In mode 3, the internal RC oscillator is disabled. The system clock must be provided externally at the input MCLK. The system clock must have twice the frequency of the chosen modulator clock. The data are provided at the MDAT output pin. Because the modulator runs with the half system clock, the data change at every other falling edge of the external clock. The data can safely be strobed at every other rising edge of MCLK. This mode allows synchronous operation to any digital system or the use of clocks different from 10MHz. See Figure 4 on page 8. On the QFN package, the modulator clock is provided as the CLKOUT signal. Output data can be strobed at each rising edge of CLKOUT.

FILTER USAGE

The modulator generates only a bitstream, which does not output a digital word like an analog-to-digital converter (ADC). In order to output a digital word equivalent to the analog input voltage, the bitstream must be processed by a digital filter.

A very simple filter built with minimal effort and hardware is the sinc^3 filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (for example, count of digital gates). For oversampling ratios in the range of 16 to 256, this is a good choice. All the characterizations in the data sheet are also done using a sinc^3 filter with an oversampling ratio of OSR = 256 and an output word width of 16 bits.

In a sinc^3 filter response (shown in Figure 10 and Figure 11), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK}/OSR$. The –3dB point is located at half the Nyquist frequency or $f_{DATA}/4$. For some applications, it may be necessary to use another filter type for better frequency response.

This performance can be improved, for example, by a cascaded filter structure. The first decimation stage can be a sinc^3 filter with a low OSR and the second stage a high-order filter.

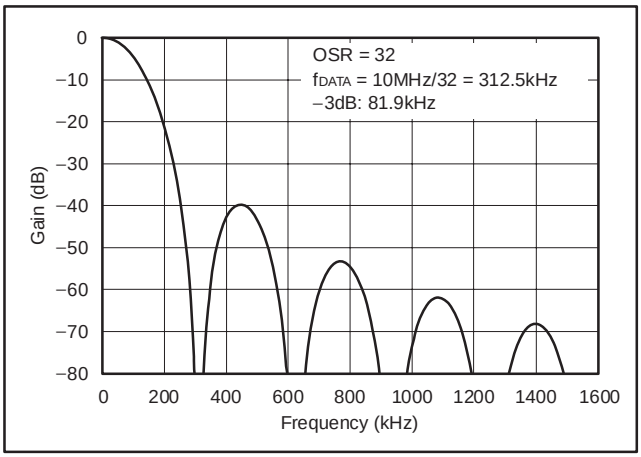


Figure 10. Frequency Response of Sinc^3 Filter

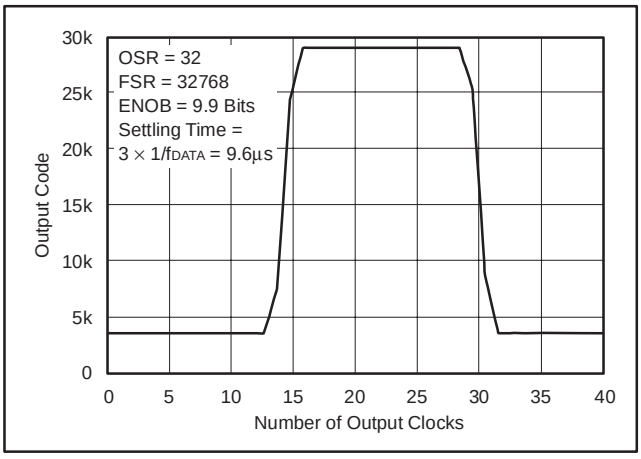


Figure 11. Pulse Response of Sinc^3 Filter (f_{MOD} = 10MHz)

The effective number of bits (ENOB) can be used to compare the performance of ADCs and delta-sigma modulators. Figure 12 shows the ENOB of the ADS1203 with different filter types. In this data sheet, the ENOB is calculated from the SNR:

$$SNR = 1.76dB + 6.02dB \times ENOB \quad (3)$$

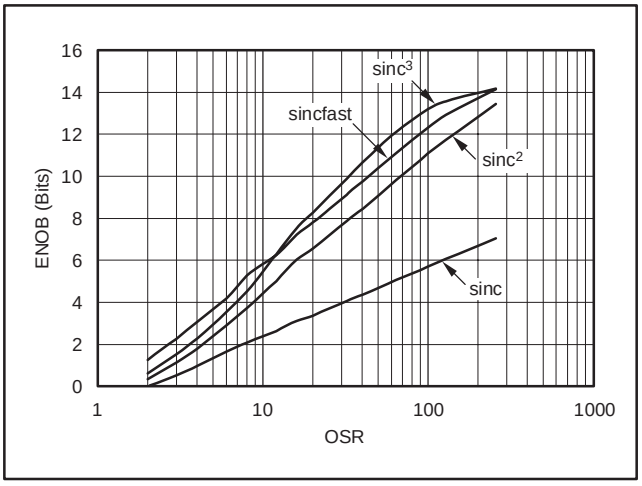


Figure 12. Measured ENOB vs OSR

In motor control applications, a very fast response time for overcurrent detection is required. There is a constraint between 1µs and 5µs with 3 bits to 7 bits resolution. The time for full settling depends on the filter order. Therefore, the full settling of the $sinc^3$ filter needs three data clocks and the $sinc^2$ filter needs two data clocks. The data clock is equal to the modulator clock divided by the OSR. For overcurrent protection, filter types other than $sinc^3$ might be a better choice. A simple example is a $sinc^2$ filter. Figure 13 compares the settling time of different filter types. The sincfast is a modified $sinc^2$ filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^2 \left(1 + z^{-2 \times OSR}\right) \quad (4)$$

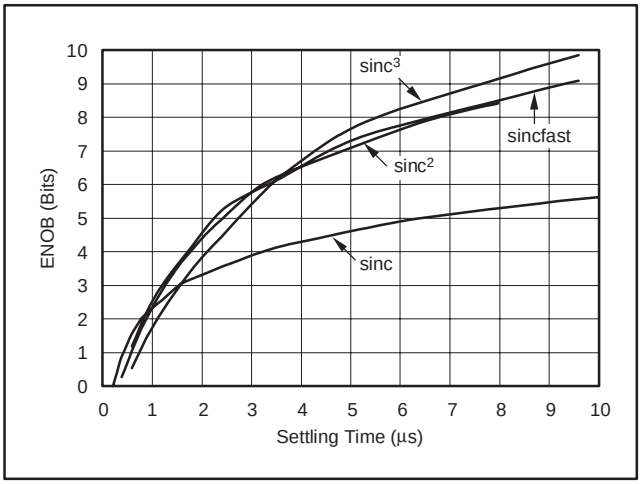


Figure 13. Measured ENOB vs Settling Time

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at www.ti.com.

APPLICATIONS

Operating the ADS1203 in a typical application using mode 0 is shown in Figure 14. Measurement of the motor phase current is done through the shunt resistor. For better performance, both signals are filtered. R_2 and C_2 filter noise on the noninverting input signal, R_3 and C_3 filter noise on the inverting input signal, and C_4 in combination with R_2 and R_3 filter the differential input signal. In this configuration, the shunt resistor is connected via three wires with the ADS1203.

The power supply is taken from the upper gate driver power supply. A decoupling capacitor of 0.1µF is recommended for filtering the power supply. If better filtering is required, an additional 1µF to 10µF capacitor can be added.

The control lines M0 and M1 are both low while the part is operating in mode 0. Two output signals, MCLK and MDAT, are connected directly to the optocoupler. The optocoupler can be connected to transfer a direct or inverse signal because the output stage has the capacity to source and sink the same current. The discharge resistor is not needed in parallel with optocoupler diodes because the output driver has push-pull capability to keep the LED diode out of the charge.

The DSP (such as a C28x or C24x) can be directly connected at the output of two channels of the optocoupler. In this configuration, the signals arriving at C28x or C24x are standard delta-sigma modulator signals and are connected directly to the SPICLK and SPISIMO pins. Being a delta-sigma converter, there is no need to have word sync on the serial data, so an SPI is ideal for connection. McBSP would work as well in SPI mode.

When component reduction is necessary, the ADS1203 can operate in mode 2, as shown in Figure 15. M1 is high and M0 is low. Only the noninverting input signal is filtered. R_2 and C_2 filter noise on the input signal. The inverting input is directly connected to the GND pin, which is simultaneously connected to the shunt resistor.

The output signal from the ADS1203 is Manchester-encoded. In this case, only one signal is transmitted. For that reason, one optocoupler channel is used instead of two channels, as in the previous example of Figure 14. Another advantage of this configuration is that the DSP will use only one line per channel instead of two. That permits the use of smaller DSP packages in the application.

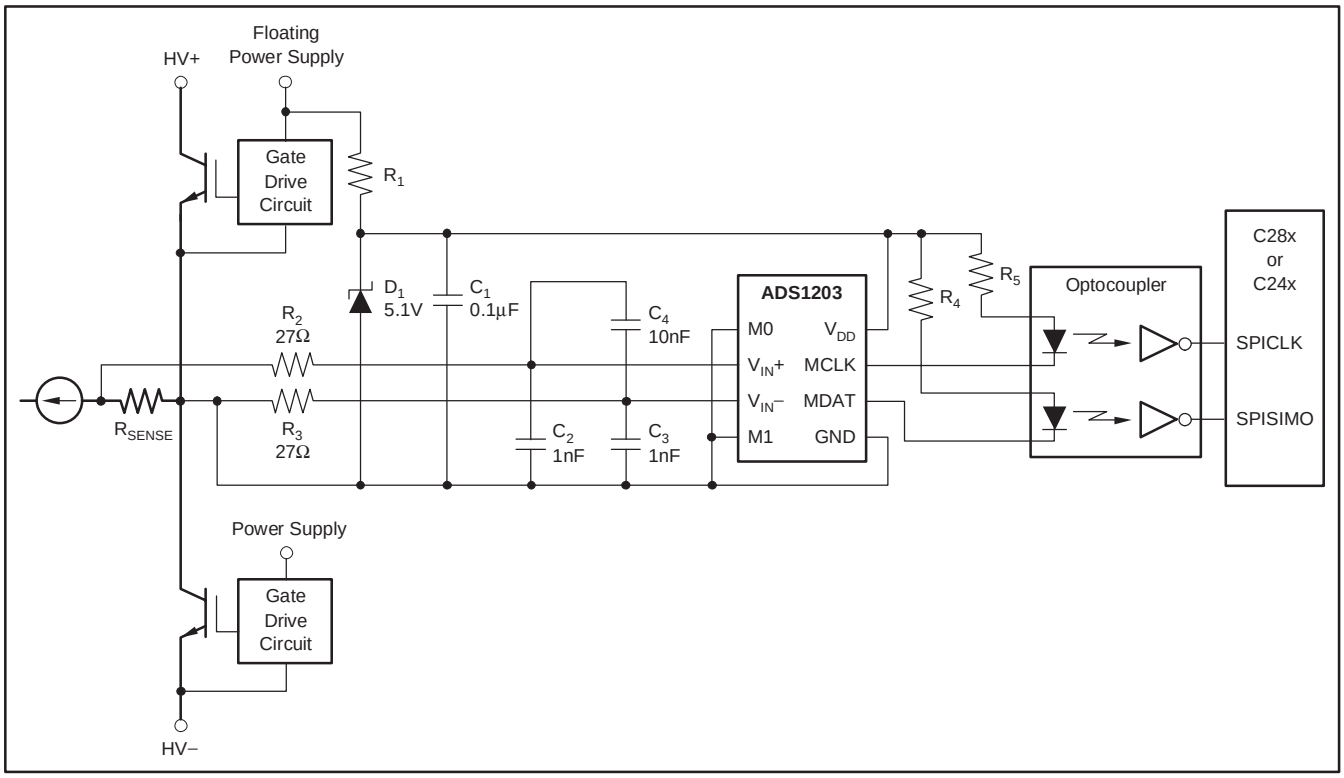


Figure 14. Application Diagram in Mode 0

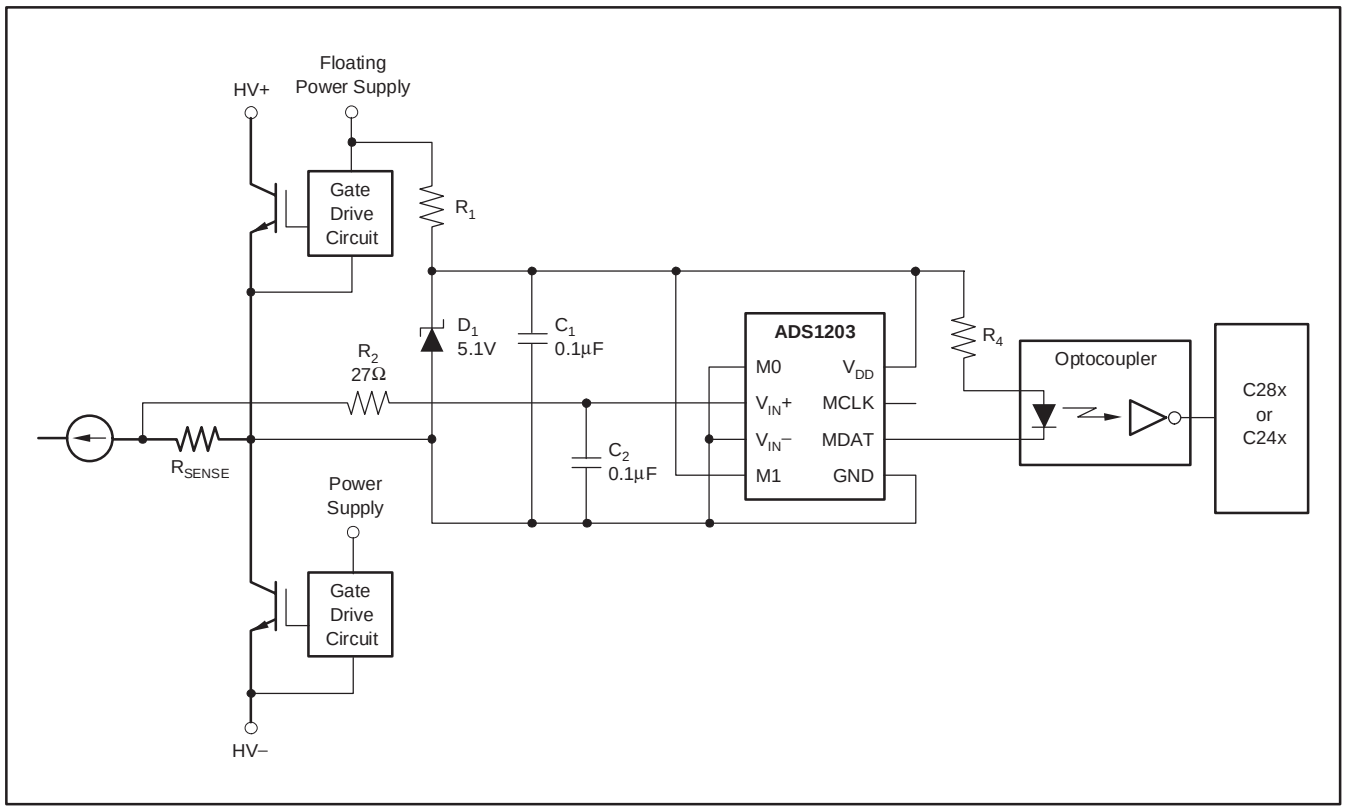


Figure 15. Application Diagram in Mode 2

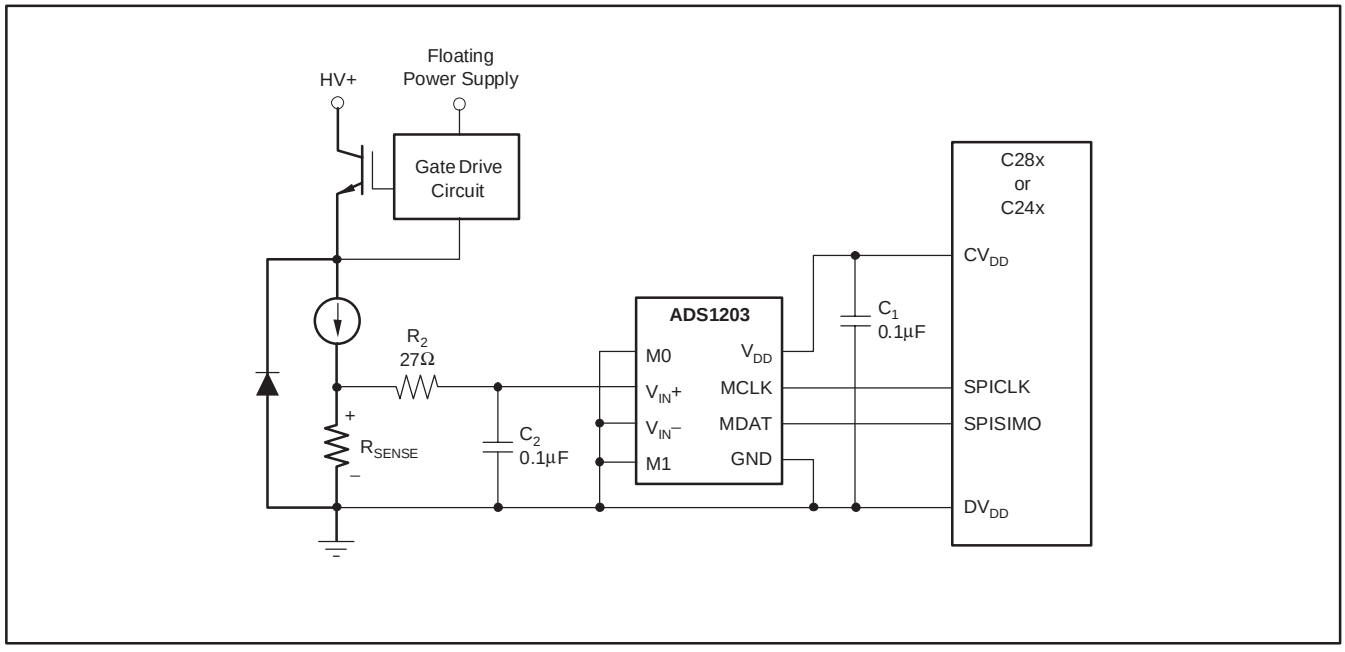


Figure 16. Application Diagram without Galvanic Isolation in Mode 0

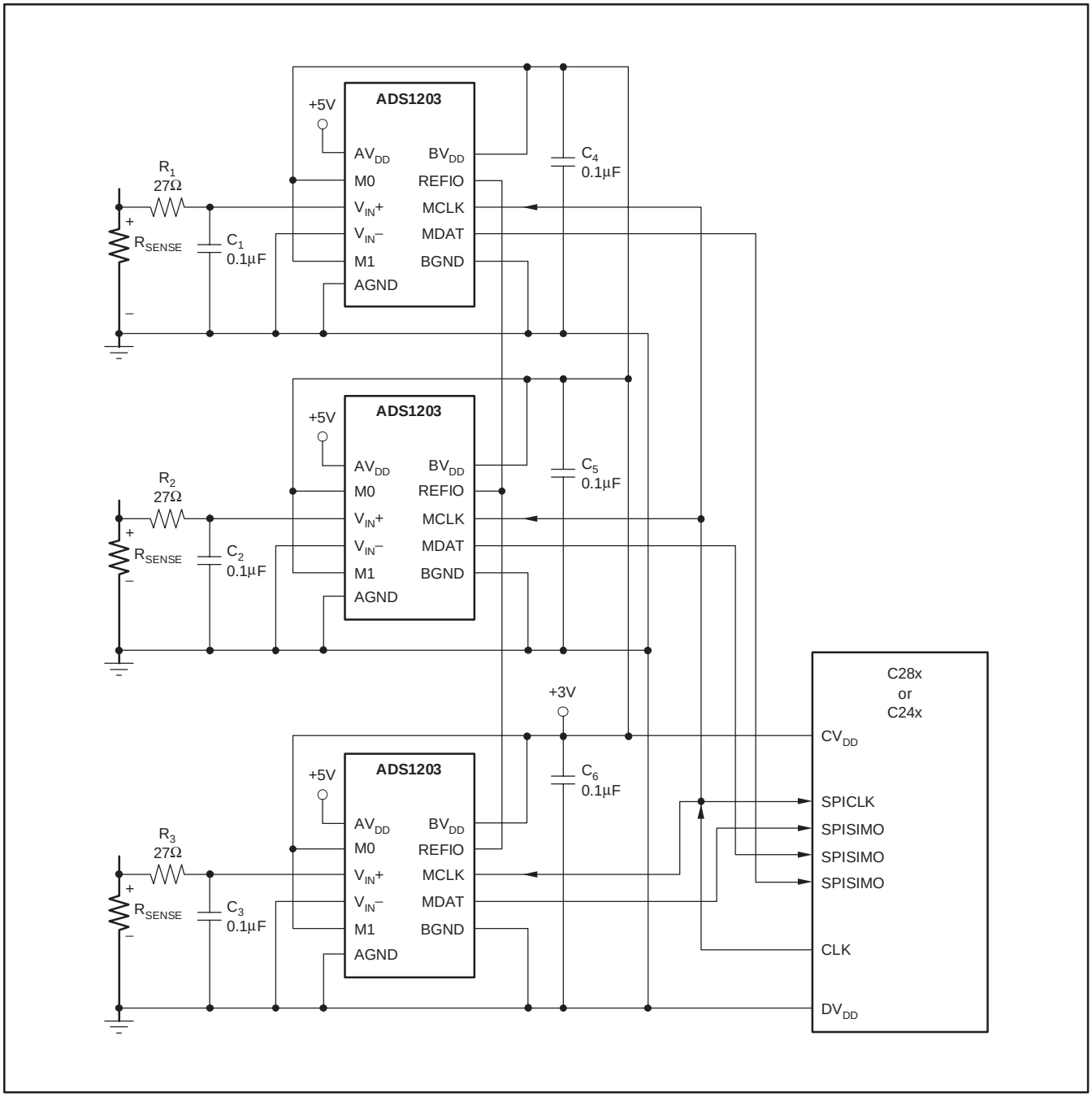


Figure 17. Application Diagram without Galvanic Isolation in Mode 3

LAYOUT CONSIDERATIONS

Power Supplies

The ADS1203 requires only one power supply (V_{DD}). If there are separate analog and digital power supplies on the board, a good design approach is to have the ADS1203 connected to the analog power supply. Another possible approach to control noise is the use of a resistor on the power supply. The connection can be made between the ADS1203 power-supply pins via a 10Ω resistor. The combination of this resistor and the decoupling capacitors between the power-supply pins on the ADS1203 provide some filtering. The analog supply that is used must be well-regulated and generate low noise. For designs requiring higher resolution from the ADS1203, power-supply rejection will be a concern. The digital power supply has high-frequency noise that can be capacitively coupled into the analog portion of the ADS1203. This noise can originate from switching power supplies, microprocessors, or DSPs. High-frequency noise will generally be rejected by the external digital filter at integer multiples of MCLK. Just below and above these frequencies, noise will alias back into the passband of the digital filter, affecting the conversion result. Inputs to the ADS1203, such as V_{IN}+, V_{IN}−, and MCLK should not be present before the power supply is on. Violating this condition could cause latch-up. If these signals are present before the supply is on, series resistors should be used to limit the input current. Experimentation may be the best way to determine the appropriate connection between the ADS1203 and different power supplies.

Grounding

Analog and digital sections of the design must be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. Do not join the ground planes; instead, connect the two with a moderate signal trace underneath the converter. For multiple converters, connect the two ground planes as close as possible to one central location for all of the converters. In some cases, experimentation may be required to find the best point to connect the two planes together.

Decoupling

Good decoupling practices must be used for the ADS1203 and for all components in the design. All decoupling capacitors, specifically the 0.1µF ceramic capacitors, must be placed as close as possible to the pin being decoupled. A 1µF and 10µF capacitor, in parallel with the 0.1µF ceramic capacitor, can be used to decouple V_{DD} to GND. At least one 0.1µF ceramic capacitor must be used to decouple V_{DD} to GND, as well as for the digital supply on each digital component.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
1/08	C	1	Features	Changed upper Operating Temperature Range from +85°C to +125°C.
		2	Absolute Maximum Ratings	Changed upper Operating Free−Air Temperature Range from +85°C to +125°C.
			Recommended Operating Conditions	Changed upper Operating Junction Temperature Range from +105°C to +150°C.
			Dissipation Ratings	Deleted $R_{\theta JA}$ column.
				Changed values.
		3	Electrical Characteristics	Changed condition; upper temperature range from +85°C to +125°C.
				Added rows with values for updated temperature range.
				Changed values throughout table.
				Changed notes 5, 7, and 8.
		7, 8	Parameter Measurement Information	Changed upper temperature range for all four timing characteristics tables from +85°C to +125°C.
8/07	B	5	Equivalent Input Circuit	Moved Equivalent Input Circuit figure to bottom of page 5.
		6	Pin Assignments	Added note to QFN package.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1203IPWT	ACTIVE	TSSOP	PW	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AZ1203	Samples
ADS1203IRGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A03I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

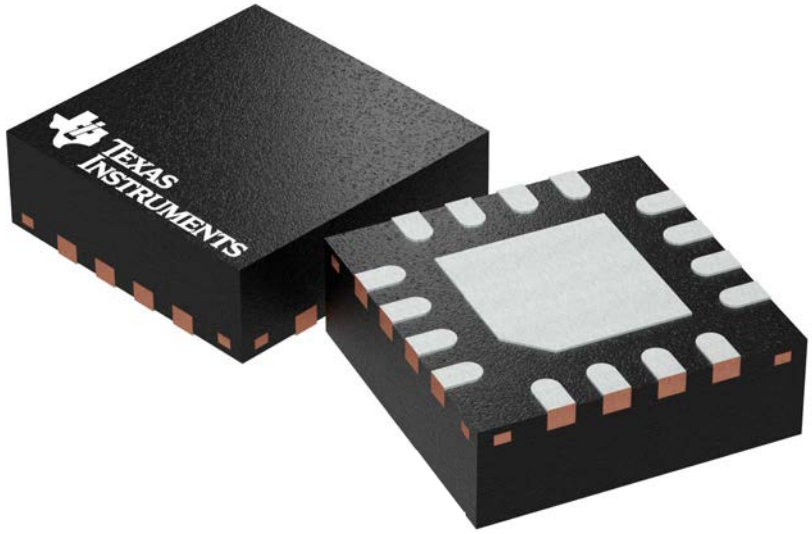
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



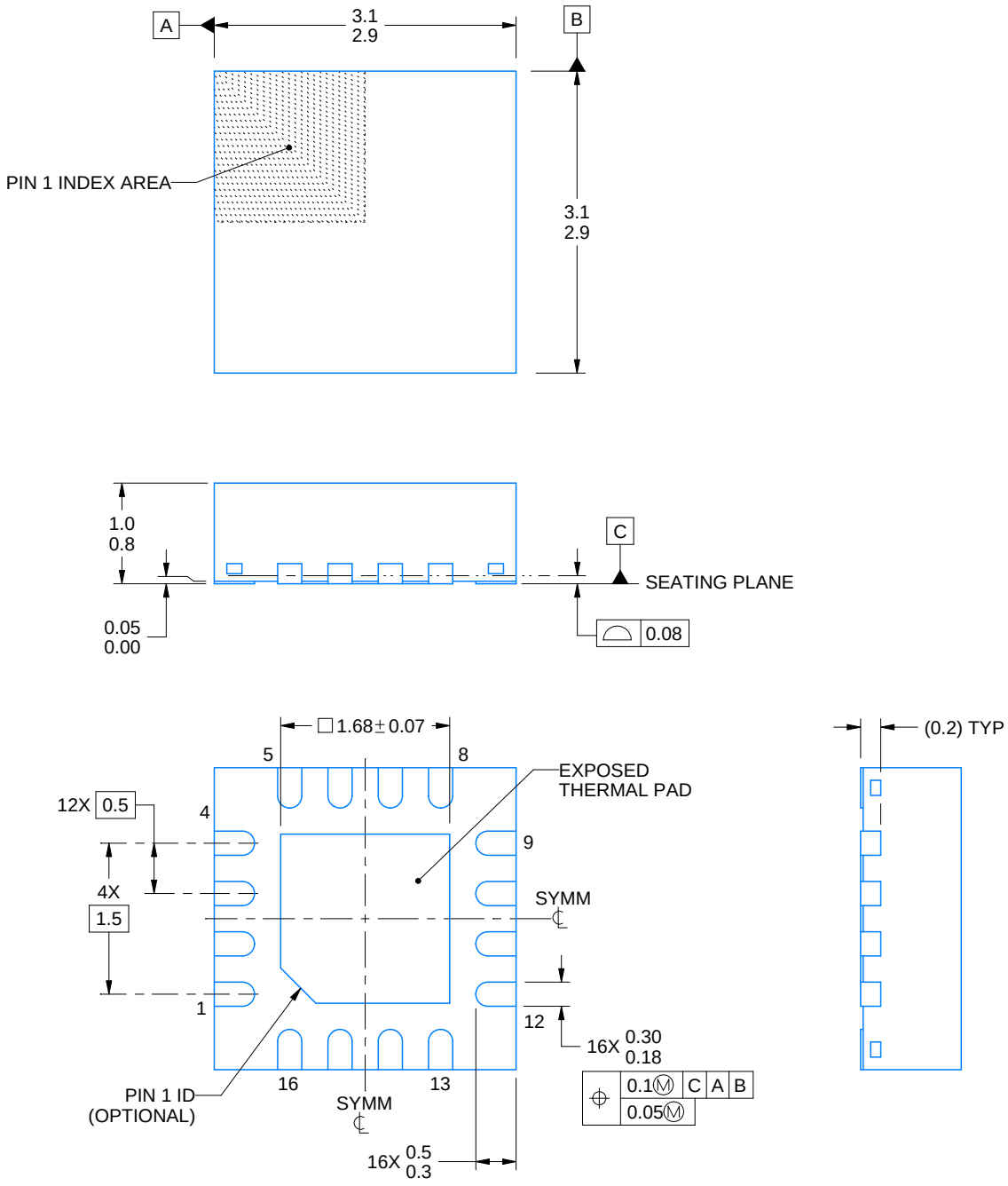
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016C

PACKAGE OUTLINE

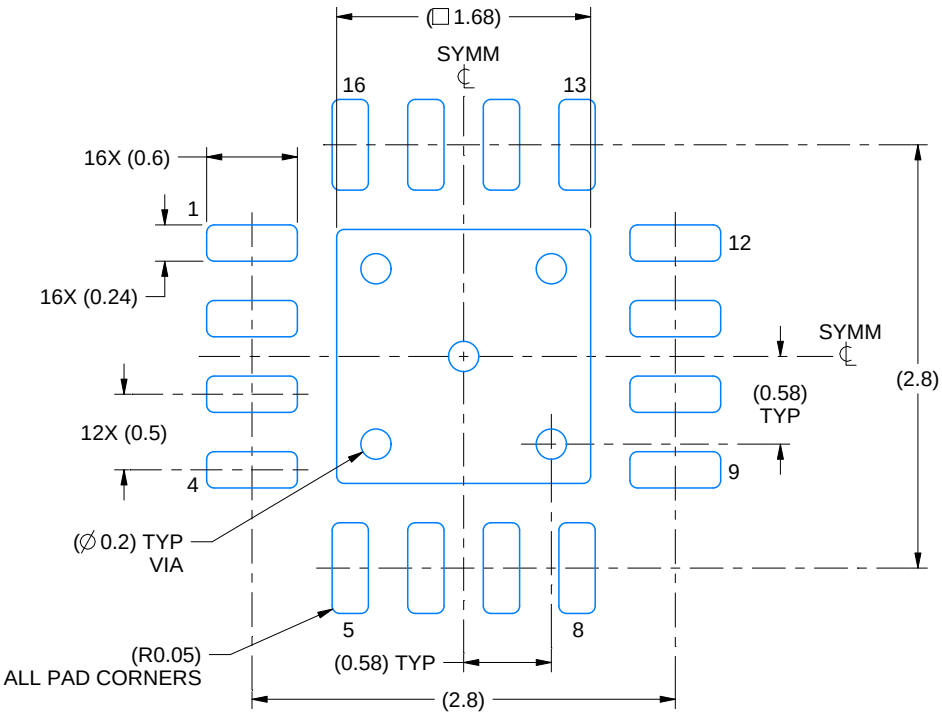
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

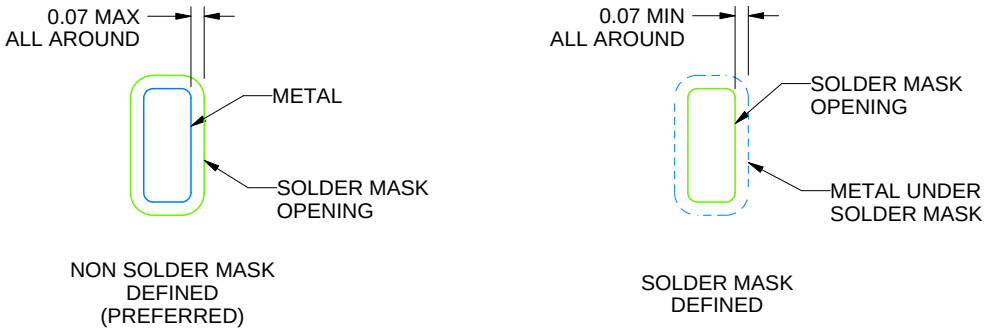


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

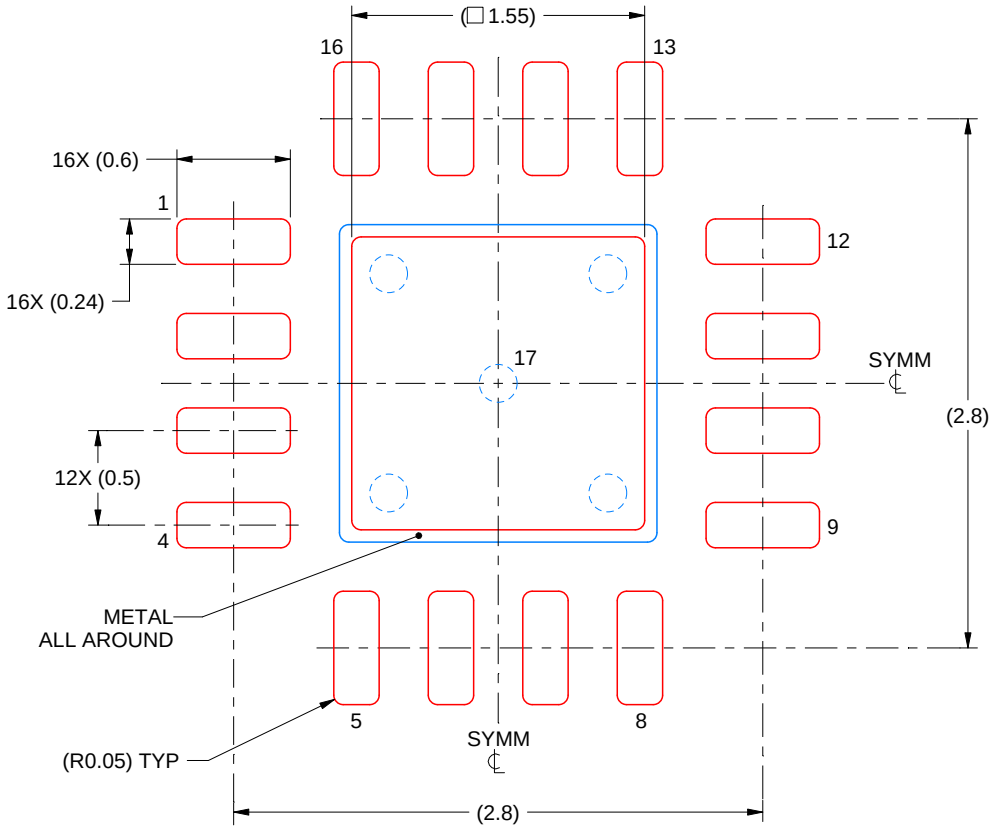


SOLDER MASK DETAILS

4222419/C 04/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/C 04/2021

NOTES: (continued)

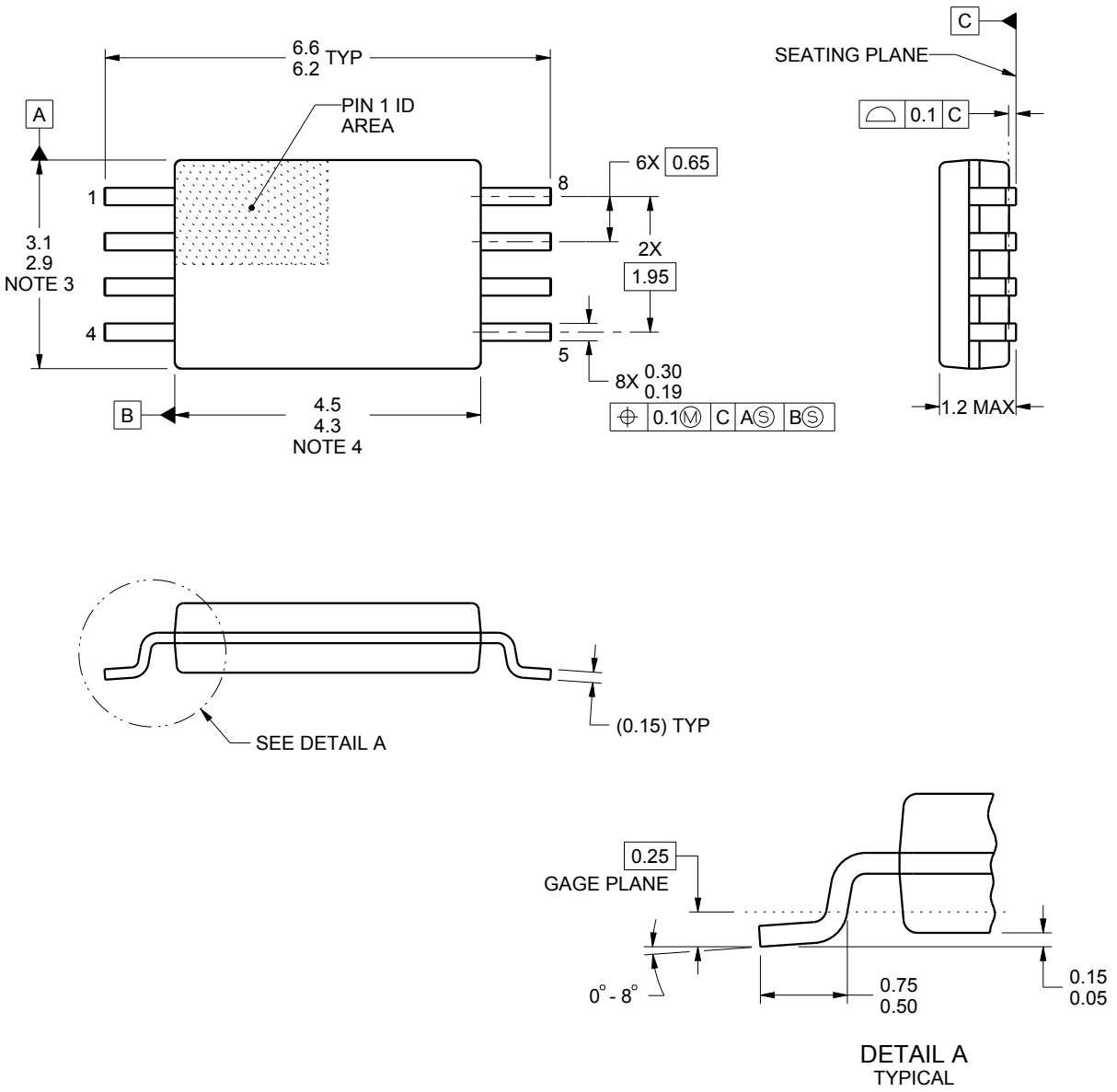
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

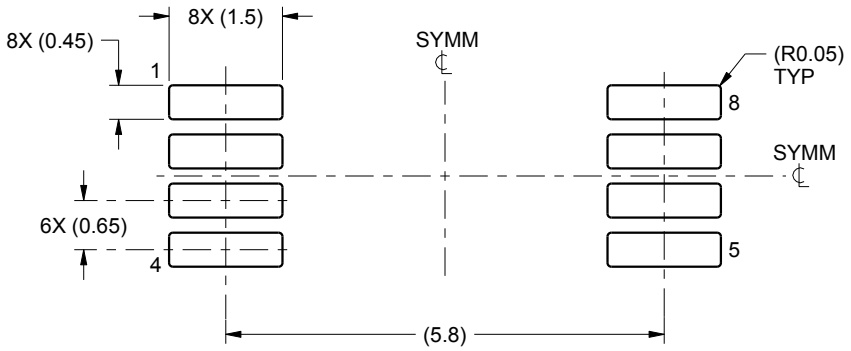
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

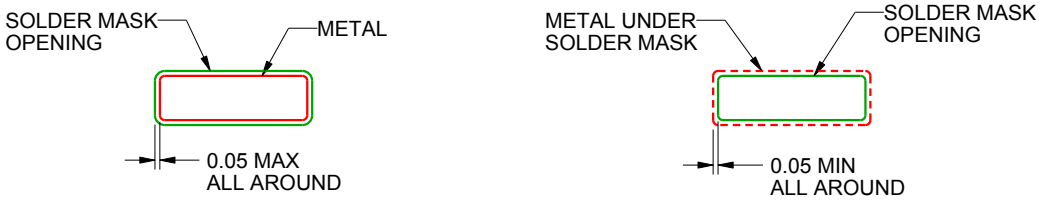


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

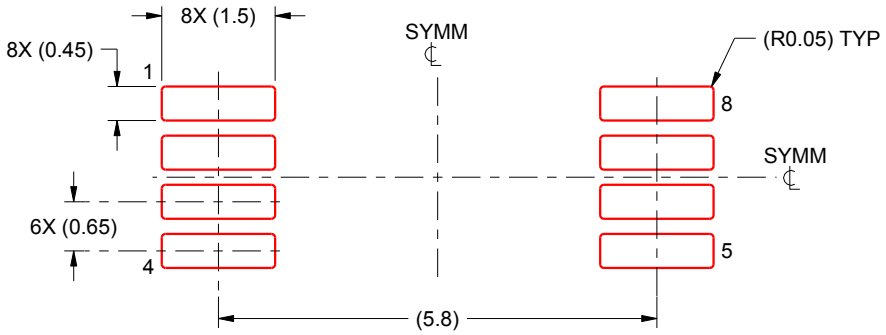


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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