ON Semiconductor®

Product Bulletin

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Issue Date: 3 November 2017

Title of Change:	MT9V124 Developer Guide Update.
Effective date:	3 November 2017
Contact information:	Contact your local ON Semiconductor Sales Office or <Sonya.Yip@onsemi.com>
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change category:	☐ Wafer Fab Change ☐ Assembly Change ☐ Test Change ☒ Other Documentation

Change Sub-Category(s):

☐ Manufacturing Site Change/Addition
☐ Manufacturing Process Change
☐ Material Change
☐ Product specific change
☒ Datasheet/Product Doc change
☐ Shipping/Packaging/Marking
☐ Other: _____

Sites Affected:	ON Semiconductor Sites: None	External Foundry/Subcon Sites: None

Description and Purpose:

MT9V124 Developer Guide was updated to correct documentation errors. Document was also converted to ON Semi format. The changes will not impact form, fit, or function of products.

MT9V124 Developer Guide Changes

1. Updated "Table 11, PLL Divider Equations"

Old Table 11:

Table 11: PLL Divider Equations

Param Setting	Description	Min Setting	Max Setting	Min_Reg	Max_Reg	Legal Setting
m	VCO output division	32	140	0x10	0x46	Inclusive
n	Input clock division	1	64	0x00	0x3F	Inclusive
p3	Output clock division	1	16	0x00	0x0F	0,1,3,5,7,9,11,13,15
F_{VCO}	VCO output frequency	280MHz	560MHz	–	–	
F_{bit_clock}	Bit clock	140MHz	280MHz	–	–	

The PLL output frequency will be set with the following equations:

New Table 11:

Table 11. PLL DIVIDER EQUATIONS

Param Setting	Description	Min Setting	Max Setting	Min_Reg	Max_Reg	Legal Setting
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n	Input clock division	1	64	0x00	0x3F	Inclusive
p3	Output clock division	1	16	0x00	0x0F	0,1,3,5,7,9,11,13,15
F_{VCO}	VCO output frequency	280 MHz	560 MHz	–	–	
F_{bit_clock}	LVDS_Serializer_Clock	140 MHz	280 MHz	–	–	

2. Updated Equations 1 and 2

Old Equations 1 and 2:

$$F_{vtsystemclock} = \frac{F_{in} \times m}{(n+1) \times (p3+1)} \quad \text{(EQ 1)}$$

$$F_{bitclock} = \frac{F_{in} \times m}{(n+1)} \quad \text{(EQ 2)}$$

New Equations 1 and 2:

The PLL output frequency will be set with the following equations:

$$F_{Internal\ PLL\ Clock} = \frac{F_{ext\_clk} \times m}{(n+1) \times (p3+1)} \quad \text{(eq. 1)}$$

$$F_{LVDS\_Serializer\_Clock} = \frac{F_{ext\_clk} \times m}{(n+1)} \quad \text{(eq. 2)}$$

Table 12 shows the related registers to program PLL and clock. Refer to the MT9V124 data sheet for more detail descriptions for the registers and variables.

3. Updated "Interface to Host Controller Section" to remove note

Old Section:

Interface to Host Controller

The MT9V124 interfaces with the MT9V124 through a serial Low Voltage Differential Signaling (LVDS). The High Speed LVDS output port on MT9V124 can transmit the sensor image data to the host system over a lengthy differential twisted pair cable. Image data is provided to the host system by the serial LVDS interface. The Start bit, 8-bit image data, LV, FV, and Stop bit are packetized in a 12-bit packet. The output interface block can select either raw data or processed data. Processed data formats include YCbCr, RGB-565, and BT656 with odd SAV/EAV code. It also supports the SOC Bypass 8+2 data format over the 12-bit packet.

The LVDS port is disabled when Hard Standby or Soft Standby is asserted.

(Please copy "Serial Low Voltage Differential Signaling (LVDS) Output" section from Page 28 to Page 29 [of what?] to here.)

Refer to Page 28-33 of the MT9V124 data sheet for more information on the two-wire serial interface, including read/write, etc.

Please refer to the data sheet for more information on LVDS output and two-wire serial interface.

New Section:

INTERFACE TO HOST CONTROLLER

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The LVDS port is disabled when Hard Standby or Soft Standby is asserted.

Refer to Page 28−33 of the MT9V124 data sheet for more information on the two−wire serial interface, including read/write, etc.

Please refer to the data sheet for more information on LVDS output and two−wire serial interface.

SOC TEST PATTERNS

The MT9V124 features an automatic color bar test pattern generation function to emulate sensor images as shown in Figure 11.

Color bar test pattern generation can be selected by programming a register.

List of Affected Parts:

MT9V124D00STCK22DC1-200

MT9V124EBKSTC-CR

Appendix A: Changed Products

Product	Customer Part Number
MT9V124EBKSTC-CR	